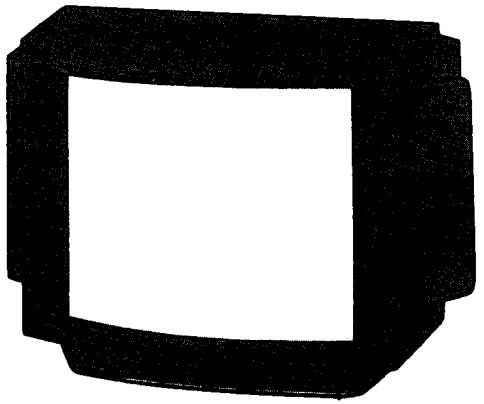
SONY

*Training Manual*

# 1989 Television Products

## ANU-1 Chassis

## Circuit Description



XBR

Course CTV-16

# Table of Contents

# ANU-1 Chassis

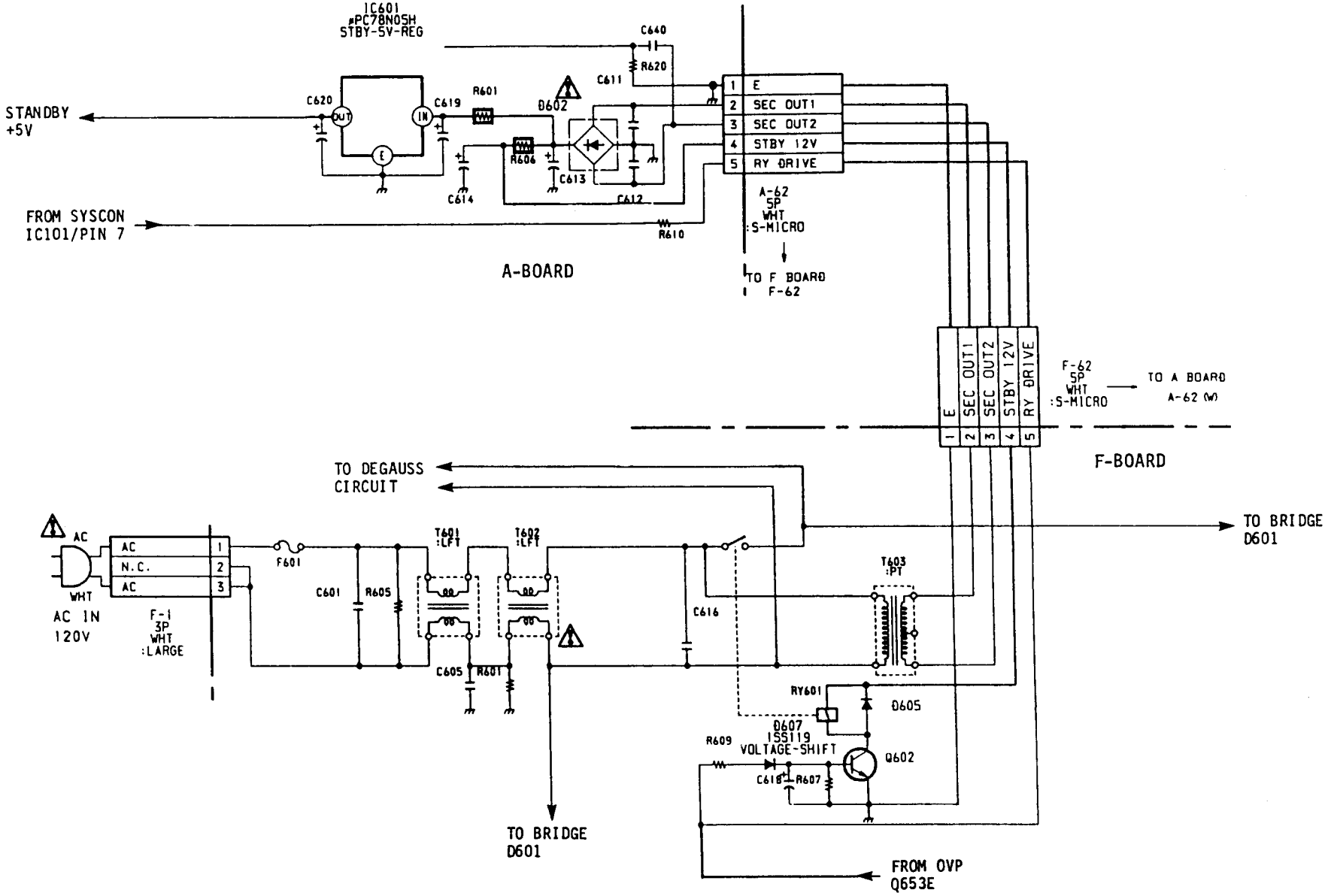
The ANU-1 chassis, introduced in mid 1989, is Sony's first chassis to employ the Philip Standard $1^2C$ bus for internal communication. Communication on this bus controls mode switching, adjustments, and safety functions. In this book we will examine the new features of the ANU-1 chassis. Sections of the ANU-1 chassis that are similar to the P-A chassis (CTV-15) will not be reviewed in this book.

## Standby Power Supply

AC line power is coupled through F601, T601 and T602 to the standby power transformer T603. Standby power from the secondary of T603 is coupled directly to D602. The 12V un-regulated power source (from D602) is filtered by C613 and coupled through R601 to the standby 5V regulator IC601. The regulated standby +5V from IC601 is then distributed throughout the set. The +12V unregulated supply is also coupled through R606 to the top of RY601.

When the set's power is OFF, IC101/pin-7 is LOW, Q602 is OFF and no current will flow through RY601. In this condition the contacts of RY601 are open, and only the standby power supply will be ON.

To turn the set's power ON, IC101/pin-7 will go HIGH, and Q602 will turn ON. Current will now flow through RY601 and its contacts will close. When the contacts of RY601 close, power will be applied to the degaussing circuit and D601 (bridge rectifier).




**STANDBY POWER**

## Standby/Power Control

Since IC101 is responsible for turning the set's power OFF and ON, IC101 must remain active at all times. Standby +5V is applied to IC101/pin-1 through L101 and D106. IC101 also requires a reset pulse at IC101/pin-27, and a clock at IC101/pin-28 and pin-29. Reset for IC101 is provided by IC103. The clock's frequency (4MHz) is controlled by R127 and X101.

Requests for power ON/OFF can come from either the front panel power switch (S51), or a remote control hand unit. IC51, the sircs detector, captures and demodulates the infrared remote control signal. IC1701 "decodes" the sircs signal and transfers the remote data to IC101.

When the front panel power button is pressed S51 will close, and IC101/pin-25 will be pulled LOW.

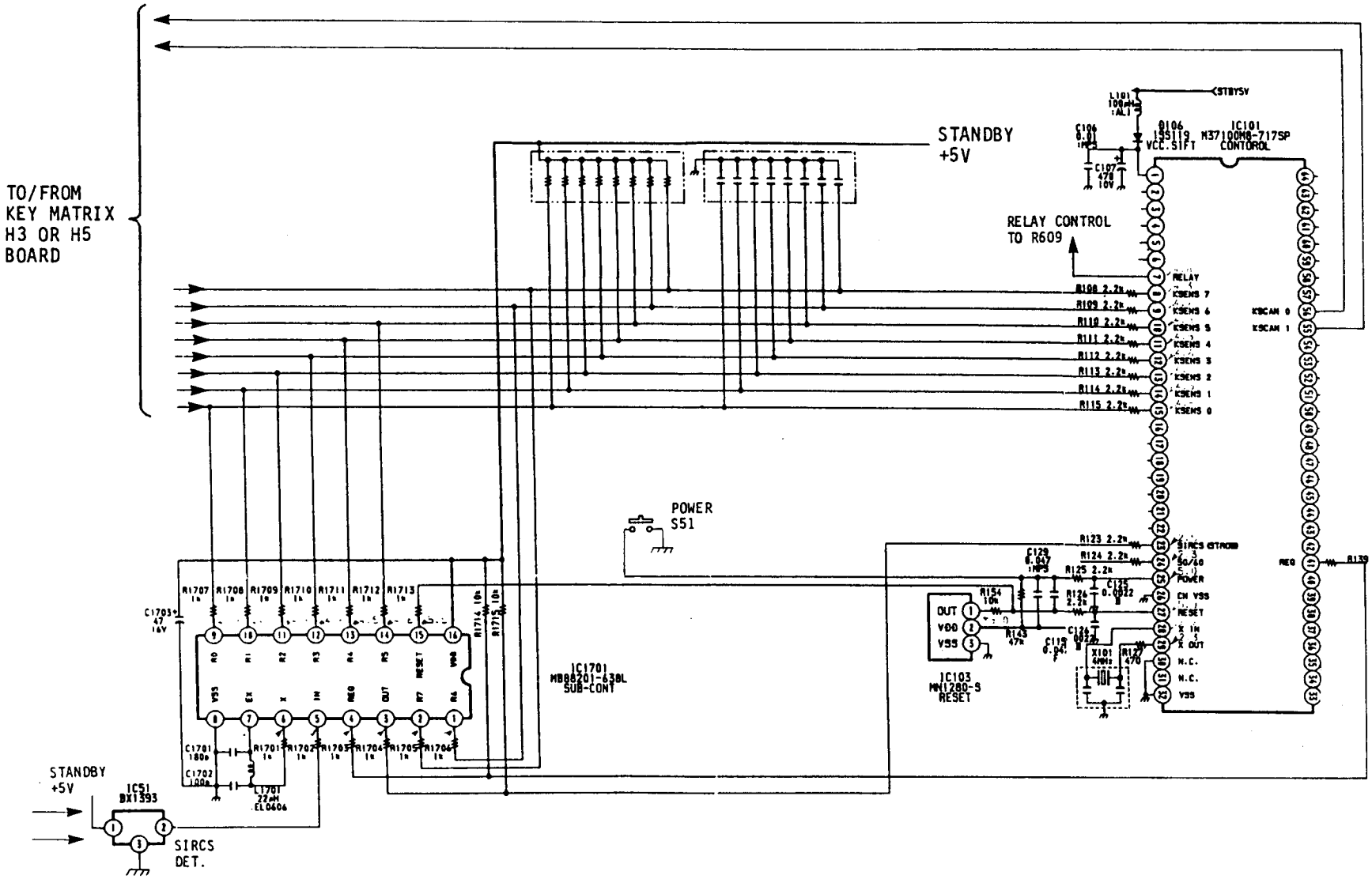
A short low pulse, caused by the charging of C115, will be applied to IC101/pin-27 (reset) at this time. In response to IC101/pin-25 going LOW, IC101 will change the state of IC101/pin-7.

For remote control operation, the infrared sircs signal is detected and demodulated by IC51. The demodulated sircs signal is coupled to IC1701/pin-5. When IC1701 detects a proper sircs signal at IC1701/pin-5, it will output a "HIGH" output signal at IC1701/pin-3. This signal is coupled through R1704 and R123 to IC101/pin-23. When IC101 detects a HIGH at IC101/pin-23, it will output high request pulses at IC101/pin-41.

These pulses occur during vertical blanking and are coupled through R139 and R1703 to IC1701/pin-4. When IC1701/pin-4 detects these request pulses, it will generate "remote control" data pulses at 1701/pin-1, pin-2, and pins-9 through 14. These pulses, which occur during vertical blanking, are detected by IC101 at the sens inputs at IC101/pins-8 through 15.

The sens inputs at IC101/pins-10 through 15 are also used to detect key closures from the front panel user controls. With no key switches closed, IC101/pins-10 through 15 are pulled up by the resistors in CP110. When a key switch is closed, one of the sens inputs (IC101/pins-10 through 15) will be coupled to one of the scan outputs (IC101/pin-55 and pin-56). Initially the scan outputs are both LOW. This "LOW" will pull down the associated scan input. When IC101 detects a LOW at one of its sens inputs it will output two unique pulse trains, one at IC101/pin-55, and one at IC101/pin-56. By examining the pulse train at the sens input, IC101 can determine which button has been pressed.

The sens inputs at IC101/pin-8 and pin-9 are used to detect the video label and channel caption features. If these features are included in the set, pulses from IC101/pin-55 are permanently coupled (through diodes) to the sens inputs at IC101/pin-8 and pin-9.




**STANDBY/POWER CONTROL**

## Power Supply Block

The main power supply for the ANU-1 is contained on the F board. IC651, T651 and the associated components form an oscillator. Regulation of the B+ (135V) line is performed by changing the frequency of the oscillator. As the current demand on the B+ supply increases, the frequency of the oscillator will decrease.

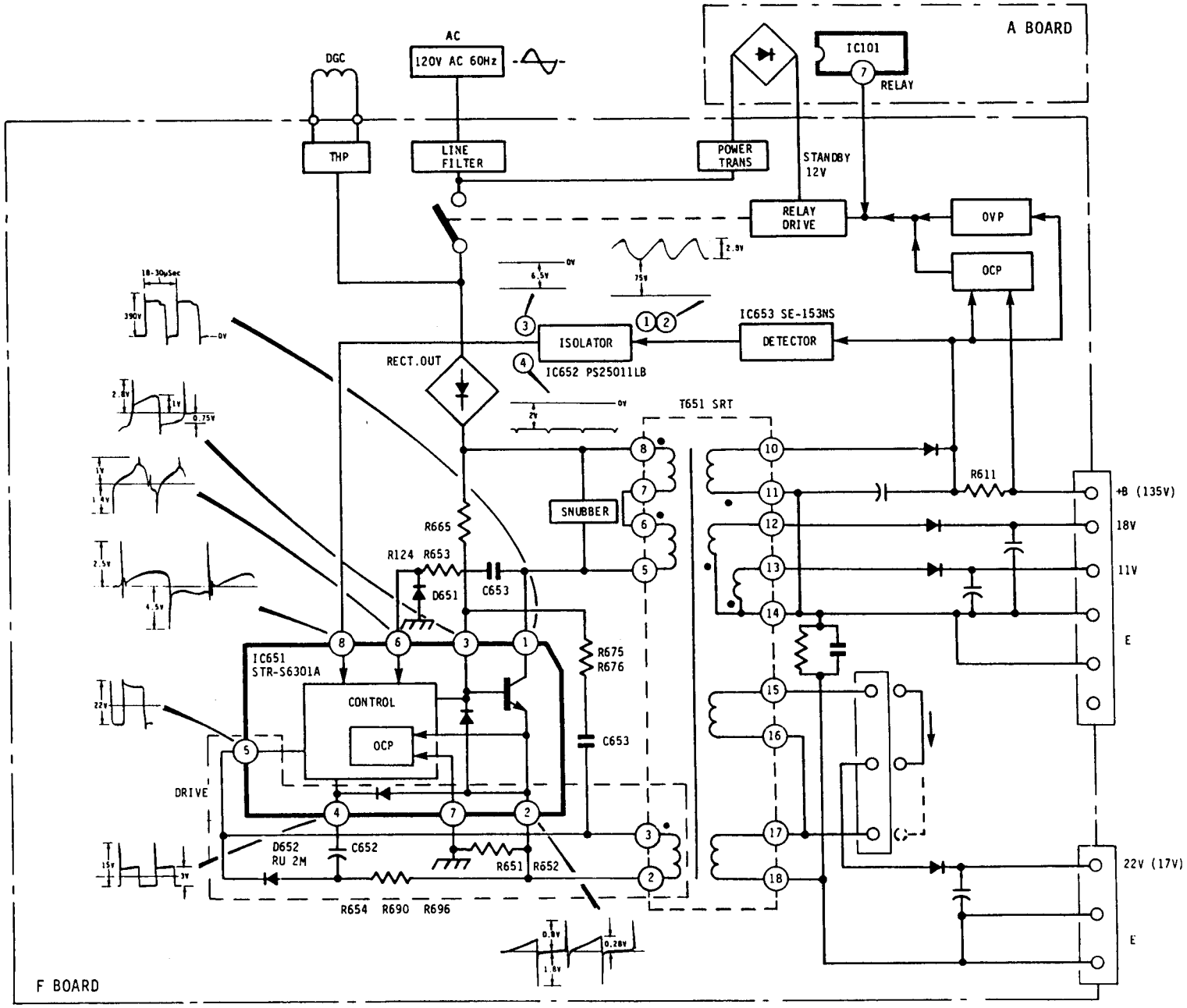
The B+ voltage is monitored by IC653. The B+ level detect signal is then coupled through an optical isolator (IC652) and input to IC651 for frequency control. The optical isolator is necessary since the oscillator (IC651 and associated components) circuitry uses AC ground (hot) and the output circuitry (T651 supply secondaries and associated components) uses an isolated ground (chassis ground). This should be noted for servicing the power supply to prevent erroneous reading due to ground loop problems.

Line current is rectified by D601 and coupled through T651/pins-8, 7, 6, and 5 to IC651/pin-1. Feedback for oscillation is provided by T651's secondary at T651/pin-2 and pin-3. T651/pin-2 is coupled directly to IC651/pin-2 and T651/pin-3 is coupled directly to IC651/pin-3.

The power supply is protected by two types of over current protection (OCP). Current in T651's primary is monitored by IC651. T651's primary is in series with the parallel resistor combination R651/R652. As current through the primary increases, the voltage drop across R651/R652 will also increase. If this voltage becomes excessive, the OCP circuit inside IC651 will prevent IC651 from oscillating. The other OCP circuit monitors current in the B+ supply by measuring the voltage drop across R611. If the voltage drop across R611 becomes excessive, the OCP circuit will disable the relay drive signal, the relay's contacts will open and power will be removed from D601.

An over voltage protection circuit also monitors the B+ line. If the B+ voltage becomes excessive the OVP circuit will disable the relay drive signal, removing power from D601.

The power supplies four outputs. The B+ (135V) 18V and 11V sources are used primarily for the receiver, and video processing portions of the set. The other supply output can be switched between 22V and 17V by moving a plug in jumper. This supply is used by the audio output section of the set.




**POWER SUPPLY BLOCK**

# Power Supply

Rectified line current from D601 is coupled through R602 and FB658 to T651/pin-8. Power for IC651 is then coupled through T651/pins-8, 7, 6, and 5, and FB660 to IC651/pin-1. IC651 will oscillate using feedback from T651/pin-2 and pin-3.

The secondary winding at T651/pin-10 is rectified to provide B+ and T651/pin-11 is connected to chassis ground. The current from T651/pin-10 is rectified by D660, filtered by C666, R611, L657, C651, and C650. The B+ supply is then distributed throughout the set.

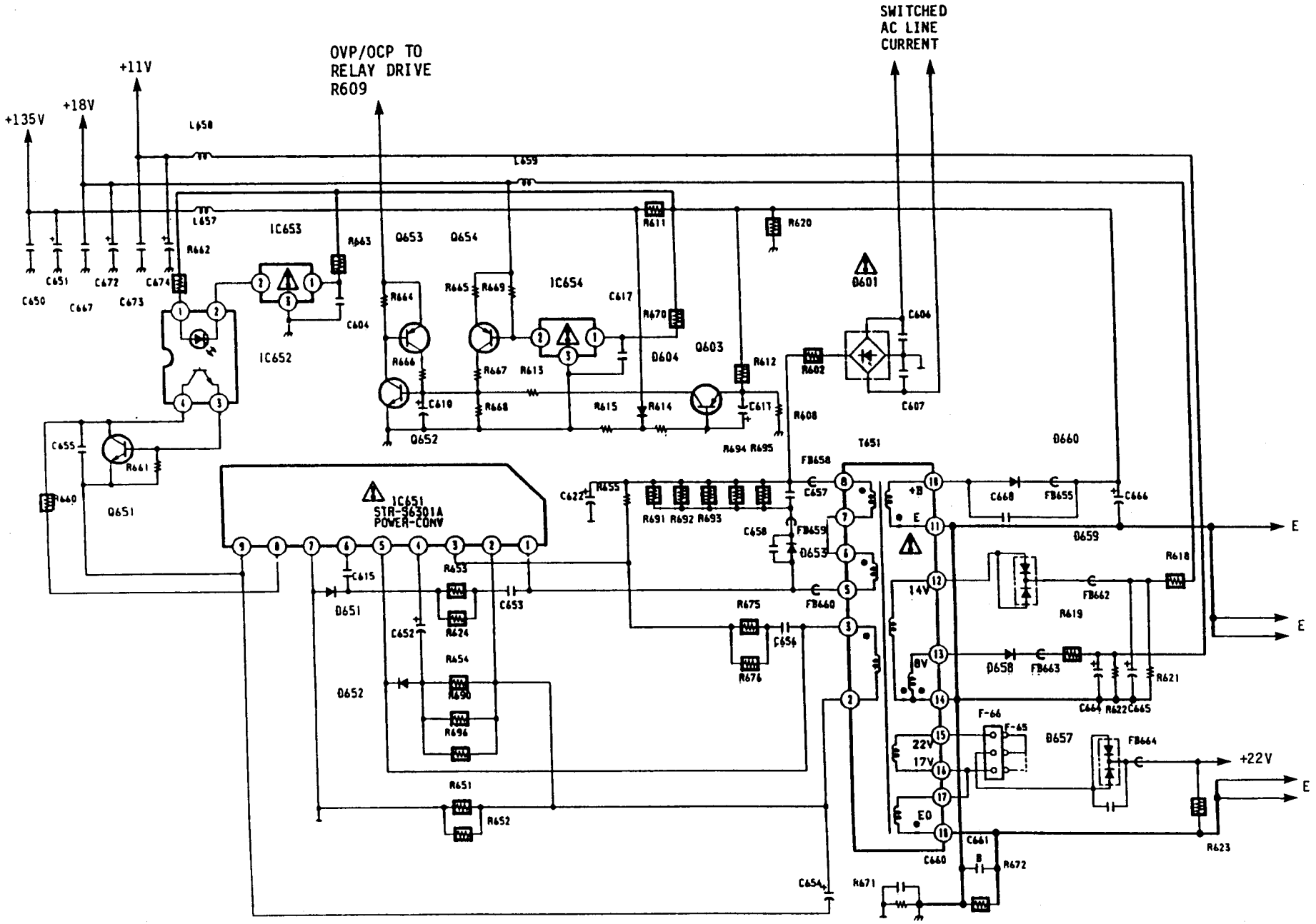
The +135V is also coupled through R6633 to IC653/pin-1. IC653 is a voltage regulator. The output at IC653/pin-2 provides a constant reference voltage to IC652/pin-2. The +135V supply, without additional regulation, is coupled through R662 to IC652/pin-1. Since the voltage at IC652/pin-2 is regulated by IC652, and the voltage at IC652/pin-3 is regulated only by IC651, any change in the level of the B+ (135V) line will be reflected by a change in the emission of the led at IC652/pin-1 and pin-2. As the led's emission changes, the conduction of the photo transistor at IC652/pin-3 and pin-4 will also change. This will alter the conduction of Q651 and change the voltage at IC651/pin-8 and pin-9. When the voltages at IC651/pin-8 and pin-9 change, IC651's oscillating frequency will change, keeping a constant 135V B+ level.

Q603, D604 and the associated components form the B+ over current protection circuit. Normally the base of Q603 is pulled up through D604 and R614.

As current in the B+ line increases, the voltage drop across R611 increases, and the voltage coupled to the base of Q603 decreases. When the voltage at the base of Q603 decreases to an unsafe level, Q603 will turn ON. When Q603 turns ON, its collector will go HIGH and Q652 and Q653 will turn ON. When Q652 and Q653 turn ON, the relay drive signal will be pulled down through R664 and Q652 C-E. This will disengage the relay and remove power from D601.

The voltage level of the B+ line is monitored by IC654. The B+ supply is coupled through R670 to IC654/pin-1. Normal B+ voltage (135V) turns IC654 ON, and IC654/pin-2 is HIGH. If the B+ voltage becomes excessive, IC654 will turn OFF, IC654/pin-2 will go LOW, and Q654 will turn ON. When Q654 turns ON, its collector will go HIGH, and Q652 and Q653 will turn ON.

Please note that the +22V, +18V, and +11V sources are not monitored by the regulation circuitry. Large fluctuations in the load on the B+ line may cause small changes in the voltage levels of these supplies. If this power supply is operated in a no-load condition, the B+ line will retain regulation, however, the other supplies will have lower than normal voltages.




**POWER SUPPLY**

## $I^2C$ Bus

In recent years, as television circuitry becomes more and more "digital", communication bus lines have become a regular feature in most TV chassis. Usually data and clock lines are connected in parallel from the system controller to many different processing circuits. To direct data to a specific device, an independent circuit "chip select" or "latch" line is used. The $I^2C$ bus uses only the clock and data lines. Data is directed to a specific device by "address control". Data in the $I^2C$ format forms blocks consisting of:

1) Start Bit

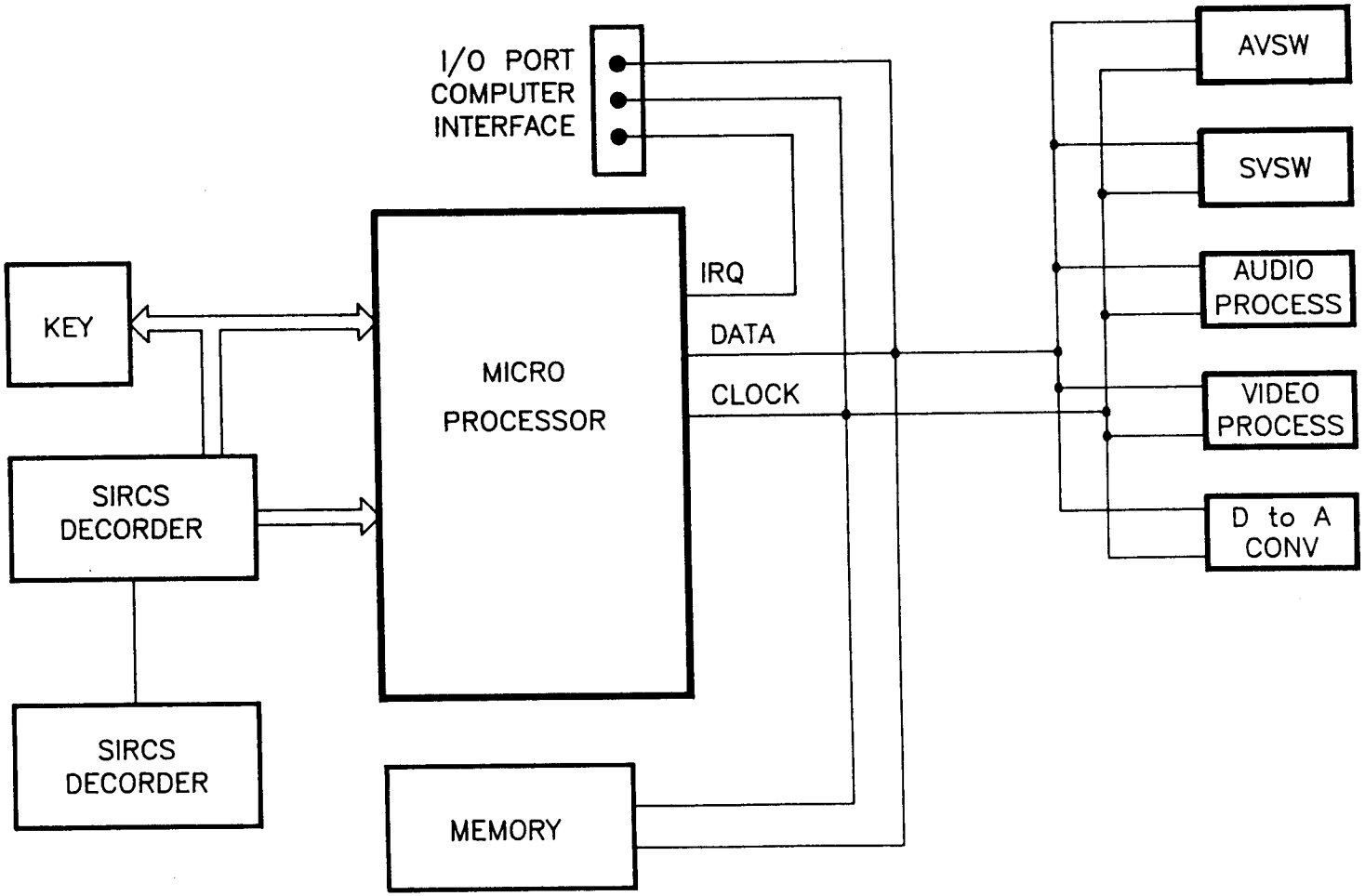
2) Address word and acknowledge bit

3) At least one data word and acknowledge bit

4) Stop Bit

Using this format, no chip select signals are necessary. Any given device will only accept data if it has the correct address word.

In addition to simplifying the hardware, the $I^2C$ bus format allows for easy interface with external computer equipment. Most adjustments (both user and service) in the ANU-1 chassis are performed via the data bus. During manufacture, a computer performs the initial alignment of the set via the data bus. Normally, the set's internal microprocessor controls the peripheral components via the data bus. An interrupt request (IQ) line enables an external computer to stop data from the internal microprocessor. The external computer then takes control of the peripheral components via the data bus. When the alignment process is complete, the alignment data will be written into the non-volatile memory and the microprocessor.


I/O PORT
COMPUTER
INTERFACE
IRQ
DATA
CLOCK
KEY
MICRO
PROCESSOR
SIRCS
DECORDER
SIRCS
DECORDER
MEMORY
AVSW
SVSW
AUDIO
PROCESS
VIDEO
PROCESS
D to A
CONV

**$I^2C$ BUS**

## Data Format

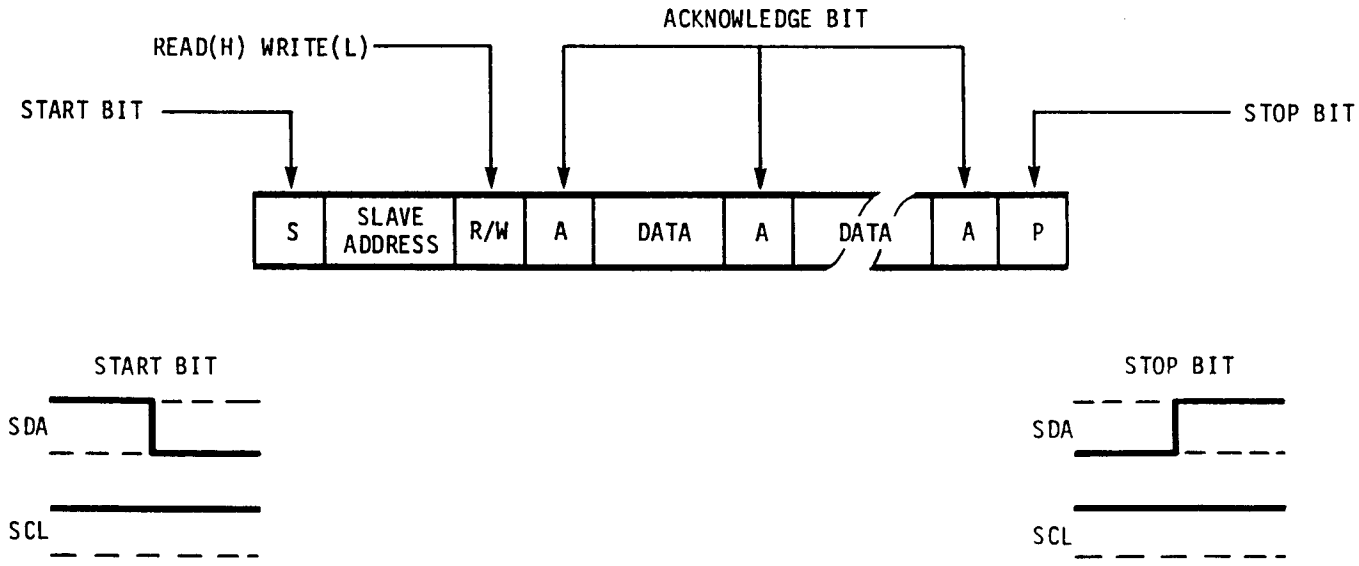
The format of the data on the bus is tightly controlled. Each device controlled by the bus must be able to recognize its address. The beginning of any data transfer is a "start bit". A start bit has no clock pulse. Any time the data line falls from HIGH to LOW with no clock pulse, all devices will recognize this as the beginning of a data transfer. Immediately following a start bit is an address word. The address word consists of a seven-bit address followed by a read/write bit. The seven-bit word will identify the device that the system controller would like to communicate to. The read/write bit will be LOW when the system controller wants to write data into the addressed device. If the system controller wants to read data from the addressed device, the read/write bit will be HIGH. The complete address word is an eight-bit word containing both the address and read/write information.

Following the address word is an acknowledge bit. During an acknowledge bit, the system controller's data I/O port will assume a high impedance state. The data line will go HIGH because of external pull-up circuitry. The system controller will then output a single clock pulse for the acknowledge bit. As the addressed device detects this clock pulse, it must pull the data line LOW to acknowledge the receipt of the address information. The system controller must detect the acknowledge bit before it will begin data transfer.

Following the first acknowledge bit, data will be transferred into eight-bit words. An acknowledge bit will follow each word. The acknowledge bit following a data word is exactly the same as the acknowledge bit following the address word. The data may be an output from the system controller or an input to the system controller, depending on the state of the read/write bit. The clock is always an output from the system controller.

Any number of data words may follow a single address word. When communication with the addressed device is finished, the system controller will output a stop bit. The stop bit is similar to a start bit in that there is not clock pulse. The stop bit, however, is a data line transition from LOW to HIGH (the start bit from HIGH to LOW).

As usual with Sony televisions, all data transfer occurs during vertical blanking. For this reason data is best observed using a dual trace scope which is triggered by vertical sync from the composite video signal.


ACKNOWLEDGE BIT
READ(H) WRITE(L)
START BIT
STOP BIT
S
SLAVE ADDRESS
R/W
A
DATA
A
DATA
A
P
START BIT
SDA
SCL
STOP BIT
SDA
SCL

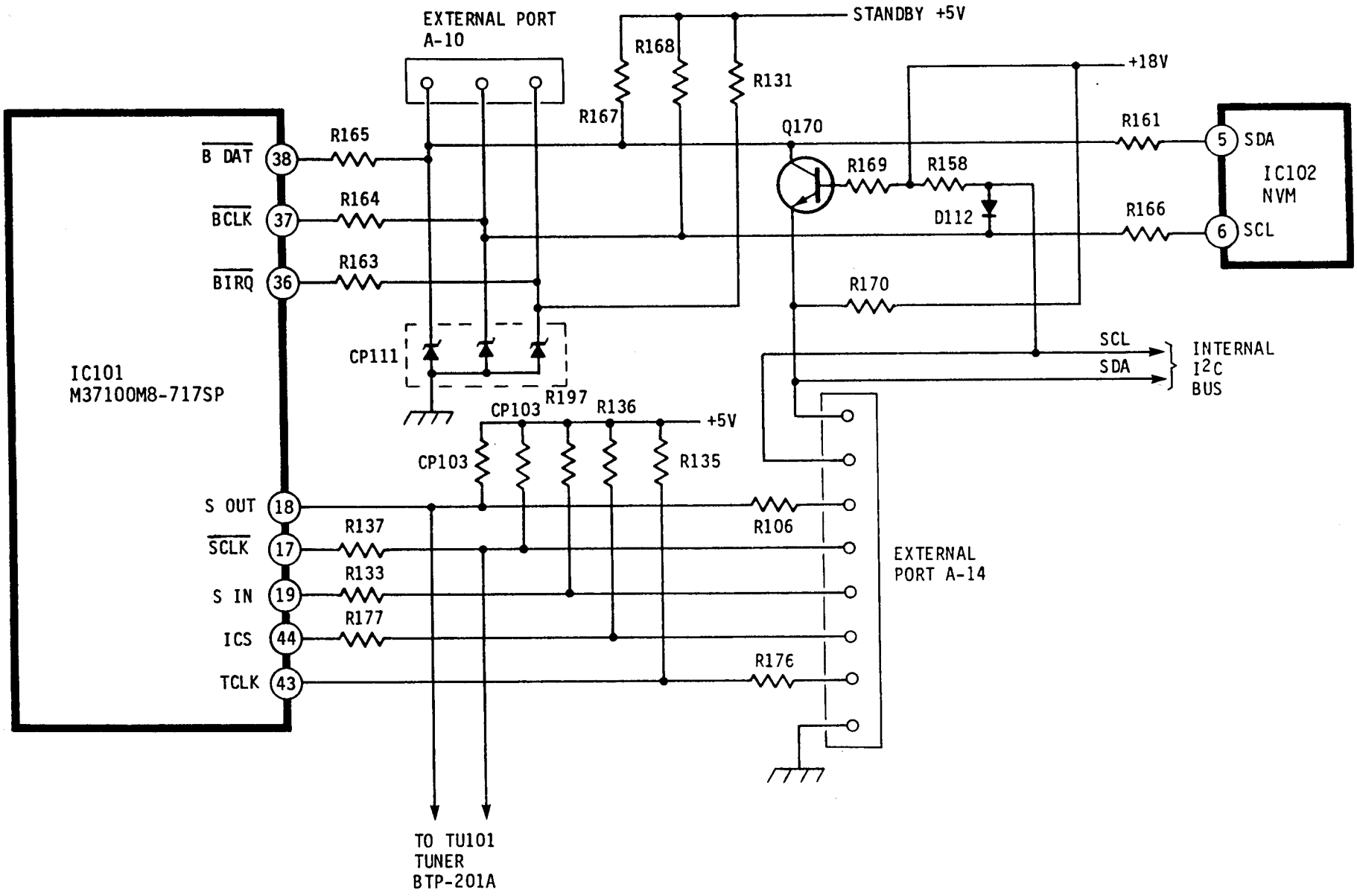
**DATA FORMAT**

## $I^2C$ Bus/External Port

The data and clock ports for IC101 (SYSCON) are located at IC101/pin-38 (data) and IC101/pin-37 (clock). The clock signal from IC101/pin-37 is coupled through R164 and D112 to the main bus. The clock signal for the non-volatile memory (IC102) is coupled through R164 and R166 to IC102/pin-6. Data is coupled to/from IC101/pin-38, through R165, and Q170 (C to E) and to the main bus. Data between IC101 (SYSCON) and IC102 (N.V.M.) is coupled through R165 and R161 between IC101/pin-38 and IC102/pin-5. Under normal conditions this is the only activity present in the $I^2C$ bus circuitry.

Data transfer to the PLL tuner (TU101) has its own independent bus. The data output for tuning is IC101/pin-18. This data is synchronized to the clock at IC101/pin-17. These ports are output ports and, like the $I^2C$ bus, are active only during vertical blanking.

The external ports at connectors A-10 and A-14 are used to interface the ANU-1 chassis with a computer during manufacturing. The computer takes control of the bus through the interrupt input at IC101/pin-36. When the computer brings IC101/pin-36 LOW (through R163), all normal communication will be interrupted. The computer can then insert data and clock signals on to the bus through the connector A-10, or A-14. Data to the tuner can be monitored or substituted at connector A-14. Serial in, chip select, and transfer clock ports are also provided at A-15. These allow independent communication with IC101. Under normal operation there are no connections to the A-10 and A-14 connectors.



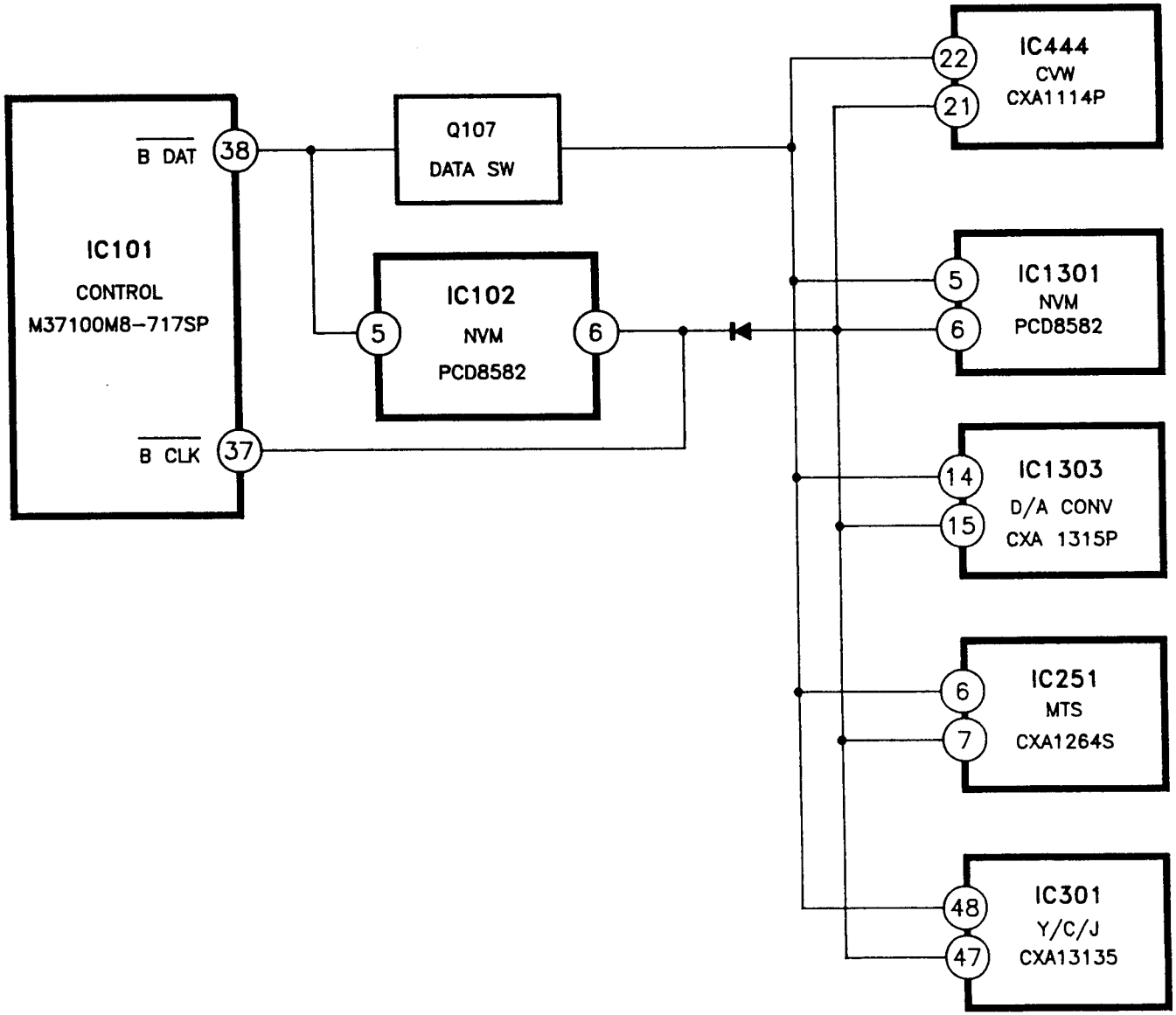

**I²C BUS/EXTERNAL PORT**

## $I^2C$ Bus/ANU-1 Chassis

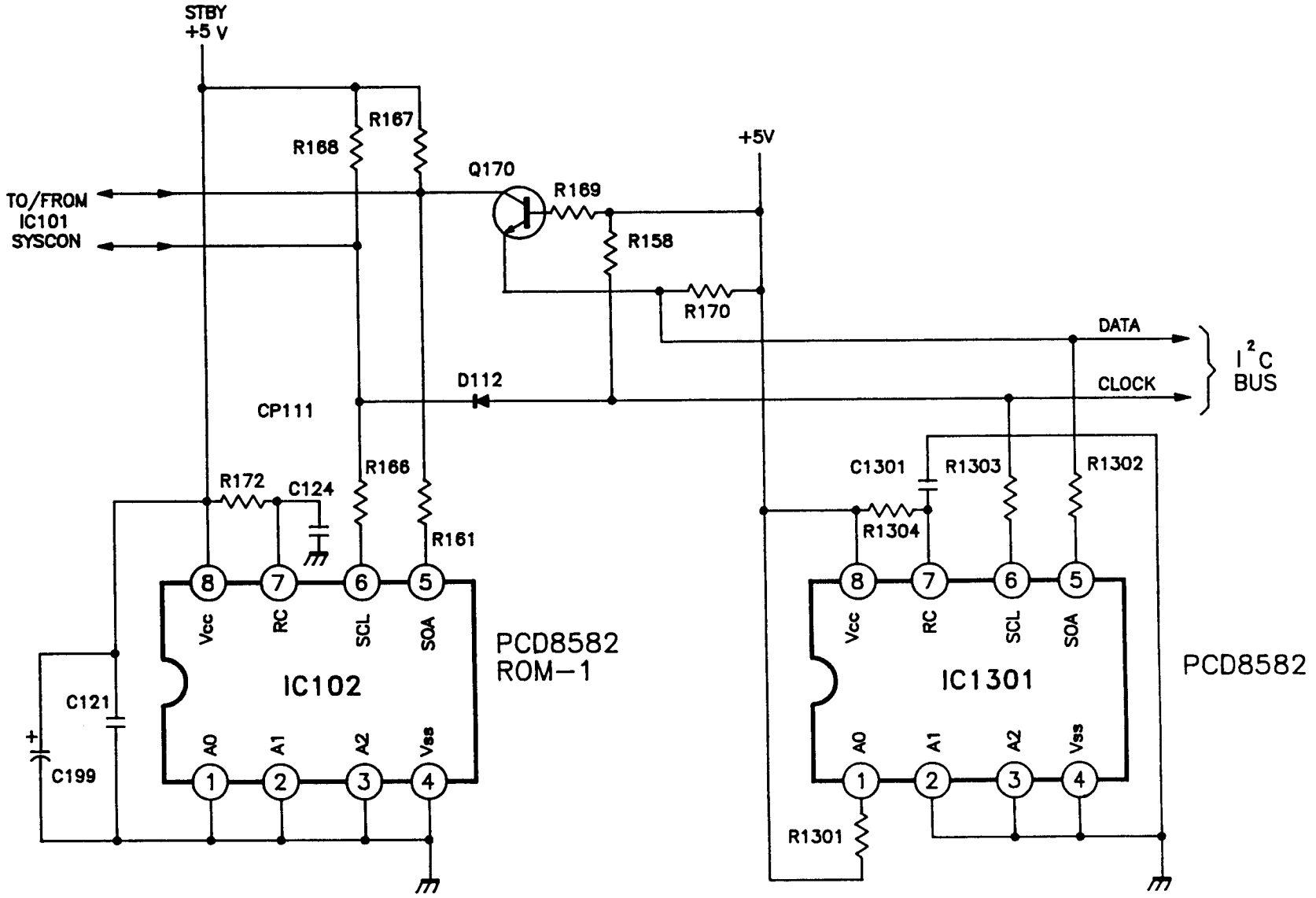
There are seven digitally controlled devices connected to the $I^2C$ bus in the ANU-1 chassis. All of these devices, of course, accept data following the $I^2C$ format. The following table provides a brief description of each device and shows the $I^2C$ bus data and clock port locations.

| IC | Description | Data | Clock |
|---|---|---|---|
| IC101 | M37100M8-717SP System Controller | 38 | 37 |
| IC102 | PCD8582 Non-Volatile Memory (Adjustment) | 5 | 6 |
| IC1301 | PCD8582 Non-Volatile Memory (CH Caption) | 5 | 6 |
| IC444 | CXA1114P Audio/Video Switch | 22 | 21 |
| IC251 | CXA12645S MTS Audio Decoder | 6 | 7 |
| IC301 | CXA1313S Y/C/Jungle | 48 | 47 |
| IC303 | CXA1315P D/A Conv Sharpness CTL | 14 | 15 |

IC101 is the main system controller. Normally the adjustment and operation data are stored in its RAM. When standby power is removed from IC101, it loses its RAM stored memory. When standby power is restored, IC101 will read the adjustment data from the non-volatile memory IC102. IC1301 is also a non-volatile memory. Data for the channel caption and video label features are stored in this memory IC. IC444 switches sources between TV (internal tuner), Video 1, Video 2, and Video 3 sources. The audio and video signals are switched simultaneously. IC251 is the MTS stereo audio decoder mode selection (main, mono, sap), and adjustments are controlled by the bus. IC301 is the Y/C/jungle circuit. Most of the picture control and scan adjustments are performed inside of IC301. All of these adjustments are controlled by the $I^2C$ bus. IC1303 is a D to A converter. It is used to control the sharpness amp/noise reduction circuit (IC1302).




**I²C BUS/ANU-1 CHASSIS**



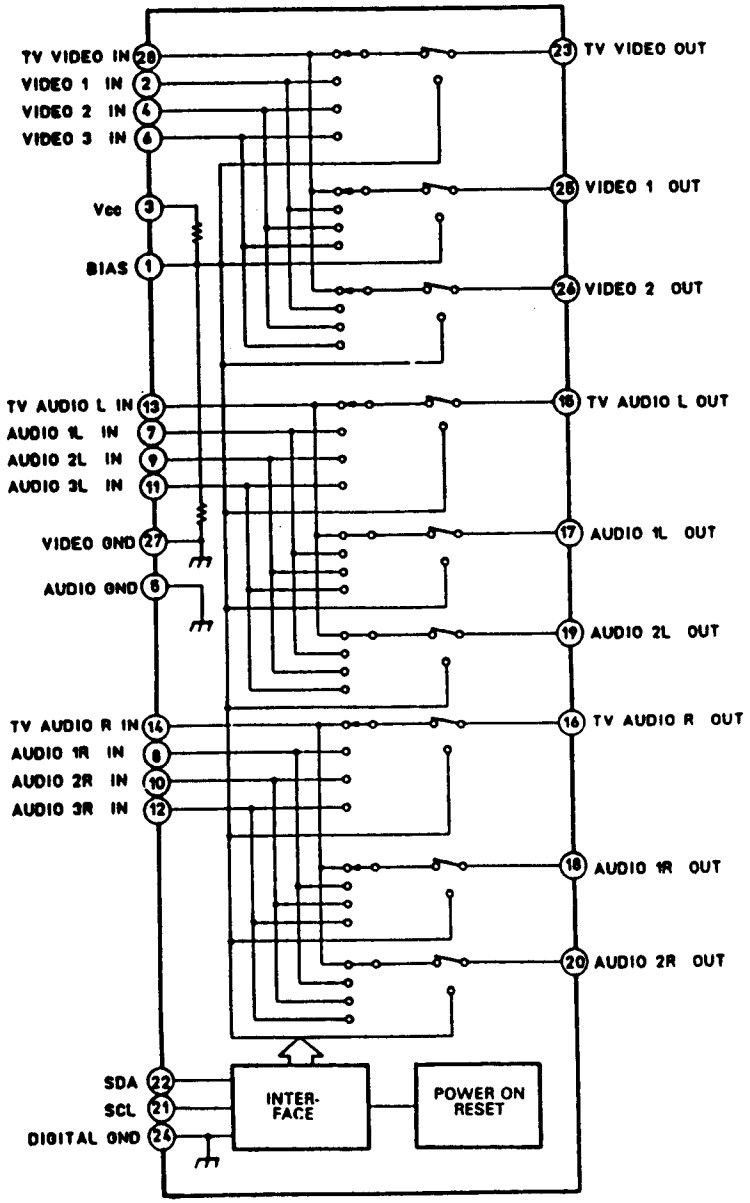

**NON-VOLATILE MEMORY**

## Non-Volatile Memory

In the XBR series of ANU-1 chassis TV receivers there are two non-volatile memories. IC102 stores the adjustment data along with the channel up/down memory data. IC1301 stores the channel caption and video label data. Since the channel caption and video label features are not included on the HSR models, this IC is deleted.

The data port is at pin-5 and the clock port at pin-6. Of course there are no chip select, output enable, or read/write control ports. Since both memories are connected to the bus in parallel, IC101 must have a way of addressing each IC individually. This is accomplished via the address control ports at pins-1 through 3. Notice that IC102/pin-1 is grounded, and IC1301/pin-1 is pulled up. By changing the states of pins-1, 2, or 3, the IC will respond to different addresses.

## U BOARD IC444 CXA1114P

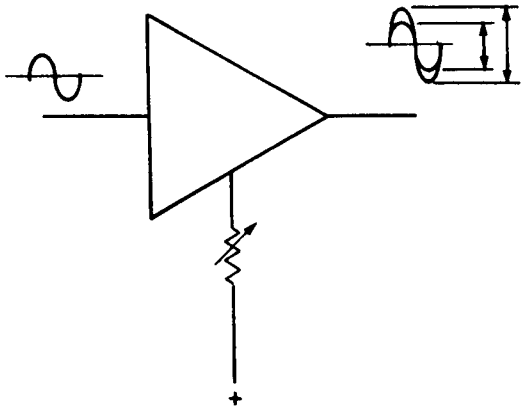



**AUDIO/VIDEO SELECTOR**

## Audio/Video Selector

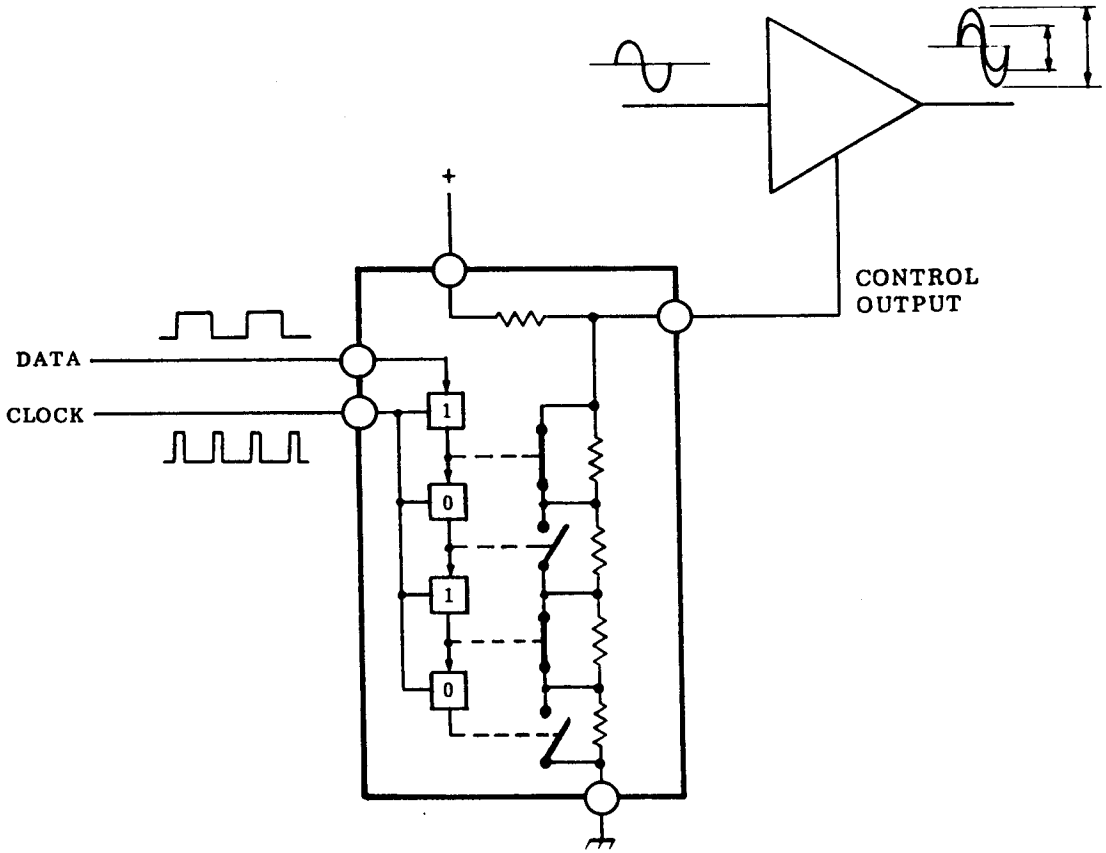
IC444 is the audio/video selector. TV video is coupled to IC444/pin-28, video 1 to IC444/pin-2, video 2 to IC444/pin-4, and video 3 to IC444/pin-6. Video from the video output at IC444/pin-23 is coupled to the rear panel video output connector and the comb filter CM1301. The video outputs at IC444/pin-25 and pin-26 are not used in this chassis. Left TV audio is input at IC444/pin-13, video 1 left audio at IC444/pin-7, video 2 left audio at IC444/pin-9, and video 3 left audio at IC444/pin-11. The switched left audio output from IC444/pin-15 is coupled to the rear panel audio output jacks (fixed level) and also the MTS decoder pack. The audio outputs from IC444/pin-17 and pin-19 are not used in this chassis. Right TV audio is input to IC444/pin-14, video 1 right audio to IC444/pin-8, video 2 right audio to IC444/pin-10 and video 3 right audio to IC444/pin-12. The right audio output from IC444/pin-16 is coupled to the rear panel audio output jacks (fixed level) and also the MTS decoder pack. The outputs at IC444/pin-18 and pin-20 are not used in this chassis.

The switch positions (internal to IC444) are controlled by the $I^2C$ bus. The bus inputs to IC444 are at IC444/pin-22 (data) and IC444/pin-21 (clock).




VARIABLE
RESISTOR
GAIN
CONTROL

Fig.A




EVR
GAIN
CONTROL

Fig.B

**ELECTRONIC VARIABLE RESISTOR**

# Electronic Variable Resistor

In the past, adjustments in electronic circuits were made by moving wipers on potentiometers, or moving cores of coils or transformers. In the factory, this type of adjustment was performed "by hand". The ANU-1 chassis uses the EVR ICs to replace the mechanical potentiometers that were used in previous models.

In Figure A, we see the schematic diagram for a voltage controlled amplifier. The gain of the amplifier can be altered by adjusting the variable resistor. Figure B shows the same circuit using an EVR IC to replace the potentiometer. The EVR IC is a type of D to A converter. A data word is loaded into a storage register inside the EVR IC. The state of the data stored in each register controls a switch loading a "1" into a particular register and will cause the associated switch to close. When one of the switches is closed, the resistor associated with it is bypassed. As more switches are closed, the DC voltage at the control output will decrease. For example, if the data word 1111 is loaded into the EVR IC in Figure B, all of the switches in the EVR IC will close, and Ov will be present at the control output. If the dataword 1110 is loaded into the EVR IC, the bottom switch will open, and the voltage will rise slightly.

In this way, the gain of the circuit can be controlled by a microprocessor or some other digital circuit. A computer can now be used during the manufacturing process to perform adjustments. Service adjustments are performed using the remote control hand unit (after the set has been placed in the service mode). One advantage to this system is that the adjustment position is numbered, so, an adjustment can be returned to exactly the original position if no improvement can be made.

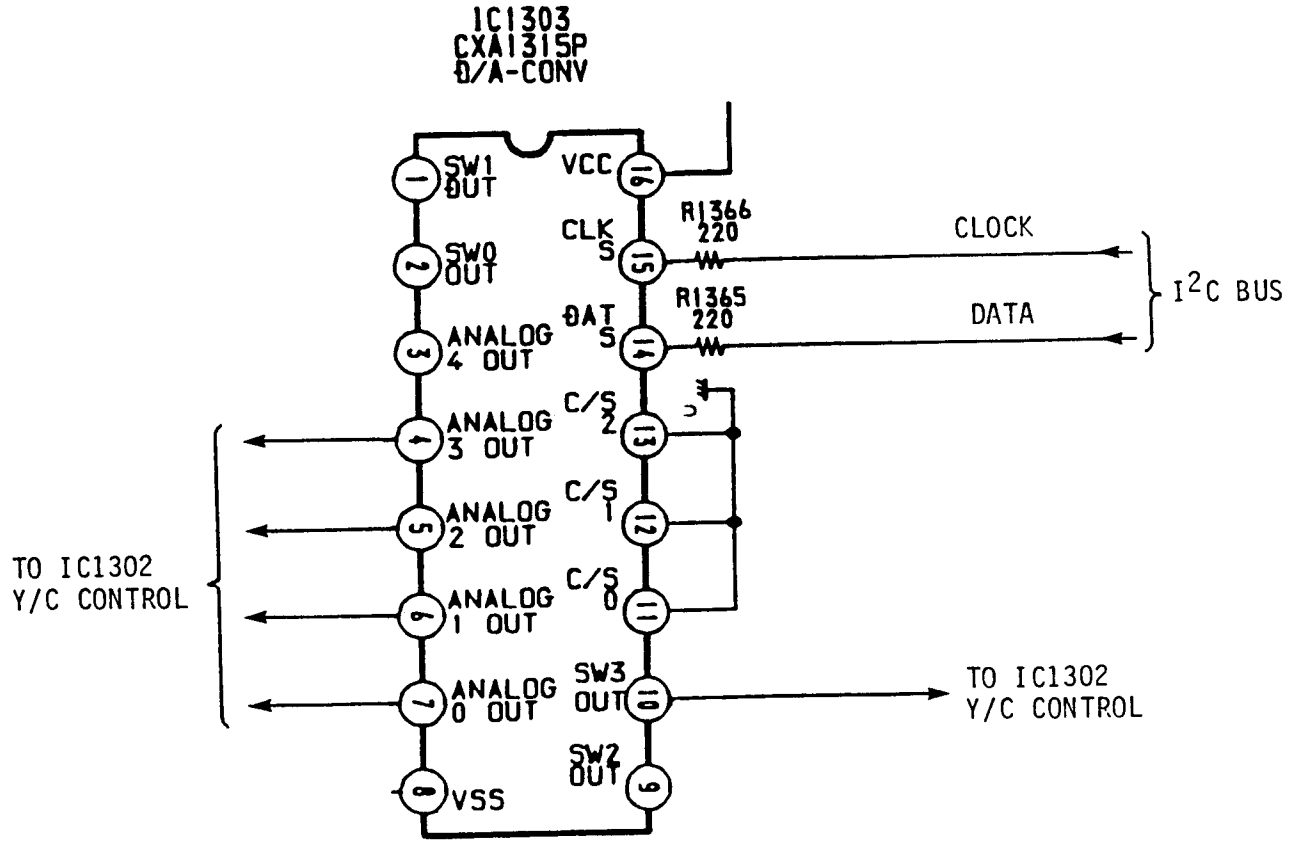
The customer receives the benefit of improved reliability since the EVR IC is not affected by dust or vibration. Of course, the actual EVR ICs used in the ANU-1 chassis are much more sophisticated than the example in Figure B.

## D to A Converter

Most of the D to A converters used in the ANU-1 chassis are housed inside of signal processing ICs. The exception to this is IC1303. IC1303 houses five D to A converters and four switches. All of the D to A converters and switches are controlled by the $I^2C$ bus. IC1303 is used to control the Y/C control circuit (IC1303). The Y/C control circuit performs aperture control and noise reduction for the video signal.

The D to A outputs are located at IC1303/pins-3 through 7 (pin-3 is not used in the ANU-1 chassis). The switch outputs are located at IC1303/pins-1, 2, 9, and 10 (only pin-10 is used in the ANU-1 chassis). Most of these adjustments are factory preset and should not require adjustment during servicing. The analog output at IC1303/pin-7 will change when the sharpness control is adjusted.

IC1303 has provisions for address selection at IC1303/pins-11 through 13. By pulling these pins up or down the IC can be made to respond to different addresses.



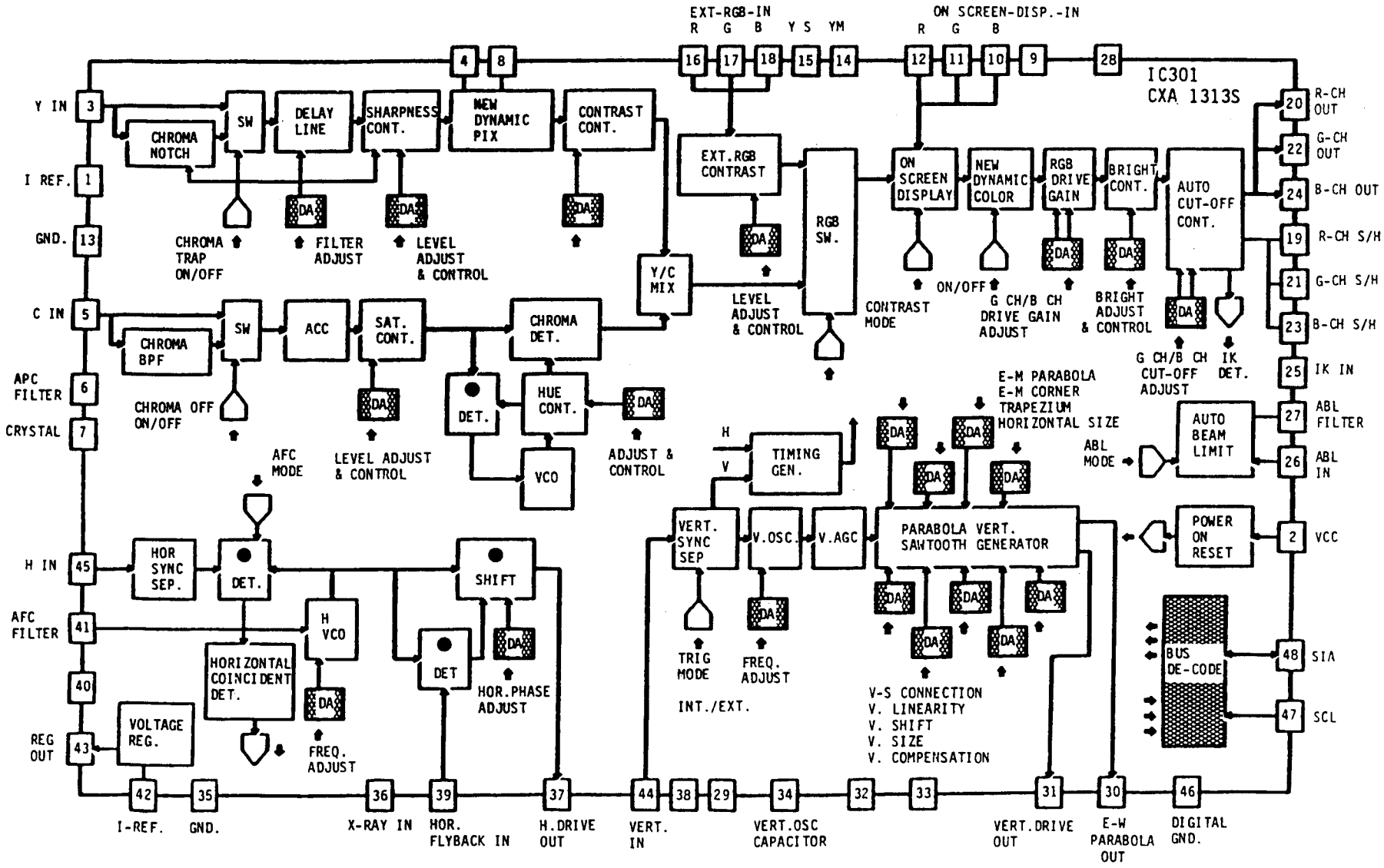

**D TO A CONVERTER**

# Video Processor

The ANU-1 chassis uses the new CXA1313S Y/C/jungle chip for video and scan processing. The most significant change from the previous Y/C/jungle (CXA1013AS) is the extensive use of internal D to A converters for adjustments. The CXA1313S contains 21 internal D to A converters. In addition to the D to A converters there are eight mode switches. All of these switches and D to A converters are controlled by the $I^2C$ bus.

In addition to the previously mentioned advantages, the EVR circuits also reduce the number of discrete components used to support the ICs. This is obvious when the RGB output section is examined. In previous models variable resistors were provided (on the C board) to control the cutoff and gain of the green and blue signals. In the ANU-1 chassis these components can be eliminated since these adjustments can be performed by CXA1313S internal circuitry. Other additional circuitry like the chroma notch filter, new dynamic color, and AFC mode switch can be added with no additional support circuitry required.

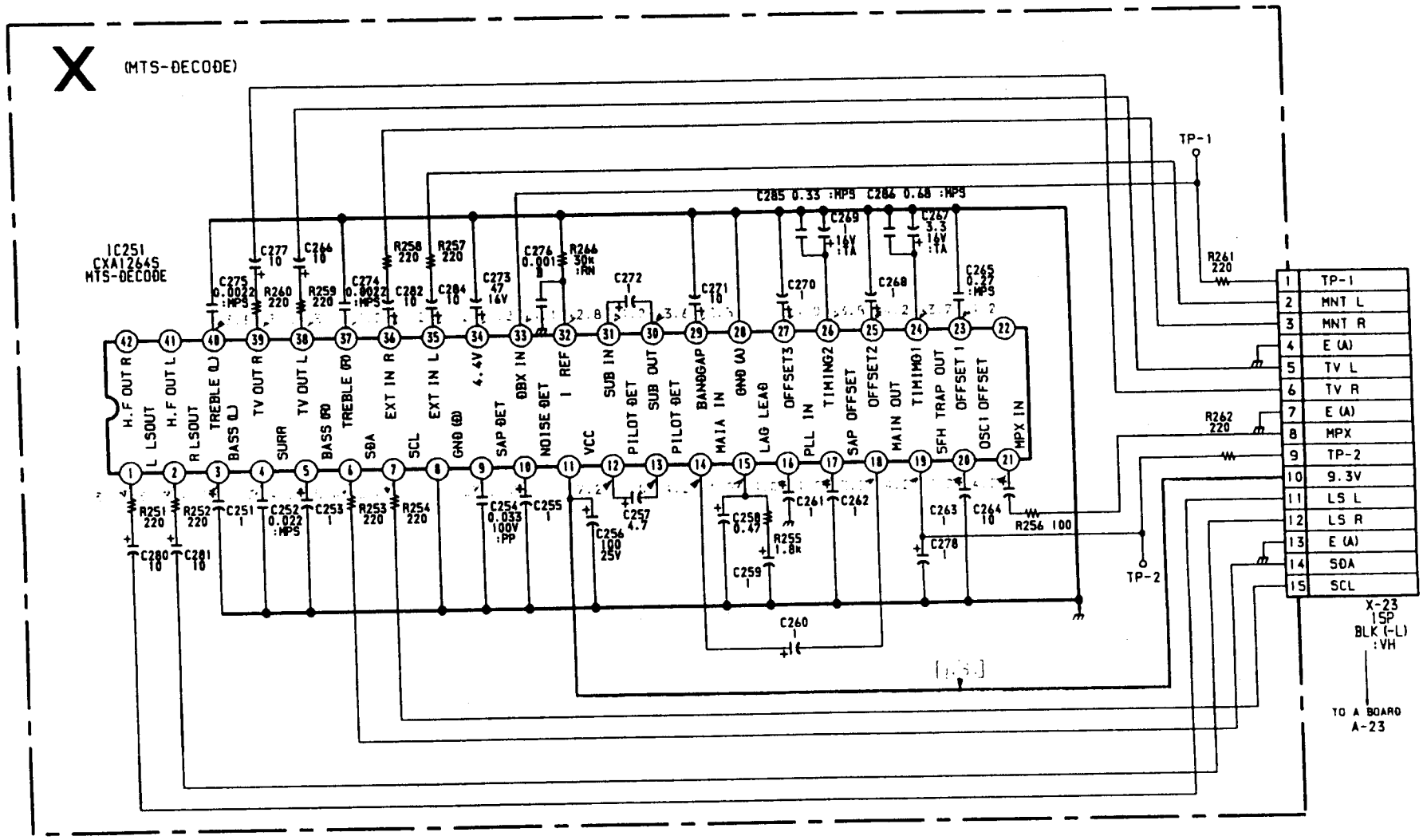
In the following sections of this book we will examine the individual processing operations separately.




**VIDEO PROCESSOR**

## MTS Decoder

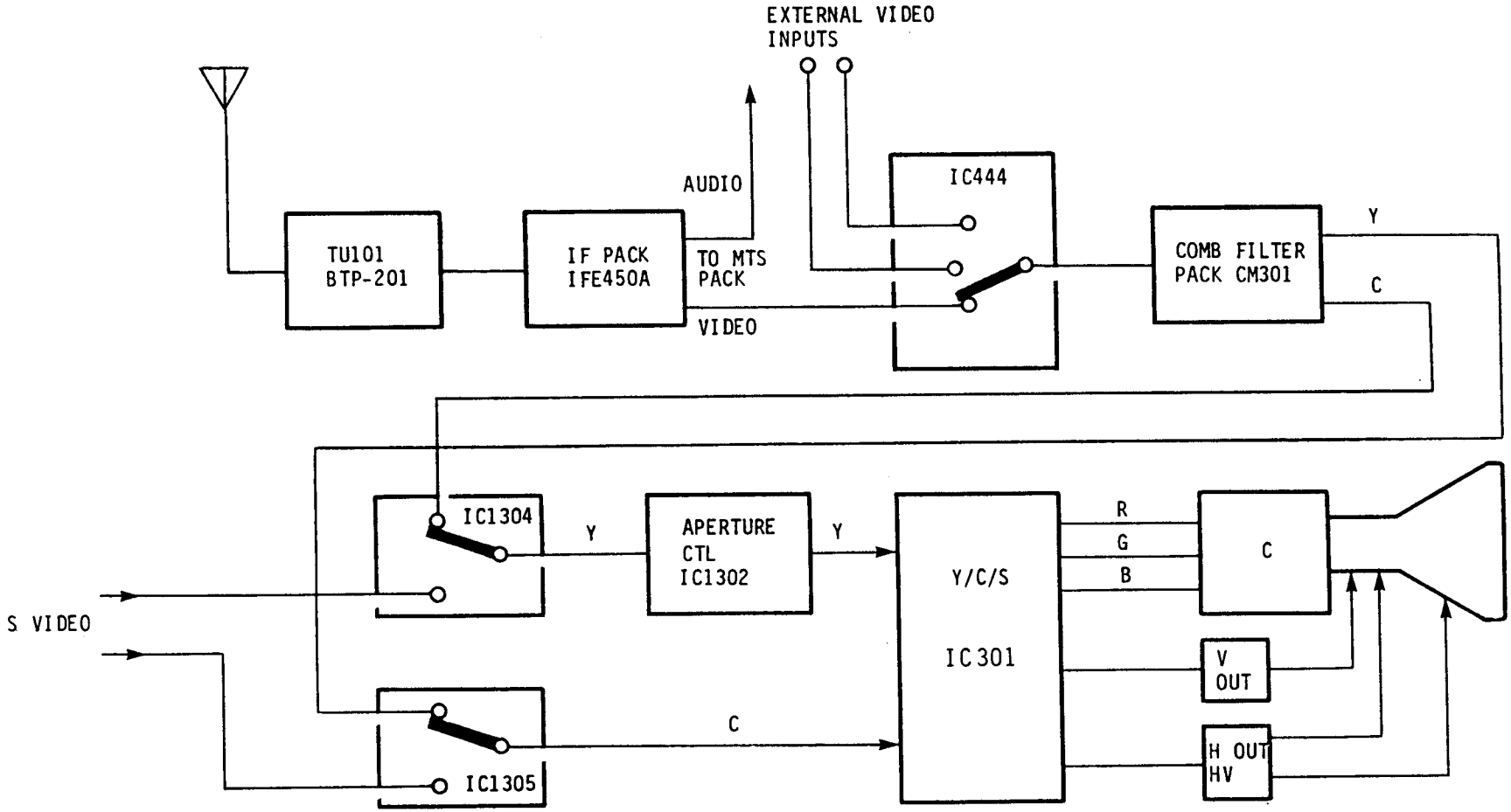
The MTS decoder used in the ANU-1 chassis is a replaceable pack which uses a CXA1264S decoder IC. The number of components in the MTS pack has been greatly reduced by the use of internal EVR circuitry. In addition to performing MTS decoding, IC251 switches between TV and external audio sources and controls signal gain for volume and balance control. All of these functions are controlled by the $I^2C$ bus.


X
(MTS-DECODE)
IC251
CXA1264S
MTS-DECODE
H.F OUT R
L LSOUT
H.F OUT L
R LSOUT
TREBLE (L)
BASS (L)
TV OUT R
SURR
TV OUT L
BASS (R)
TREBLE (R)
SDA
EXT IN R
SCL
EXT IN L
GND (D)
4.4V
SAP DET
OBX IN
NOISE DET
I REF
VCC
SUB IN
PILOT DET
SUB OUT
PILOT DET
BANDGAP
MAIA IN
GND (A)
LAG LEAD
OFFSET3
PLL IN
TIMING2
SAP OFFSET
OFFSET2
MAIN OUT
TIMING1
SFH TRAP OUT
OFFSET1
OSC1 OFFSET
MPX IN
C285 0.33 :MPS
C286 0.68 :MPS
TP-1
TP-2
R261 220
R262 220
R256 100
C278
TP-1
MNT L
MNT R
E (A)
TV L
TV R
E (A)
MPX
TP-2
9.3V
LS L
LS R
E (A)
SDA
SCL
X-23
15P
BLK (-L)
:VH
TO A BOARD
A-23

MTS DECODER

## Signal Process

The tuner and IF sections have not changed from the P3-A chassis to the ANU-1 chassis. Video and audio switching have changed slightly with the introduction of the CXA1114P (IC444) switching IC. The ANU-1 chassis introduces a new comb filter, using a CCD delay rather than a glass delay (XBR models). The two comb filters are physically interchangeable, however, due to performance differences they are not recommended as substitutes for each other. The Y and C outputs are then input to the Y and C video switches (IC1304/Y and IC1305/C). The Y signal is then input to the aperture control circuit IC1302. The Y signal from IC1302, and the C signal from IC1305 are input to the Y/C/jungle (IC301). IC301 then converts the Y and C signals to the R, G, B, H, and V signals.



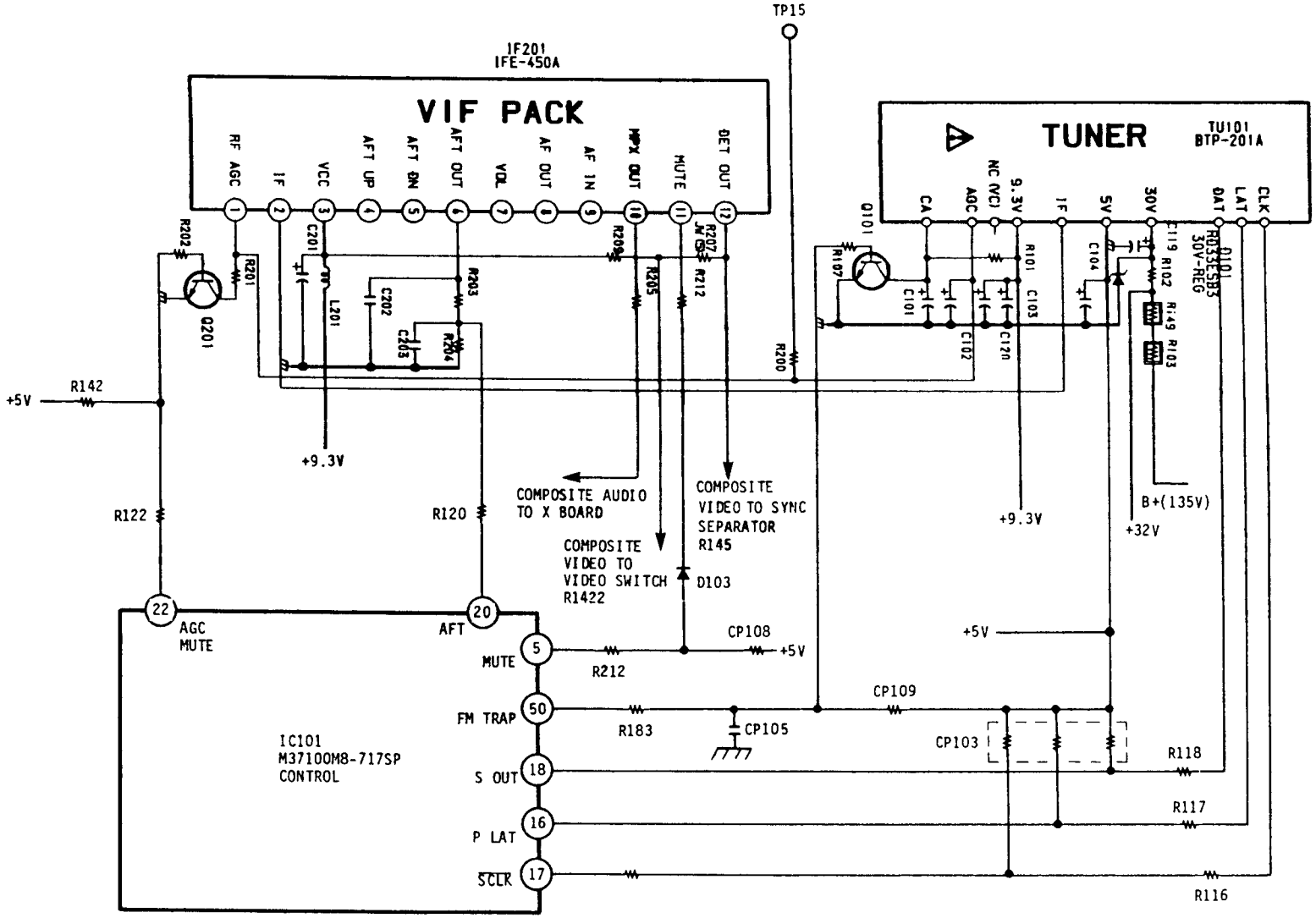

**SIGNAL PROCESS**

# Tuner Control

The tuner and IF sections of the ANU-1 chassis are very similar to those of the P3-A chassis. Data, clock, and latch signals from IC101/pins-18, 17, and 16 are input to the tuner (TU101). The tuner requires three independent supplies of 5V, 9.3V, and 30V. The CA input switches an internal FM trap when in the cable mode. This input is controlled by IC101/pin-50 and Q101. A DC control voltage from the IF is input to the AGC gain control input. During initial start up and channel change, IC101 takes control of the AGC input via the output at IC101/pin-22 and Q201. The tuner's output is coupled to the IF pack (IF201) at pin-2.

In addition to the main (IF) input at IF201/pin-2, the IF pack requires +9.3V power supply at IF201/pin-3. The only other input to IF201 used in the ANU-1 chassis is the mute input at IF201/pin-11. During initial turn on and channel change, IC101/pin-5 and IF201/pin-11 will go HIGH. This will mute the video and audio outputs of IF201.

The IF pack has four outputs. The composite video signal is output at IF201/pin-12. This signal is coupled to the sync separator and to the video switch. The composite audio signal from IF201/pin-10 is coupled to the MTS decoder. The RF AGC signal, as previously described, is coupled from IF201/pin-1 to the AGC input of TU101. The final output from IF201 is the AFT. The AFT output at IF201/pin-6 is a tri-state signal. When a station is properly tuned, the output at IF201/pin-6 will be 2.5V. If the local oscillator is slightly HIGH or LOW, IF201/pin-6 will go to +5V or 0v. The AFT signal from IF201/pin-6 is coupled through R203 and R120 to IC101/pin-20. IC101 will change the data to the tuner to correct the local oscillator's frequency.

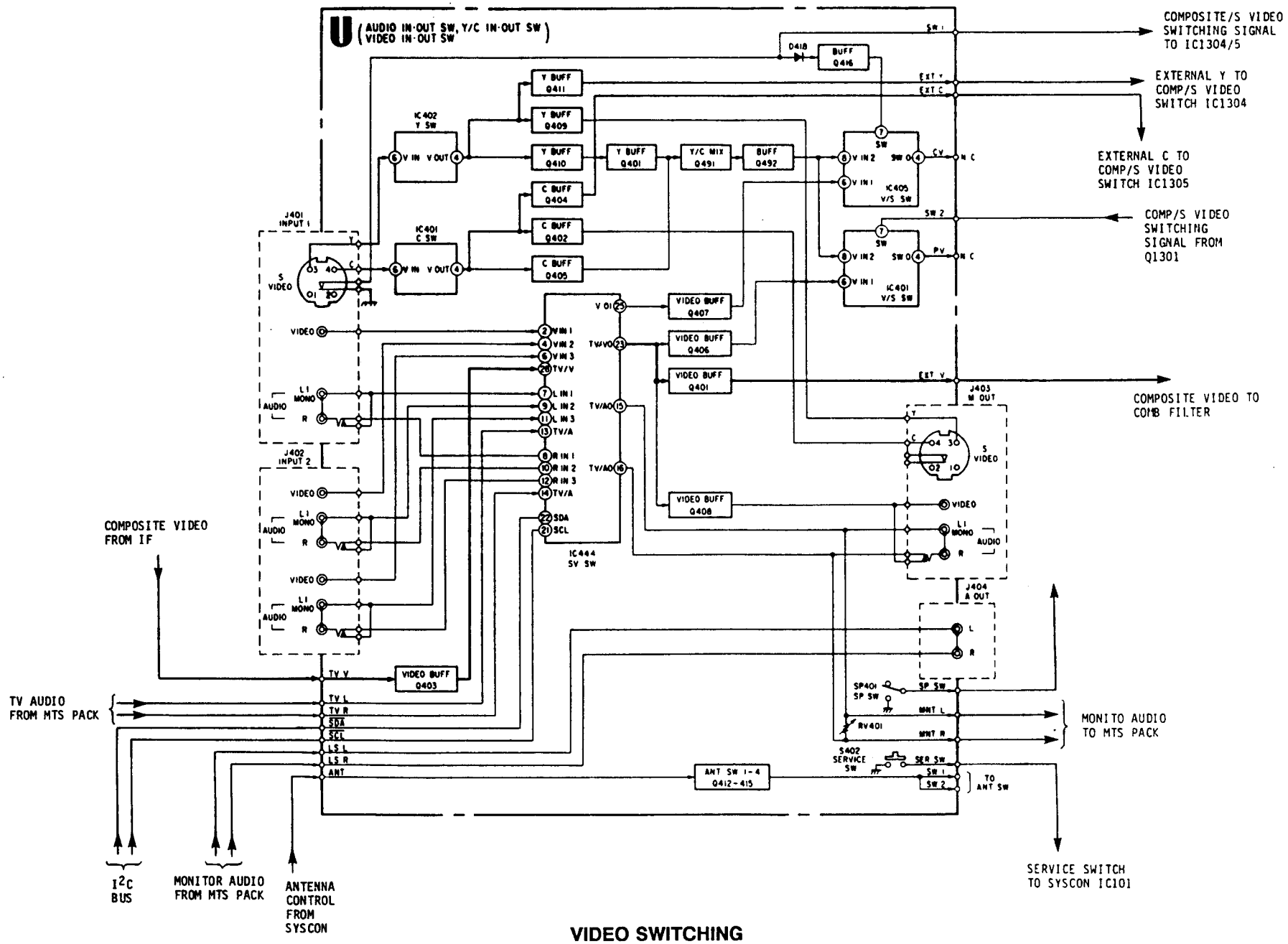



**TUNER CONTROL**

## Video Switching

The U board contains the video and audio switching circuitry, audio and video output and input connectors, service switch and speaker switch. IC401 and IC405 the S video switches are not used in the single S video input versions of the ANU-1 chassis. The U board is mounted vertically at the rear of the set. The U board is connected to the B board by flexible connectors so that it can be folded down for easy service. Since the operation of IC444 has been previously described, we will examine only the S video circuitry on the U board.

In addition to the composite video input for video 1, a separate S video connector is provided for use with ED Beta or Super VHS. Signal switching for the S video signal is performed on the B board. When an S video connector is inserted into the S video connector in J401, the switch inside of the S video connector will close, and the SW1 signal will go LOW. The Y signal from the S video connector pin-3 is coupled through IC402/pin-6 and pin-4 to the Y buffers Q411 and Q409. The buffered Y signal from Q411 is coupled to the S video switch (on the B board). The buffered Y signal from Q409 is coupled to the S video monitor output connector J403. The C signal from the S video connector pin-4 is coupled to the C buffers Q402 and Q404. The buffered C signal from Q404 is coupled to the S video switch (on the B board). The buffered C signal from Q402 is coupled to the S video monitor output connector J403.

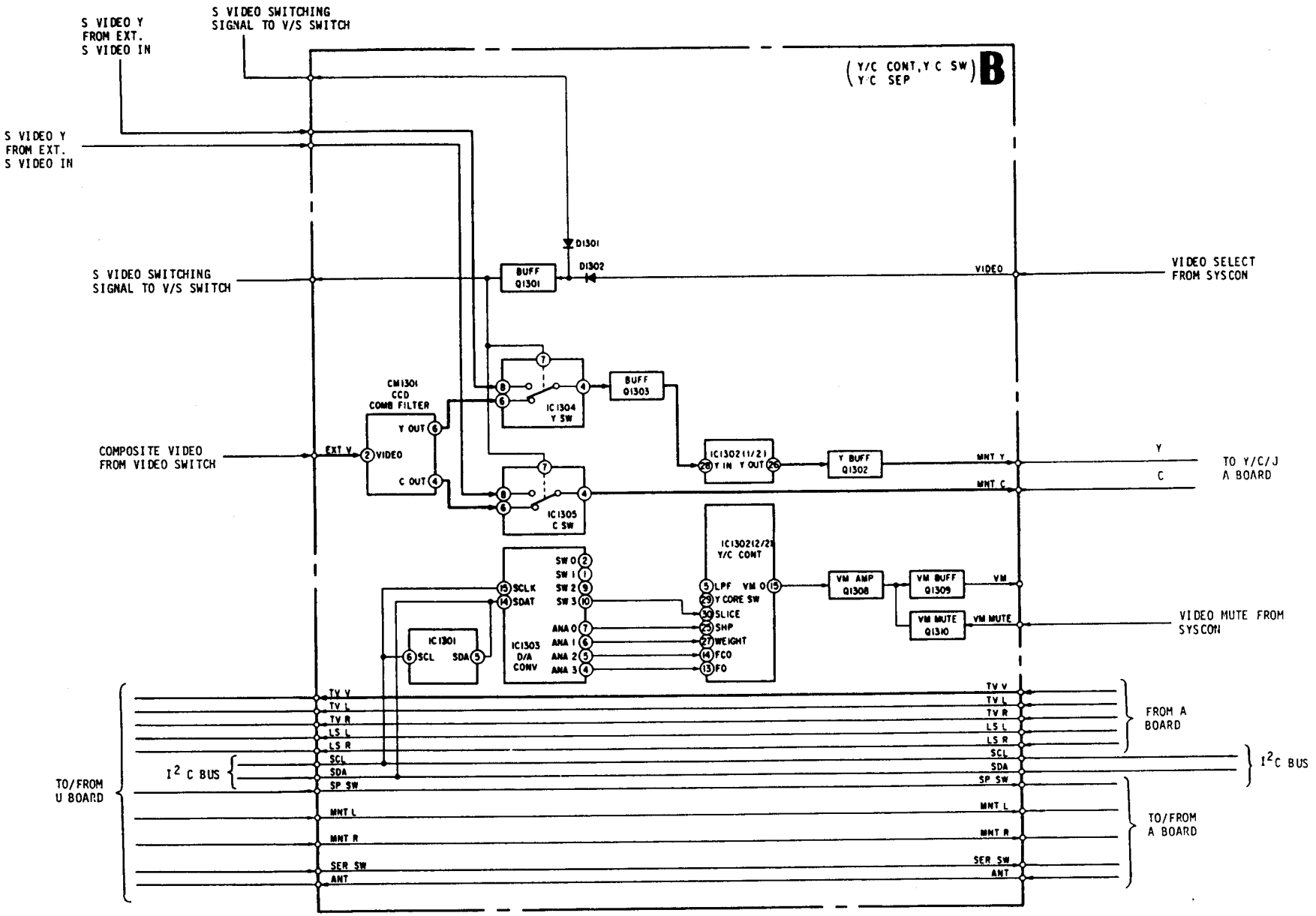



**VIDEO SWITCHING**

## B Board

The major components on the B board are the comb filter (CM1301), the Y and C switches (IC1304 and IC1305), the non-volatile memory (IC1301), the D to A converter (IC1303), and the Y/C control circuit (IC1302). Since the operation of IC1301, and IC1303 have been previously discussed, our examination of the B board circuitry will revolve around IC1302, CM1301, IC1304, and IC1305. IC1305 and IC1306 switch between the comb filter's outputs and the S video signals. The chroma signal from IC1305 is coupled directly to the A board and the Y/C/jungle circuit. The Y signal from IC304 is coupled to the YC control circuit IC1302. The enhanced Y signal from the Y/C control circuit is buffered by Q1302 and coupled to the Y/C/jungle circuit on the A board.

In the following section we will examine the comb filter and Y/C switches, and then move on to the Y/C control circuit.


S VIDEO Y FROM EXT. S VIDEO IN
S VIDEO SWITCHING SIGNAL TO V/S SWITCH
(Y/C CONT, Y C SW / Y C SEP) B
S VIDEO Y FROM EXT. S VIDEO IN
S VIDEO SWITCHING SIGNAL TO V/S SWITCH
D1301
D1302
BUFF Q1301
VIDEO
VIDEO SELECT FROM SYSCON
CM1301 CCD COMB FILTER
Y OUT
C OUT
EXT V
VIDEO
COMPOSITE VIDEO FROM VIDEO SWITCH
IC1304 Y SW
IC1305 C SW
BUFF Q1303
IC1302(1/2) Y IN Y OUT
Y BUFF Q1302
MNT Y
MNT C
Y
C
TO Y/C/J A BOARD
IC1302(2/2) Y/C CONT
LPF
Y CORE SW
SLICE
SHP
WEIGHT
FCO
FO
VM 0
VM AMP Q1308
VM BUFF Q1309
VM
VM MUTE Q1310
VM MUTE
VIDEO MUTE FROM SYSCON
IC1303 D/A CONV
SW 0
SW 1
SW 2
SW 3
ANA 0
ANA 1
ANA 2
ANA 3
SCLK
SDAT
IC1301
SCL
SDA
TV V
TV L
TV R
LS L
LS R
SCL
SDA
SP SW
MNT L
MNT R
SER SW
ANT
I2C BUS
TO/FROM U BOARD
FROM A BOARD
I2C BUS
TO/FROM A BOARD

**B BOARD**

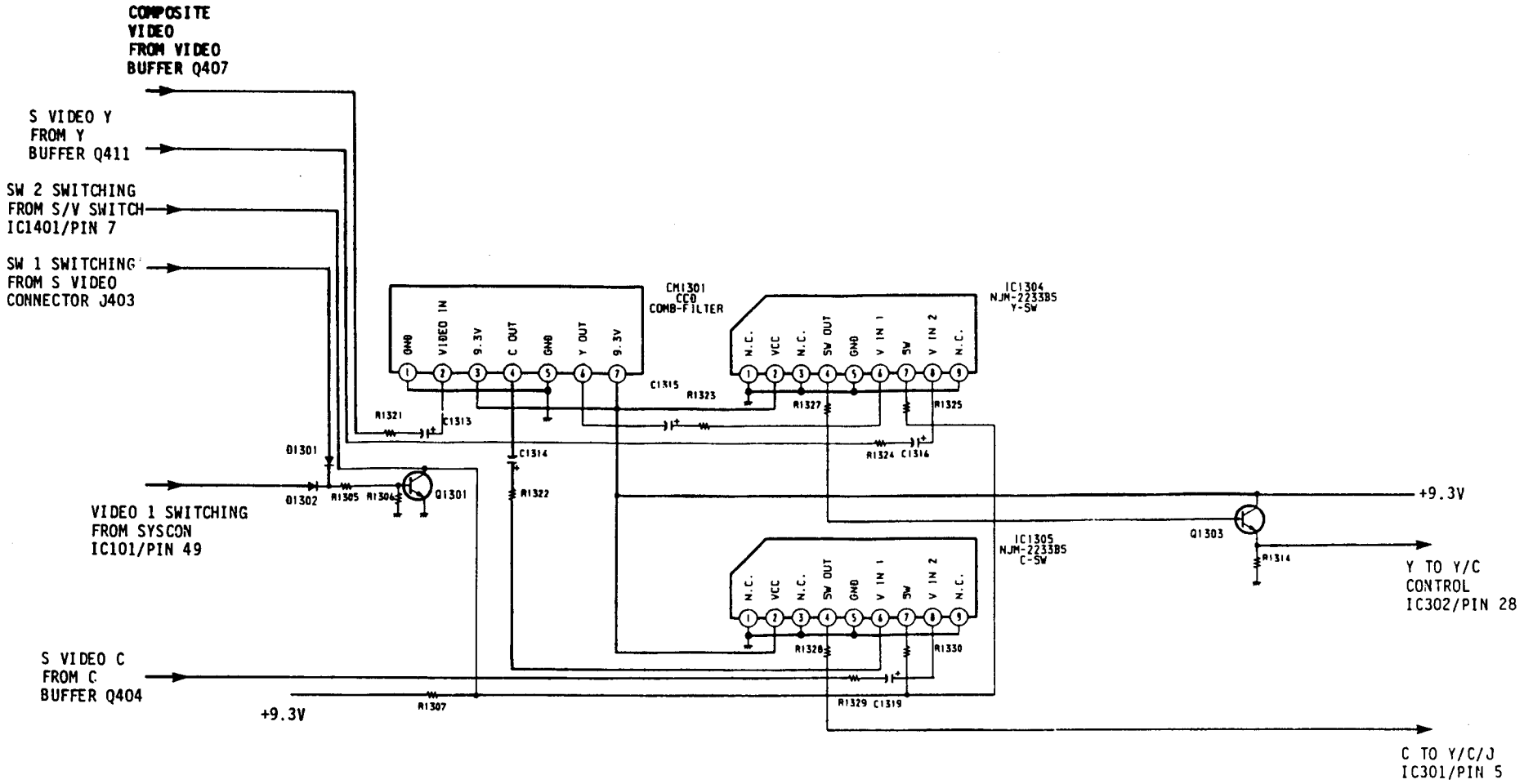
## Comb Filter/S Video Switch

Composite video from the U board is coupled to CM1301/pin-2. The comb filter separates the Y and C signals and outputs the Y signal at CM1301/pin-6 and the C signal at CM1301/pin-4. The comb filter requires +9.3V power supply at pin-3 and pin-7, and ground at pin-1 and pin-5.

IC1304 and IC1305 switch the Y and C signals between the video 1/S video signals and the comb filter's Y and C outputs.

Since the operation of IC1304 and IC1305 are exactly the same, only IC1304 will be described here. The comb filter Y signal is coupled to IC1304/pin-6 and the video 1/S video Y signal is coupled to IC1304/pin-8. When IC1304/pin-7 is LOW, the comb filter Y signal at IC1304/pin-6 will be coupled through IC1304 to the switched output at IC1304/pin-4. When IC1304/pin-7 goes HIGH, the S video Y signal from IC1304/pin-8 will be coupled to the switched output at IC1304/pin-4.

In the TV, video 2, and video 3 modes, IC101/pin-49 is HIGH. In this condition, D1302 is forward biased and current will flow through D1302 and R1305 to the base of Q1301. This will turn Q1301 on, and Q1301's collector and IC1304/pin-7 will be LOW. If no S video connector is plugged into the video 1 input connector J403 the SW1 switching signal will be HIGH. In this condition D1301 will be forward biased. When the unit is switched to video 1 mode, IC101/pin-49 will go LOW. In this condition, D1301 will be forward biased and current will flow through D1301 and R1305 to the base of Q1301. When an S video plug is inserted into J403, the SW1 signal will go LOW. If the video 1 mode is selected, IC101/pin-49 will also go LOW. In this condition D1301 and D1302 will not be forward biased, and Q1301 will turn OFF. The collector of Q1301 and IC1304/pin-7 will now go HIGH. The SW2 switching signal is used only in modes containing multiple S video inputs.



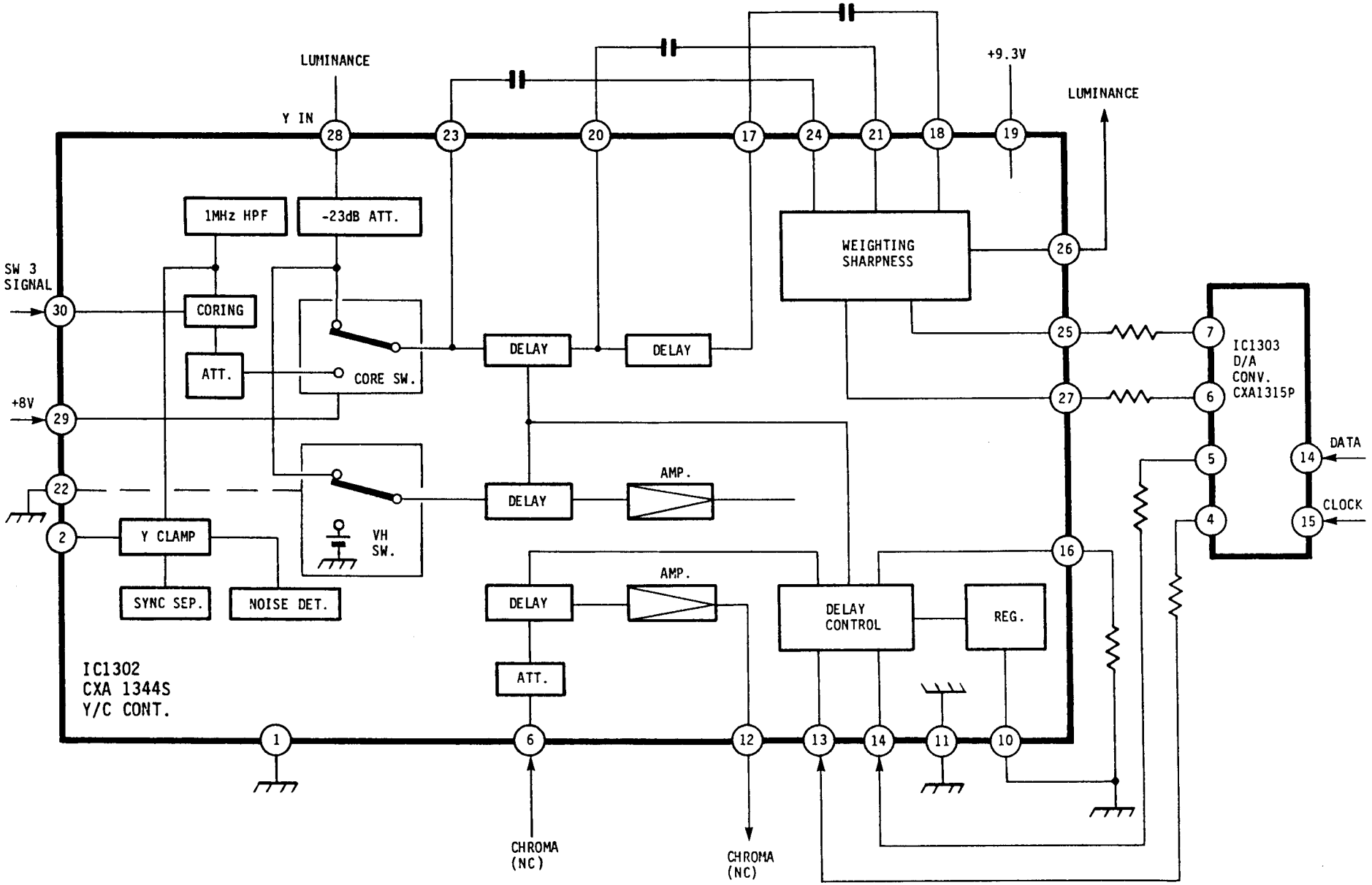

**COMB FILTER/S VIDEO SWITCH**

## Y/C Control Block

The Y/C control circuit is very similar to the aperture circuit found in single imager color video cameras. Its main purpose is to decrease the transition time of the luminance signal when the signal changes between light and dark. By decreasing the transition time of the luminance signal, edges become sharper.

The Y signal is input to IC1302/pin-28, passes through the -23db amp and the core switch to a delay and the weighting/sharpness amp. The output of the delay is input to the weighting/sharpness and another delay. The second delay's output is also input to the weighting/sharpness amp. The weighting/sharpness amp compares to the undelayed Y signal, the once delayed Y signal and the twice delayed signal, and develops an "edge signal". This signal consists of sharp "spikes" which occur wherever there is a transition in the luminance signal. The spikes have a very short transition time. The spike signal is added to the luminance signal. This results in a luminance signal with very short transition times and large spikes at each transition. The spikes are then removed by white clip and dark clip circuits.

There are four adjustments associated with the Y/C control circuit. Three are factory preset and cannot be adjusted. The fourth is the customer's sharpness control. As the customer changes the sharpness adjustment setting, the DC level at IC1303/pin-7 and IC1302/pin-25 will change. This will alter the amount of the edge signal being added to the luminance signal. The SW-3 input at IC1302/pin-3 is controlled by a switch output at IC1303/pin-10. Normally this signal remains LOW.

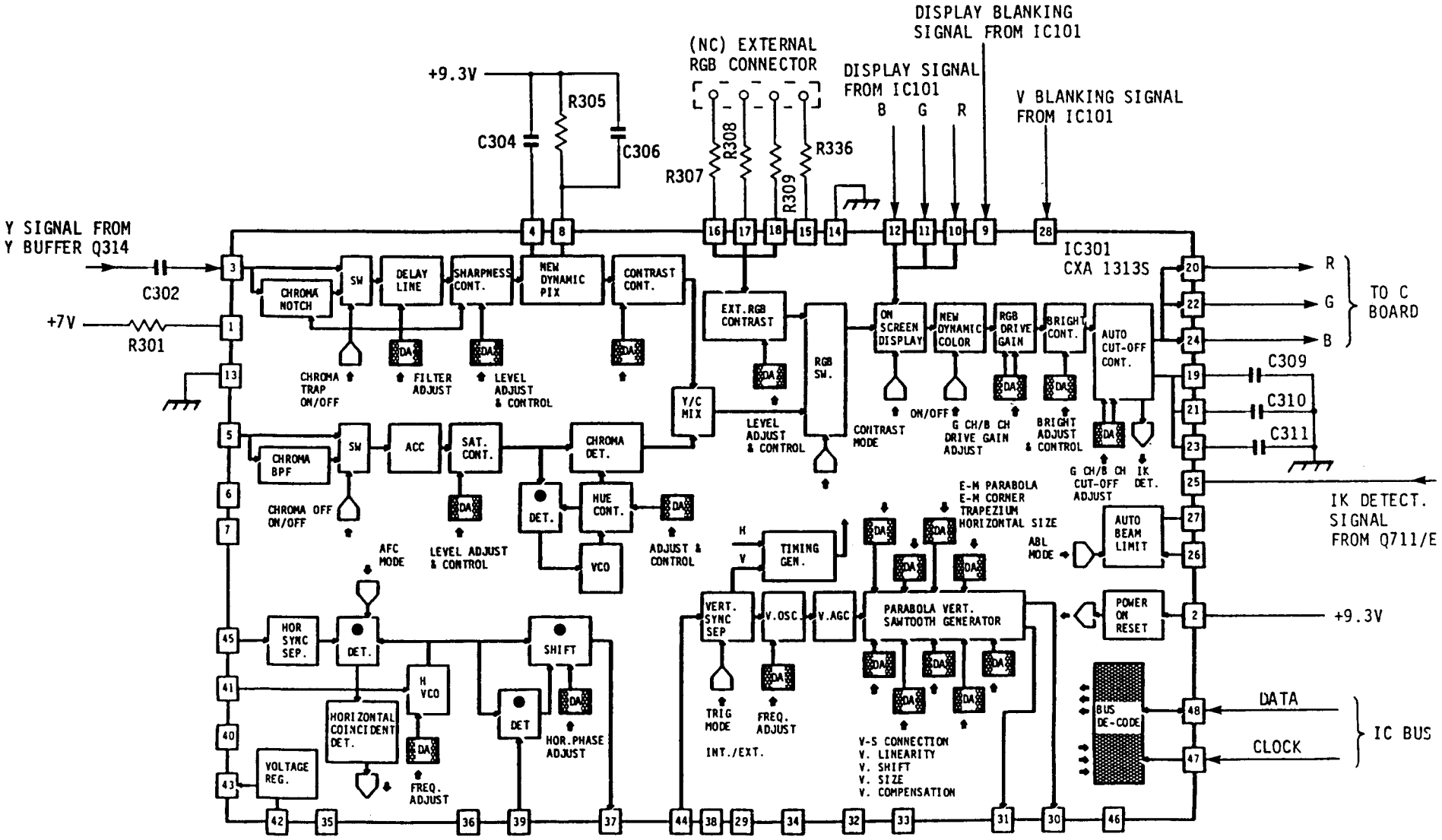



**Y/C CONTROL BLOCK**

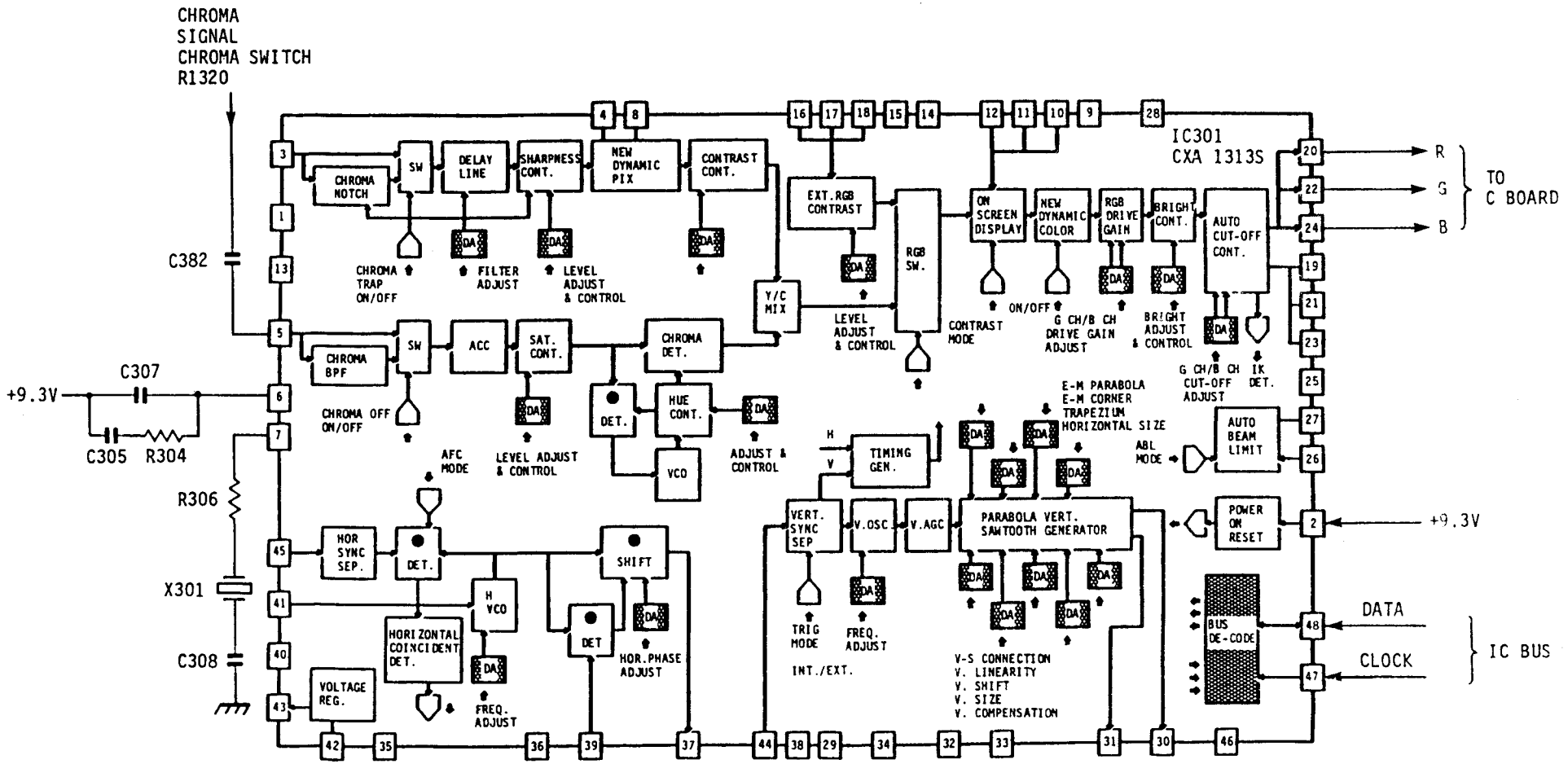
## Luminance Process

All luminance processing, other than that performed by IC1302, is performed by IC301. All luminance and RGB adjustments are performed inside of IC301 by D to A converters which are controlled by the $I^2C$ bus. The bus inputs are located at IC301/pin-48 (data) and pin-47 (clock).

The luminance signal is input to IC301/pin-3. The signal is input to both the chroma notch filter and the notch filter bypass switch. The notch filter switch is controlled by the $I^2C$ bus. The luminance signal then passes through the delay and sharpness control circuits to the new dynamic pix circuit. The output of the dynamic pix circuit passes through the contrast control circuit to the Y/C mix circuit. The chroma and luminance signals are mixed and the RGB signals are "decoded" in the Y/C mixer. The RGB signals are then passed through the external RGB switch (not used in this model) to the on-screen display circuit. The on-screen display mix circuit will superimpose the display characters on the normal RGB signals. The RGB signals from the on-screen display circuit pass through the new dynamic color, RGB gain control, brightness control, and auto cut-off control circuits, and are output at IC301/pin-20 (R), pin-22 (G), and pin-24 (B). These signals are then coupled to the C board. Since the RGB drive and cut-off adjustments are performed inside of IC301, these controls have been deleted from the C board. The IK detect signal at IC301/pin-25 is used by the auto cut-off circuit to detect the current in the RGB drivers (on the C board).



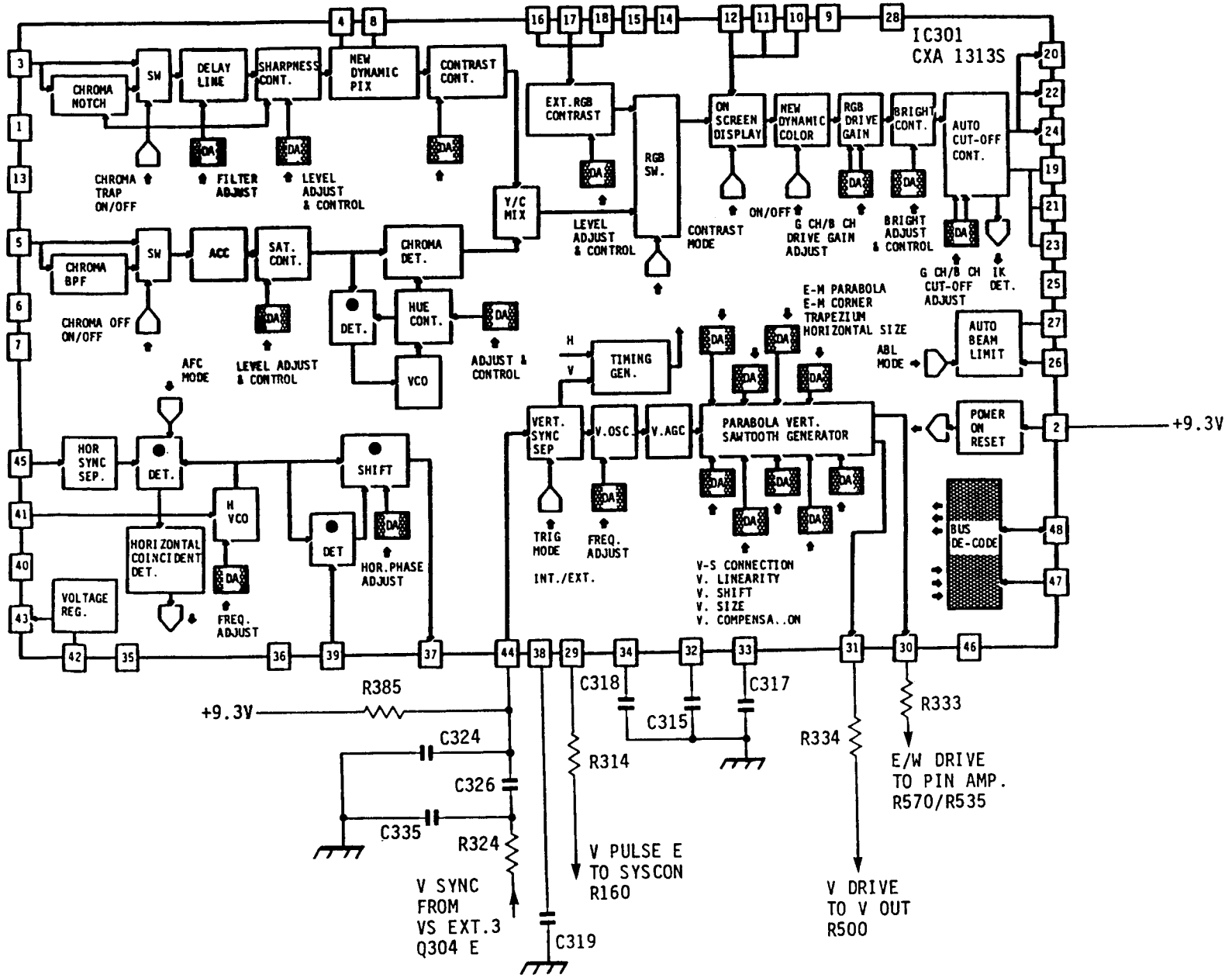

**LUMINANCE PROCESS**




**CHROMA PROCESS**

## Chroma Process

All chroma processing and color adjustments are performed inside of IC301. The chroma signal is input to IC301/pin-5 and coupled to both the chroma band pass filter and the chroma BPF bypass switch. The chroma BPF bypass switch is controlled by the $I^2C$ bus. The chroma signal from the chroma BPF bypass switch passes through the automatic color control and saturation detector circuits and is coupled to both the burst and chroma detectors. The burst detector, VCO, and HUE control circuits support the chroma detector. The chroma detector removes the 3.58MHz carrier from the chroma signal and outputs the color signal to Y/C mixer where the RGB signals are developed and processed as described in the luminance process section of this book.

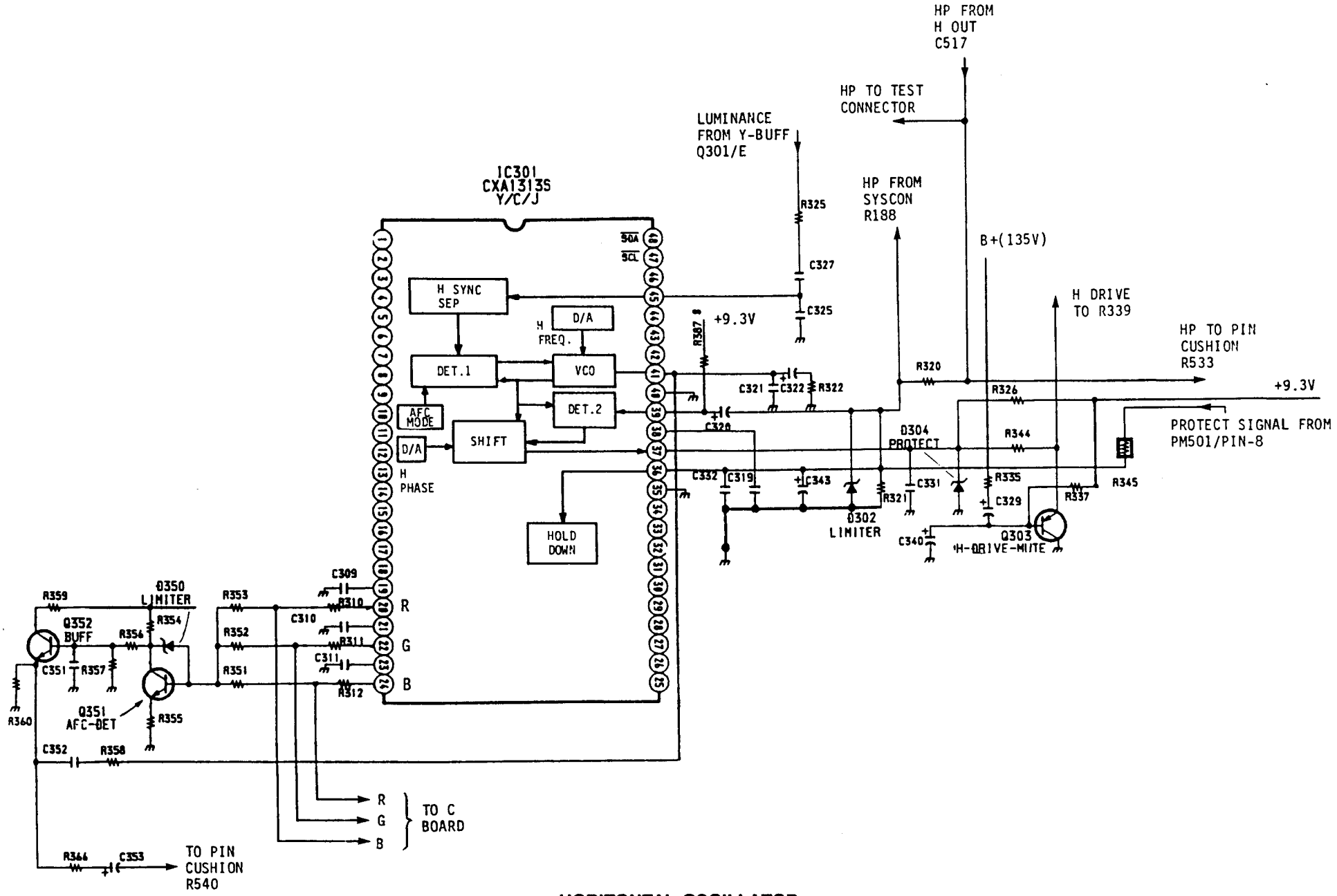



**VERTICAL OSCILLATOR**

## Vertical Oscillator

Like the chroma and luminance processing circuits, most of the vertical deflection process circuits are contained inside of IC301. Since the vertical output circuit is essentially the same as previous models, it will not be discussed in this book (see CTV-15 for similar circuit).

The luminance signal from the emitter of Q304 is coupled to IC301/pin-44 through the V BPF circuit consisting of R324, C324, C335, and R385. From IC301/pin-44 the luminance signal is coupled to the internal sync separator circuit. The vertical pulses output from the vertical sync separator are coupled to the timing generator (for internal timing) and to the vertical oscillator. The V pulses input to the vertical oscillator are used to synchronize the oscillator to the luminance signal. The synchronized output from the vertical oscillator passes through the vertical AGC circuit and is input to the vertical sawtooth/parabola generator. The sawtooth/parabola generator has two outputs. The sawtooth signal from IC301/pin-31 is coupled to the vertical output circuit. The parabola signal from IC301/pin-30 is coupled to the pincushion amp.




**HORIZONTAL OSCILLATOR**

## Horizontal Oscillator

The horizontal oscillator and hold down circuits are the final circuits inside of IC301 to be examined. Special attention should be paid to the AFC mode switch. The AFC circuit can be switched OFF for H frequency adjustment. With the AFC circuit OFF, the horizontal oscillator can be adjusted to a wide range of frequencies. If the H frequency is adjusted to HIGH, the HIGH voltage will rise above a safe level and then hold down circuitry will activate, and the set will shut down. Under normal circumstances this should not pose a problem, however, care should be taken when adjusting the horizontal frequency.

The luminance signal from the emitter of Q301 is coupled through the filter consisting of R325, C327, and C325 to IC301/pin-45. The signal at IC301/pin-45 is coupled to the H sync separator inside of IC301. The horizontal pulses output from the H sync separator are coupled to the detector 1 circuit. The detector 1 circuit is a switchable horizontal AFC circuit. This circuit has four states of operation. They are: wide AFC range, medium AFC range, narrow AFC range, and AFC OFF. In the "AFC OFF" mode (3) the VCO (H OSC) free runs. For normal operation the detector 1 circuit is kept in the mid-AFC range (0).

The output of detector 1 is used to lock the VCO to the video signal.

The VCO output is coupled through the (phase) shift circuit and output at IC301/pin-37. This signal (H drive) is coupled through R334 to the horizontal output section. The horizontal output and hold down circuitry in the ANU-1 chassis is essentially the same as previous models and is not discussed in this book (see CTV-15).

Horizontal pulses from the horizontal output circuit are coupled through R320 and input to IC301/pin-39. These pulses are compared to the VCO output by detector 2 to assure that the entire horizontal system is phase locked. The horizontal pulse from the horizontal output circuit are also coupled to the pincushion, and system control (for character sync) circuits.

To insure stability in the VCO, a filter network consisting of C321, C322, and R322 is provided at IC301/pin-41. This filter network is also coupled to the AFC detector consisting of Q351, Q352, and the associated components. During changes in brightness, pulses from the AFC detector will be coupled through C352 and R358 to IC301/pin-41. These pulses help to stabilize the H OSC during changes in loading due to changes in the brightness level.

Q303 and the associated components are the H drive mute circuitry. They provide a delay to prevent the horizontal output circuitry from operating until the B+ power supply becomes stable. When power is first turned ON, the charging of C340 will turn Q303 ON. When C340 becomes fully charged, the base of Q303 has no bias and Q303 will turn OFF.

High voltage hold down is controlled by IC301/pin-36. Normally this pin is LOW (0V) and the horizontal oscillator operates normally. If the high voltage supply voltage becomes excessive, PM501/pin-8 and IC301/pin-36 will go HIGH. The hold down circuitry inside of IC301 will then stop the horizontal oscillator from oscillating. Since PM501's operation is the same as the protection module used in previous models, HS operation is not discussed in this book (see CTV-15).