

# HIGH CMRR, SECOND GENERATION CURRENT-MODE INSTRUMENTATION AMPLIFIERS

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**Abstract**-Common-mode bootstrapping techniques have been used to produce high CMRR second generation current-mode instrumentation amplifiers. Simulation results, which take component mismatch into account show CMRR performance better than 70dBs at 100kHz for unity differential gain.

## 1. INTRODUCTION AND BACKGROUND

Many application areas, particularly those encountered by the authors in medical instrumentation design, require wide bandwidth instrumentation amplifiers, with low differential gain and high CMRR. The current-mode instrumentation amplifier circuit previously reported by Toumazou and Lidgey [1], is shown in Fig.1, and this was chosen as the basis for the development of new instrumentation amplifiers.

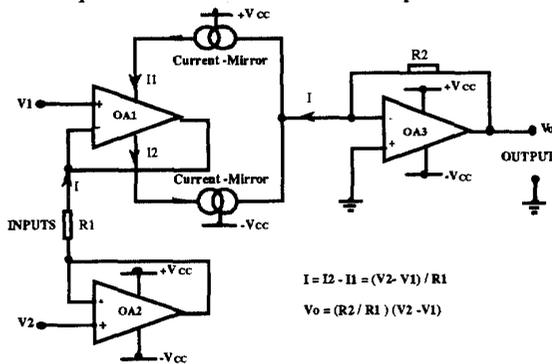


Fig.1 First Generation Current-mode IA

In this first generation instrumentation amplifier (IA), design, common-mode signals are principally rejected by the differential input voltage controlled current source (DVCCS) comprising op-amps OA1 and OA2. This is because the current through R1 is essentially zero if  $V1 = V2$ , as both op-amps are configured as voltage-followers. Also, the symmetry of this DVCCS stage indicates that the common-mode rejection will be good at high frequencies, as was successfully demonstrated in [1]. Presented with a target specification requiring a high CMRR instrumentation amplifier with unity differential gain operating up to 50kHz, the authors have developed modified and improved versions of the Fig.1 circuit.

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## 2. CIRCUIT OPERATION AND FURTHER DEVELOPMENT

If the performance of the two voltage-follower configured op-amps, OA1 and OA2, are not identical, then a common-mode input signal to the circuit of Fig.1 will result in current flow through R1, and hence an output in response to that common-mode input. However, even if the matching between OA1 and OA2 is perfect, a common-mode input will result in a very low level of supply current modulation. A perfect match between OA1 and OA2 can be simulated by removing R1 from the circuit. Under these conditions, applying a signal at V1, effectively a common-mode input since R1 is infinite, results in supply currents I1 and I2 varying with signal. Provided FET input op-amps are used for OA1 and OA2, so that the input current levels are very low, then  $I1 = I2$  and  $\Delta I1 = \Delta I2 = \Delta I$  but  $\Delta I \neq 0$ . Further investigation of the magnitude of  $\Delta I$  resulting from a common-mode input reveals that, as might be expected, the current modulation,  $\Delta I$ , is greatly reduced if the power supply voltage of OA1 is held constant.

An improved current-mode instrumentation amplifier, which has the same basic topology as Fig.1, was developed by Zhu et al [2] and is shown in Fig.2. The CMRR performance of this circuit is significantly better than that reported earlier in [1], mainly because supply voltage modulation of OA1 has been reduced substantially.

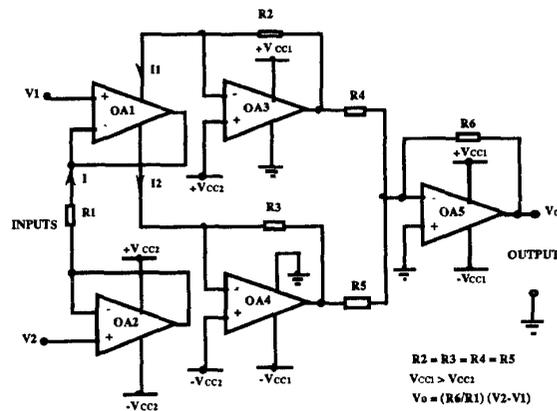


Fig.2 An improved current-mode IA

Power supply sensing of OA1 is achieved with OA3 and OA4 configured as VCCS stages. The non-inverting inputs of these two op-amps are tied to +VCC2 and -VCC2,

ensuring that the voltage supplies to OA1 are fixed. Output voltage summing from OA3 and OA4 is achieved using a conventional voltage summer, comprising OA5, R4, R5 and R6. The resistors R2 and R3 must be well matched, as must R4 and R5 to ensure that any common-mode output from the DVCCS stage is effectively nulled. Reporting preliminary work on this second generation current-mode instrumentation amplifier, Zhu et al [2] have achieved experimental CMRR performance of better some 60dB up to 200kHz using selected LF351 op-amps with closely matched frequency responses. The performance of this circuit showed a significant improvement over the first generation design. However, further improvements in CMRR performance was considered both desirable in application and possible using the same basic IA topology.

### 3. SECOND GENERATION CURRENT-MODE IA WITH COMMON-MODE BOOTSTRAPPING

Following this work, it was considered that the CMRR performance could be improved further if the input stage op-amp power supply voltages were made to track the common-mode input signal. To achieve this, additional circuitry, as shown in Fig.3, is used to bootstrap the power supply connections of OA1 to the common-mode input voltage.

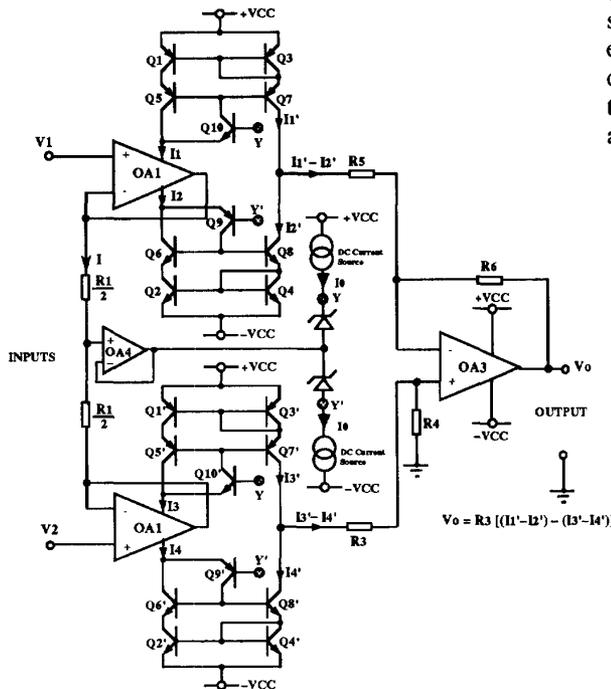


Fig.3 Second generation current-mode IA

The power supply currents of the front-end op-amps, OA1 and OA2, are now provided via four current-conveyors, CCII+s, which are based on the modified Wilson current-mirror. Referring specifically to the positive power supply connection to OA1, the CCII+ comprises Q1, Q3, Q5, Q7, and Q10. Transistor Q10 has replaced the original direct connection between the base and collector of Q5 in the modified-Wilson current-mirror, with the base of Q10 acting as the high input impedance Y-node of the CCII+.

Resistor R1 is divided into two equal values and the mid-point voltage between these resistors is connected to the input of a voltage-follower, OA4. The output of OA4 is connected to the point between the two zener diodes, which together with the two constant current sources provide a DC level-shift to the input common-mode signal. The Y and Y'-nodes are linked to the input of the current-conveyors.

With this arrangement, any common-mode voltage will be followed by OA4 and fed to the centre point between the two zeners. Effectively, the power supplies for OA1 and OA2 will then follow the common-mode voltage and hence reduce the common-mode output current. In addition, the original single-ended output from the input stage has been change into a dual output which feeds into a differential-amplifier comprising OA3 and associated resistors. It would seem that the full symmetry of the new design will provide additional common-mode rejection via the output differential amplifier stage. However, though there is potentially additional CMRR enhancement, whether this is achievable in practice will depend critically on the relative matching of the two halves of the circuit around OA1 and OA2, in particular Q9, Q10, Q9' and Q10'.

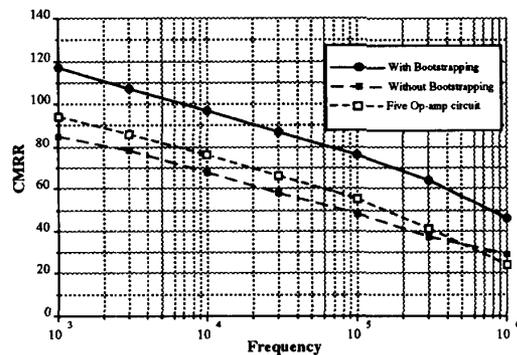


Fig.4 Simulation results of CMRR

#### 4. SIMULATION ANALYSIS AND RESULTS

To demonstrate the characteristics of the new circuit design and compare the performance with different circuit topologies, PSPICE simulation has been carried out, using a 741 op-amp transistor-level model. Firstly, the evaluation focussed on the validity of the technique used to increase the input stage common-mode transconductance rejection. A sinusoidal common-mode voltage with an amplitude of 2V at 10kHz was applied to both of the inputs V1 and V2.

Initially all the devices were set with perfectly matched parameters. The supply current of OA1,  $I_1$ , was probed and when the bootstrap nodes (Y & Y') of Q9, Q10, Q9' and Q10' were connected directly to  $\pm V_{cc}$  the current  $I_1 \approx 17.66 \times 10^{-3} \sin(2\pi ft) \text{ mA} + 1.11 \text{ mA}$ . However, when the OA1 and OA2 power supply connections were bootstrapped to the common-mode input, namely the Y and Y'-nodes linked directly, then the current  $I_1 \approx 39.0 \times 10^{-6} \sin(2\pi ft) \text{ mA} + 1.11 \text{ mA}$ , demonstrating a significant reduction by a factor of  $\approx 10^3$  in supply current modulation.

The second set of simulation work undertaken was to analyse the comparative performances of the three different instrumentation amplifier designs. A combined differential (1V) and common-mode signal (2V) was applied to the inputs and then the differential gains and common-mode gains were measured as a function of frequency. Common-mode rejection ratios were then calculated.

To take into account practical device and component mismatches, parameters of all the components were set with random variations of  $\pm 4\%$  to  $\pm 8\%$ . These included the variations in all the NPN and PNP transistor parameters and resistors. Fig.4 shows the simulation CMRR results of three

different circuit configurations as indicated in the figure. The graph clearly illustrates the advantages of the Fig.3 instrumentation amplifier. It is anticipated that the performances will be improved if the real device mismatches are lower than the worst-case used in these simulations.

#### 5. CONCLUSION AND FUTURE WORK

A second generation current-mode instrumentation amplifier, incorporating a common-mode bootstrapping technique to improve CMRR, has been presented. The preliminary simulation results demonstrate the potential improvement in CMRR with this circuit topology. Despite device mismatches, the results show that the new instrumentation amplifier out performs previously described configurations.

At the time of writing, experimental verification using an experimental prototype is being undertaken, the results of which will be presented at the symposium. Following this, work will begin on development of a transistor-level realisation for SPICE evaluation and subsequent monolithic implementation.

#### REFERENCES

- [1] C. Toumazou and F.J. Lidgey, 'Novel current-mode instrumentation amplifier', *Electronics Letters*, 1989, Vol.25, pp.228-230.
- [2] Q.S. Zhu, F.J. Lidgey and M.A. Vere Hunt, 'Improved wide-band, high CMRR instrumentation amplifier', *Clin. Phys. Physiol. Phys. Meas.*, 1992, Vol.13, Suppl.A, pp.51-55.
- [3] B.L. Hart and R.W.J. Barker, 'DC matching errors in the Wilson current-source', *Electronics Letters*, 1978, Vol.12, pp.389-390.