Mnemonic	Description		Status bits	
BYTE ORIENTED FILE REGISTER OPERATIONS				
ADDWF	Add W and f		C, DC, Z	
ANDWF	AND W and f		Z	
CLRF	Clear f		Z	
CLRW	Clear W		Z	
COMF	Compliment f		Z	
DECF	Decrement f		Z	
DECFSZ	Decrement f and Skip if Zero			
INCF	Increment f		Z	
INCFSZ	Increment f and Skip if Zero			
IORWF	Inclusive OR W with f		Z	
MOVF	Move f		Z	
MOVWF	Move W to f			
NOP	No Operation			
RLF	Rotate Left f through Carry		C	
RRF	Rotate Right f through Carry		C	
SUBWF	Subtract W from f		C, DC, Z	
SWAPF	Swap nibbles in f			
XORWF	Exclusive OR W with f		Z	
BIT ORIENTED FILE REGISTER OPERATIONS				
BCF	Bit Clear f			
BSF	Bit Set f			
BTFSC	Bit Test f, Skip if Clear			
BTFSS	Bit Test f, Skip if Set			
LITERAL AND CONTROL OPERATIONS				
ADDLW	Add literal and W		C, DC, Z	
ANDLW	AND literal and W		Z	
CALL	Call Subroutine			
CLRWDT	Clear Watchdog Timer		TO, PD	
GOTO	Go to address			
IORLW	Inclusive OR literal with W		Z	
MOVLW	Move literal to W			
RETFIE	Return from interrupt			
RETLW	Return with literal in W			
RETURN	Return from Subroutine			
SLEEP	Go into Standby mode		TO, PD	
SUBLW	Subtract W from literal		C, DC, Z	
XORLW	Exclusive OR literal with W		Z	

16F88 Special File Registers & RAM sorted by bank & alphabetically

The following tables are designed to supplement the 16F88 datasheet by Microchip.

	Green = bit set on reset "1"
	White = bit clear on reset "0"
	Yellow = unknown on reset (not cleared or set)
	X = not in use, usually returns a zero "0"
*	Asterisk = bit is read only
	Blue = RAM unknown state on reset (not cleared or set)

Common to banks 0, 1, 2 & 3 (all banks)

	Bit 7	6	5	4	3	2	1	0
FSR								
INDF								
INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PCL								
PCLATH				Write Buffer for Upper five PCL bits				
STATUS	IRP	RP1	RP0	*NOT_TO	*NOT_PD	Z	DC	C
RAM 0x070 - 0x07F								

Specific to bank 0 (PORTB & TMR0 repeated in bank 2)

	Bit 7	6	5	4	3	2	1	0
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO		ADON
ADRESH	A/D Result Register (MSB)							
CCP1CON			CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
CCPR1H	Capture/Compare/PWM Register 1 (MSB)							
CCPR1L	Capture/Compare/PWM Register 1 (LSB)							
PIR1		ADIF	*RCIF	*TXIF	*SSPIF	CCP1IF	TMR2IF	TMR1IF
PIR2	OSFIF	CMIF		EEIF				
PORTA								
PORTB								
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREG	USART Receive Data Register							
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
SSPBUF	Synchronous Serial Port Receive/Transmit Buffer							
T1CON		T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	NOT_T1SYNC	TMR1CS	TMR1ON
T2CON		TOUTPS3	TOUTPS2	POUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
TMR0	Timer0 Module Register							
TMR1H	Holding Register for 16-bit Timer1 (MSB)							
TMR1L	Holding Register for 16-bit Timer1 (LSB)							
TMR2	Timer2 Module Register							
TXREG	USART Transmit Data Register							
RAM 0x020 - 0x06F								

Specific to bank 1 (OPTION_REG & TRISB repeated in bank 3)

	Bit 7	6	5	4	3	2	1	0
ADCON1	ADFM	ADCS2	VCFG1	VCFG0				
ADRESL	A/D Result Register (LSB)							
ANSEL		ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
CVRCON	CVREN	CVROE	CVRR		CVR3	CVR2	CVR1	CVR0
OSCCON		IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0
OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
OSCTUNE			TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
PCON							NOT_POR	NOT_BOR
PIE1		ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
PIE2	OSFIE	CMIE		EEIE				
PR2								
TRISA								
TRISB								
TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D
SSPADD	Synchronous Serial Port Address							
SSPSTAT	SMP	CKE	D_A	I2C_STOP	I2C_START	R_W	UA	BF
RAM 0x0A0 - 0x0EF								

Specific to bank 2(PORTB & TMR0 repeated in bank 2)

	Bit 7	6	5	4	3	2	1	0
EEADR								
EEADRH								
EEDATH								
EEDATA								
PORTB								
TMR0	Timer0 Module Register							
WDTCON				WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN
RAM 0x110 - 0x16F								

Specific to bank 3(OPTION_REG & TRISB repeated in bank 1)

	Bit 7	6	5	4	3	2	1	0
EECON1	EEPGD			FREE	WRERR	WREN	WR	RD
OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
TRISB								
RAM 0x190 - 0x1EF								