

## Features

- Fast Read Access Time – 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 40 mA Active Current
  - 100  $\mu$ A CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$  Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5V  $\pm$  10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Commercial and Industrial Temperature Ranges

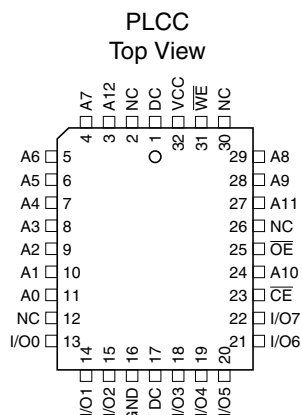
## Description

The AT28C64B is a high-performance electrically-erasable and programmable read only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100  $\mu$ A.

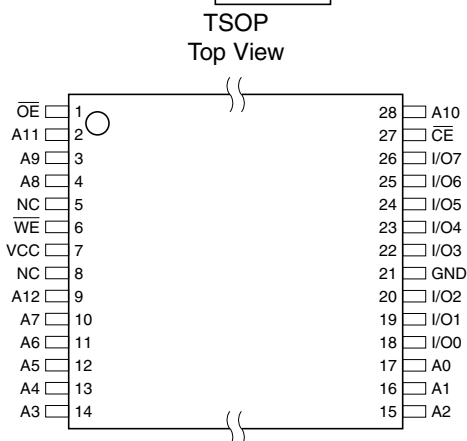
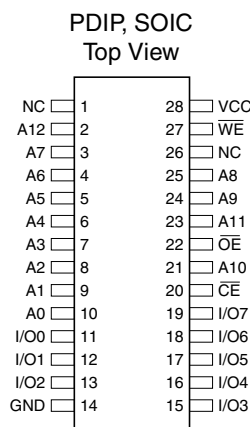
(continued)

## Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.



## 64K (8K x 8) Parallel EEPROM with Page Write and Software Data Protection

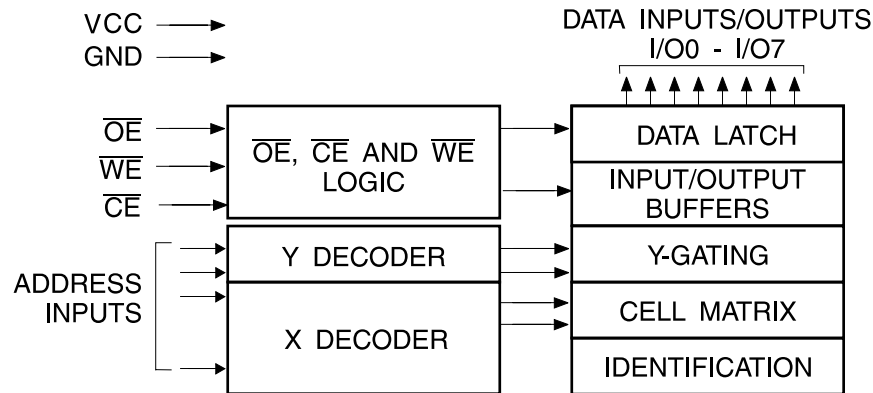
## AT28C64B



The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by  $\overline{\text{DATA POLLING}}$  of  $\text{I/O}_7$ . Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground .....	-0.6V to +6.25V
All Output Voltages with Respect to Ground .....	-0.6V to $V_{CC} + 0.6V$
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground .....	-0.6V to +13.5V

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## Device Operation

**READ:** The AT28C64B is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

**BYTE WRITE:** A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high initiates a write cycle. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{WC}$ , a read operation will effectively be a polling operation.

**PAGE WRITE:** The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150  $\mu s$  ( $t_{BLC}$ ) of the previous byte. If the  $t_{BLC}$  limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each  $\overline{WE}$  high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

**DATA POLLING:** The AT28C64B features  $\overline{DATA}$  Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O<sub>7</sub>. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin.  $\overline{DATA}$  Polling may begin at any time during the write cycle.

**TOGGLE BIT:** In addition to  $\overline{DATA}$  Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O<sub>6</sub> toggling between one and zero. Once the write has completed, I/O<sub>6</sub> will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

**DATA PROTECTION:** If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

**HARDWARE DATA PROTECTION:** Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 3.8V (typical), the write function is inhibited; (b)  $V_{CC}$  power-on delay – once  $V_{CC}$  has reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high, or  $\overline{WE}$  high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the  $\overline{WE}$  or  $\overline{CE}$  inputs will not initiate a write cycle.

**SOFTWARE DATA PROTECTION:** A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the “Software Data Protection Algorithm” diagram in this datasheet). After writing the 3-byte command sequence and waiting  $t_{WC}$ , the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of  $t_{WC}$ , read operations will effectively be polling operations.

**DEVICE IDENTIFICATION:** An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V  $\pm$  0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

## DC and AC Operating Range

		AT28C64B-15	AT28C64B-20	AT28C64B-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

## Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	X	
Output Disable	X	V <sub>IH</sub>	X	High Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub> <sup>(3)</sup>	V <sub>IL</sub>	High Z

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to the "AC Write Waveforms" diagrams in this datasheet.
  3. V<sub>H</sub> = 12.0V ± 0.5V.

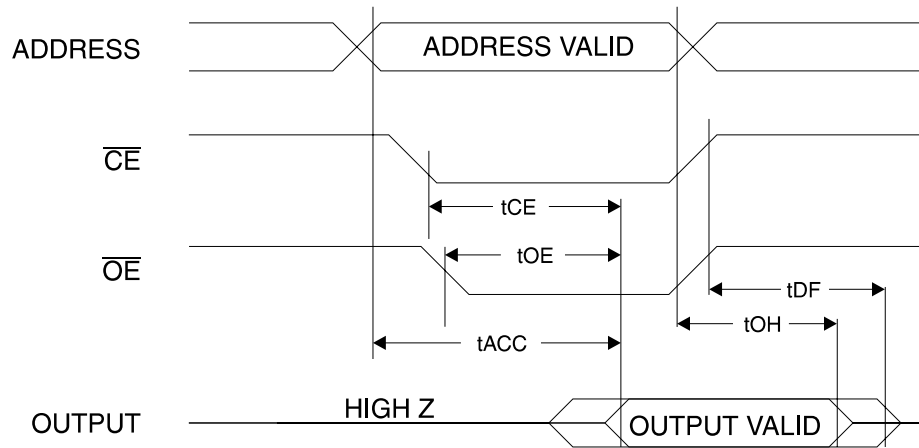
## DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> + 1V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>CC</sub>		10	μA
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V <sub>CC</sub> + 1V	Com., Ind.	100	μA
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current TTL	$\overline{CE} = 2.0V$ to V <sub>CC</sub> + 1V		2	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz; I <sub>OUT</sub> = 0 mA		40	mA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.40	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

## AC Read Characteristics

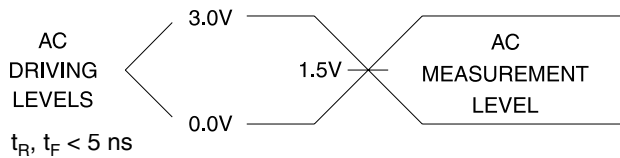
Symbol	Parameter	AT28C64B-15		AT28C64B-20		AT28C64B-25		Units
		Min	Max	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
$t_{OH}$	Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

## AC Read Waveforms<sup>(1)(2)(3)(4)</sup>

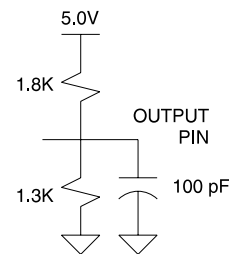


- Notes:
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
  - $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
  - $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5 \text{ pF}$ ).
  - This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



## Output Test Load



## Pin Capacitance

$f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

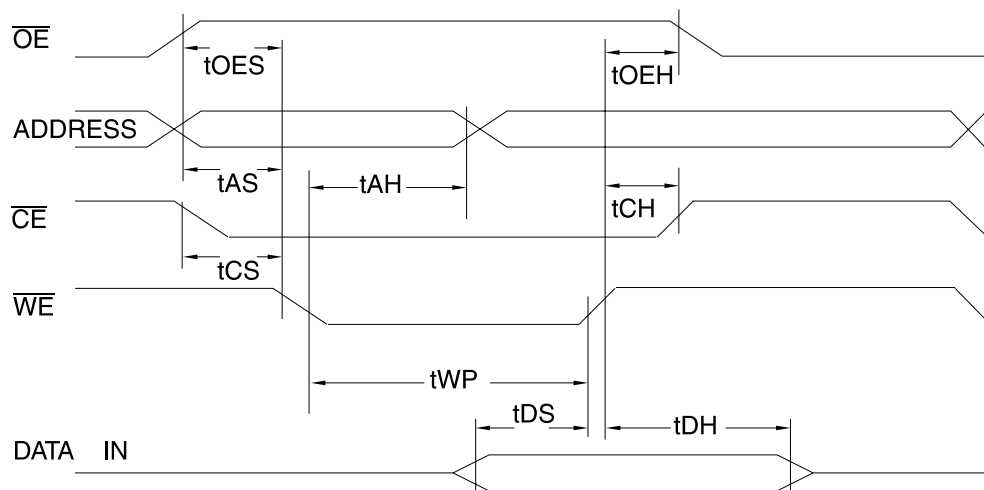
- Note:
- This parameter is characterized and is not 100% tested.

## AC Write Characteristics

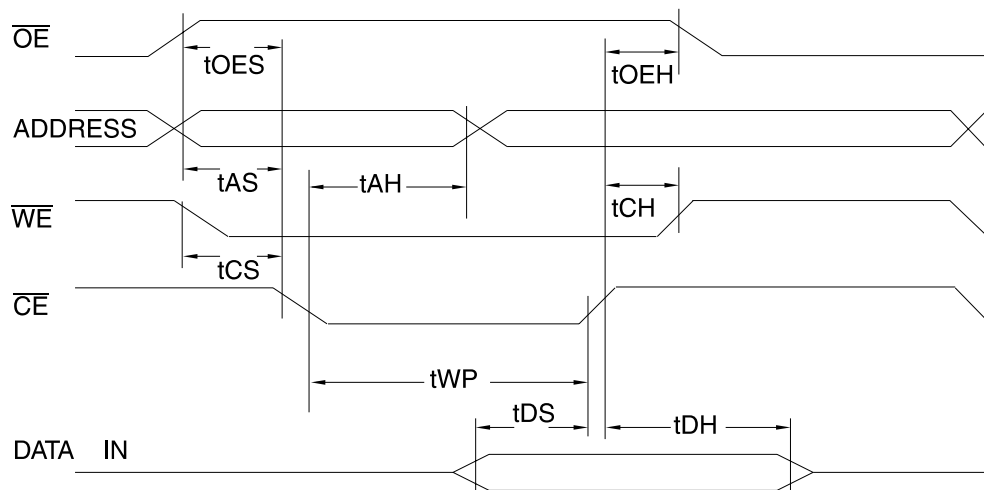
Symbol	Parameter	Min	Max	Units
$t_{AS}, t_{OES}$	Address, $\overline{OE}$ Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Chip Select Setup Time	0		ns
$t_{CH}$	Chip Select Hold Time	0		ns
$t_{WP}$	Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ )	100		ns
$t_{DS}$	Data Setup Time	50		ns
$t_{DH}, t_{OEH}$	Data, $\overline{OE}$ Hold Time	0		ns

## AC Write Waveforms

### $\overline{WE}$ Controlled



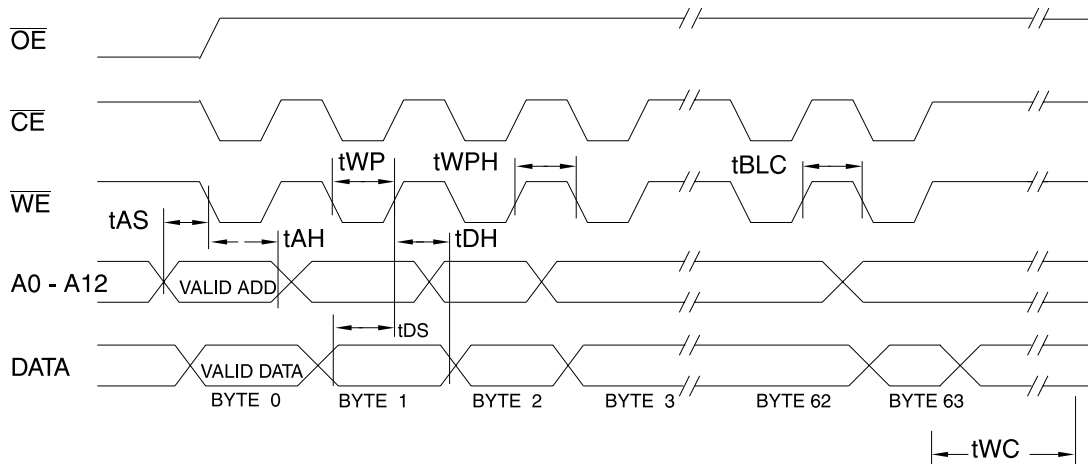
### $\overline{CE}$ Controlled



## Page Mode Characteristics

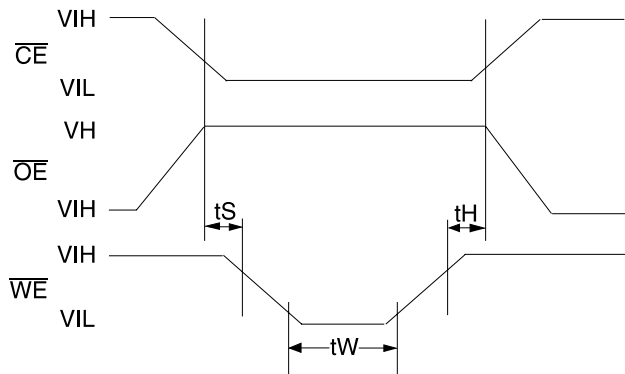
Symbol	Parameter	Min	Max	Units
$t_{WC}$	Write Cycle Time		10	ms
$t_{WC}$	Write Cycle Time (option available; contact Atmel sales office for ordering part number)	0	2	ms
$t_{AS}$	Address Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{DS}$	Data Setup Time	50		ns
$t_{DH}$	Data Hold Time	0		ns
$t_{WP}$	Write Pulse Width	100		ns
$t_{BLC}$	Byte Load Cycle Time		150	$\mu$ s
$t_{WPH}$	Write Pulse Width High	50		ns

## Page Mode Write Waveforms<sup>(1)(2)</sup>



- Notes:
1. A6 through A12 must specify the same page address during each high to low transition of  $\overline{WE}$  (or  $\overline{CE}$ ).
  2.  $\overline{OE}$  must be high only when  $\overline{WE}$  and  $\overline{CE}$  are both low.

## Chip Erase Waveforms

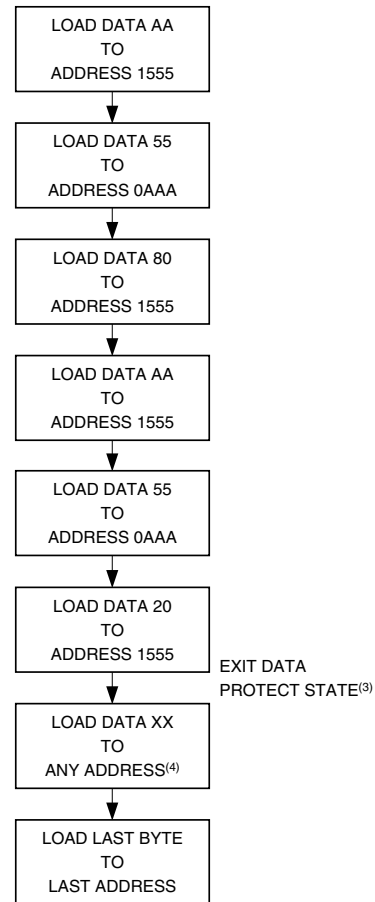


$t_S = t_H = 1 \mu\text{sec (min.)}$

$t_W = 10 \text{ msec (min.)}$

$V_H = 12.0 \pm 0.5V$

## Software Data Protection Disable Algorithm<sup>(1)</sup>



1. Data Format: I/O7 - I/O0 (Hex);  
Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

The diagram illustrates the timing relationships for a memory access cycle. The signals shown are:

- $\overline{OE}$** : Output Enable, active low. It transitions from high to low at the start of the cycle and returns to high after the data is no longer needed.
- $\overline{CE}$** : Chip Enable, active low. It transitions from high to low to enable the memory and returns to high to disable it.
- $\overline{WE}$** : Write Enable, active low. It transitions from high to low to enable writing and returns to high to enable reading.
- A0 - A5**: Address bus lines 0 through 5, labeled as **BYTE ADDRESS**.
- A6 - A12**: Address bus lines 6 through 12, labeled as **PAGE ADDRESS**.
- DATA**: Data bus, showing the data being written (AA, 55, A0) and read (55, A0).

Key timing parameters are indicated by arrows:

- tAS**: Address Setup time before  $\overline{WE}$  goes low.
- tAH**: Address Hold time after  $\overline{WE}$  goes high.
- tWP**: Write Pulse width (low time of  $\overline{WE}$ ).
- tWPH**: Write Pulse height (low level of  $\overline{WE}$ ).
- tDH**: Data Hold time after  $\overline{WE}$  goes high.
- tBLC**: Burst Latency time between the first and second burst.
- tDS**: Data Setup time before  $\overline{WE}$  goes low.
- tWC**: Write Cycle time from the start of the write pulse to the end of the data hold time.

- # AT28C64B

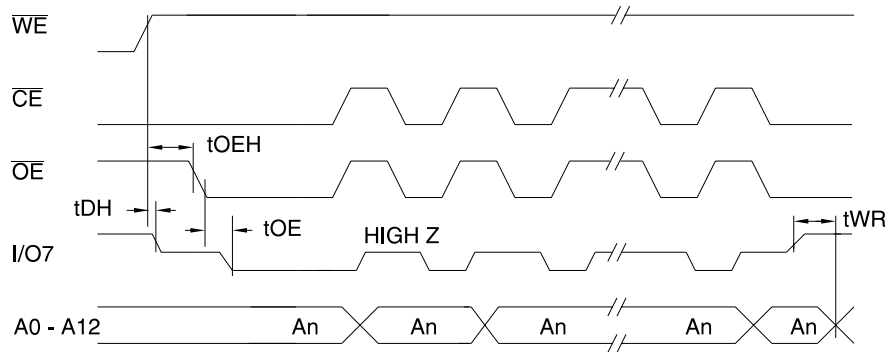


## Data Polling Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Units
$t_{DH}$	Data Hold Time	0			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	0			ns
$t_{OE}$	$\overline{OE}$ to Output Delay <sup>(2)</sup>				ns
$t_{WR}$	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.  
2. See "AC Read Characteristics".

## Data Polling Waveforms

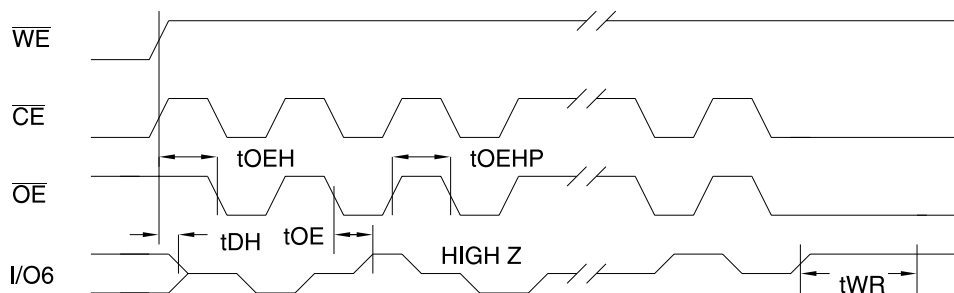


## Toggle Bit Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Units
$t_{DH}$	Data Hold Time	10			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	10			ns
$t_{OE}$	$\overline{OE}$ to Output Delay <sup>(2)</sup>				ns
$t_{OEHP}$	$\overline{OE}$ High Pulse	150			ns
$t_{WR}$	Write Recovery Time	0			ns

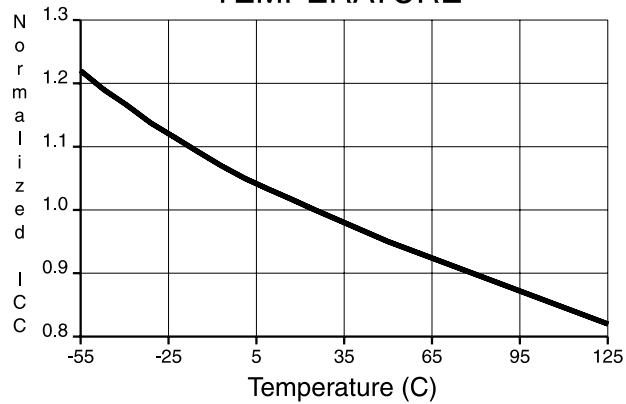
Notes: 1. These parameters are characterized and not 100% tested.  
2. See "AC Read Characteristics".

## Toggle Bit Waveforms<sup>(1)(2)(3)</sup>

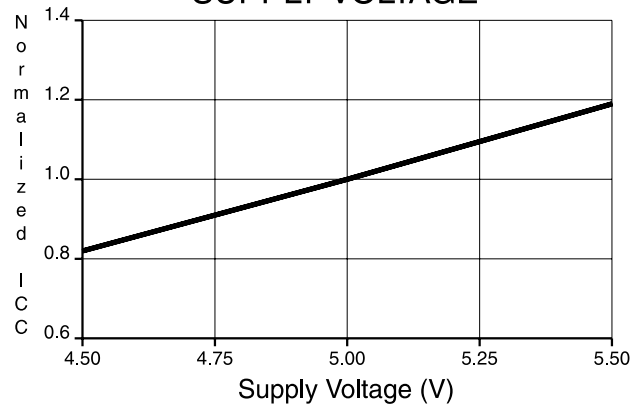


Notes: 1. Toggling either  $\overline{OE}$  or  $\overline{CE}$  or both  $\overline{OE}$  and  $\overline{CE}$  will operate toggle bit.  
2. Beginning and ending state of I/O6 will vary.  
3. Any address location may be used but the address should not vary.

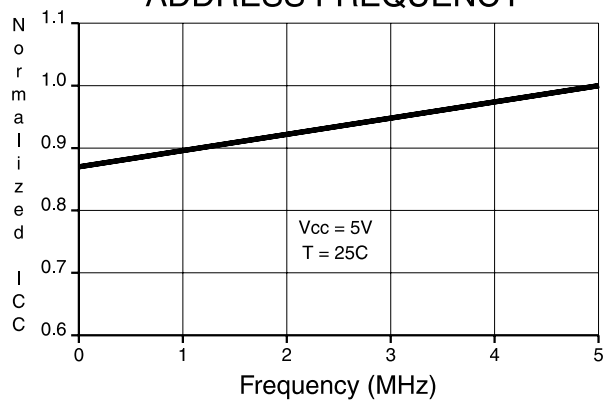
NORMALIZED SUPPLY CURRENT vs.  
TEMPERATURE



NORMALIZED SUPPLY CURRENT vs.  
SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs.  
ADDRESS FREQUENCY



## Ordering Information<sup>(1)</sup>

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JC	32J	Commercial (0°C to 70°C)
			AT28C64B-15PC	28P6	
			AT28C64B-15SC	28S	
			AT28C64B-15TC	28T	
			AT28C64B-15JI	32J	Industrial (-40°C to 85°C)
			AT28C64B-15PI	28P6	
			AT28C64B-15SI	28S	
			AT28C64B-15TI	28T	
200	40	0.1	AT28C64B-20JC	32J	Commercial (0°C to 70°C)
			AT28C64B-20PC	28P6	
			AT28C64B-20SC	28S	
			AT28C64B-20TC	28T	
			AT28C64B-20JI	32J	Industrial (-40°C to 85°C)
			AT28C64B-20PI	28P6	
			AT28C64B-20SI	28S	
			AT28C64B-20TI	28T	
250	40	0.1	AT28C64B-25JC	32J	Commercial (0°C to 70°C)
			AT28C64B-25PC	28P6	
			AT28C64B-25SC	28S	
			AT28C64B-25TC	28T	
			AT28C64B-25JI	32J	Industrial (-40°C to 85°C)
			AT28C64B-25PI	28P6	
			AT28C64B-25SI	28S	
			AT28C64B-25TI	28T	

Note: 1. See "Valid Part Numbers" table below.

## Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C64B	15	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	20	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28C64B	–	W

## Die Products

Reference Section: Parallel EEPROM Die Products
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Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)
W	Die







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