



Software Chip Erase

The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFH). After the software chip

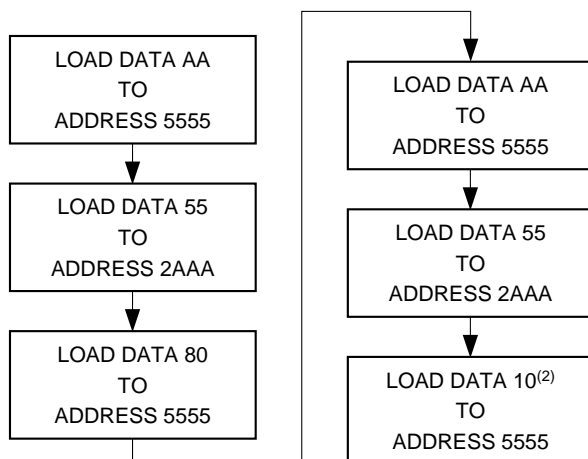
erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time required to erase the whole chip is t_{EC} (20 ms). The software data protection is still enabled even after the software chip erase is performed.

Chip Erase Cycle Characteristics

Symbol	Parameter	
t_{EC}	Chip Erase Cycle Time	20 ms Max

Note: 1. Please refer to individual data sheets for the minimum and maximum values of the t_{AS} , t_{AH} , t_{DS} , t_{DH} , t_{WP} , t_{BLC} , and t_{WPH} parameters.

Chip Erase Software Algorithm⁽¹⁾⁽³⁾



- Notes:
1. Data Format: (Hex); Address Format: (Hex).
 2. After loading the 6-byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion in 20 ms (max).
 3. The flow diagram shown is for a x8 part. For a x16 part, the data should be 16 bits long (e.g., the data to be loaded should be AAAA for step 1 in the algorithm).

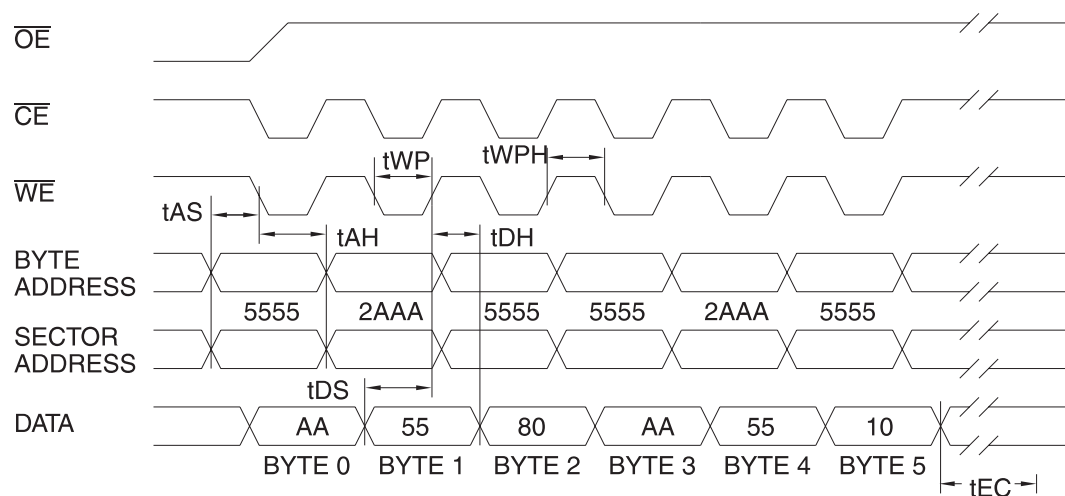
Parallel EEPROMs

Application Note

Rev. 0544B-10/98



Chip Erase Cycle Waveforms



Note: 1. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Japan

Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand

North America:

1-(800) 292-8635

International:

1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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