leading edge

What's hot in the design community

Edited by Fran Granville

NASA/JPL

But how do the Martians feel?

"We're sending a complicated system into an unknown environment at very high speed. I feel calm. I feel ready. I can only conclude it's because I don't have a full grasp of the situation."

–Mark Adler, deputy mission manager for NASA's Spirit Mars-rover landing, *Scientific American*, March 2004

Test high-speed crosspoint switch in ac domain

By Nicholas Cravotta

THE 2×2, 1.5-Gbps Scan90CP02 crosspoint switch from National Semiconductor provides LVDS (low-voltage differential signaling), programmable pre-emphasis, and support for IEEE 1149.6. The recently approved IEEE 1149.6 specification extends the capabilities of IEEE 1149.1 for evaluating ac-coupled interconnects. Many high-speed LVDS connections now use ac, or capacitive, coupling to eliminate signal offsets between drivers and receivers that reside at remote locations. However, you cannot test ac-coupled, differential interconnections on datapaths faster than 1 Gbps using traditional IEEE 1149.1 techniques, which target testing static, dc-coupled, single-ended networks.

IEEE 1149.6 extends boundary scan into the ac domain and does not interfere with the transmission path. IEEE 1149.6 requires the addition of a pulse generator in the signal-path driver and a pulse detector in the signal-path receiver. In an ac-coupled interconnect, only the edge transitions of the pulse train pass through the coupling capacitors; the receiver sees and must detect a string of narrow pulses at each transition and provide a pass/fail indication at the receiver's IEEE 1149.1 port.

The 1.5-Gbps, 2×2 Scan90CP02 LVDS crosspoint switch has programmable pre-emphasis and support for IEEE 1149.6 to enable testing of ac-coupled interconnects.

Programmable pre-emphasis improves signal integrity across backplanes and cables and across configurations and applications, including conventional crosspoint switches, buffer/repeaters, 1-to-2 splitters, and 2-to-1 multiplexers, and it provides redundancy for data and clock signals. Available in a 5×5-mm LLP-28 package, the Scan90CP02 sells for $4.95 (1000).

▶**National Semiconductor**, www.national.com.

Serial data storage receives broad board support

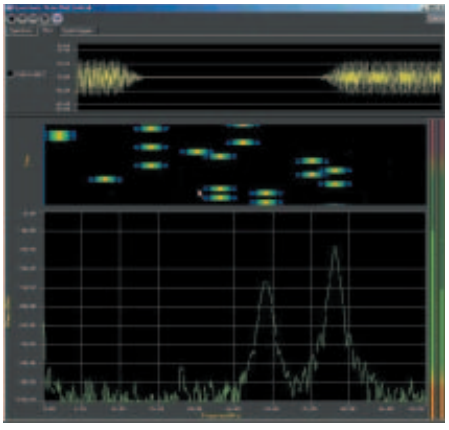
TARGETING EASIER OEM DESIGN of serial-data-storage systems, Ario Data Networks has announced a trio of similar SATA (Serial ATA) bridge-controller boards. The Ario-FST is for 2-Gbps Fibre connections, the Ario-SST is an Ultra 320SCSI board, and the Ario-iST is a 1-Gbps iSCSI unit, each interfacing as a Serial ATA bridge controller. The modular architecture allows Ario's boards to offer common features across all interfaces. These features include dual-path capability, host-side management for as many as 512 concurrent commands, and device-side queues as deep as 64 commands. Ario's boards also monitor the system power rails, the cooling-fan operation, and key temperatures.

The speed and capacity of systems you can build with these boards should meet your data needs for the near future. Ario says that the maximum sustained bandwidth and configuration using an array of these controllers reaches 350 Mbps and 120 Tbytes for the Ario FST, using 40 controllers and 480 drives; 350 Mbps and 84 Tbytes for the Ario-SST, using 15 controllers and 336 drives; and 200 Mbps and 5.1 Tbytes per Internet Protocol address for the Ario-iST. Prices per board are approximately $1900.

—by Bill Schweber

▶**Ario Data Networks**, 1-408-432-8778, www.ariodata.com.

Enhanced software boosts power of broadband, deep-memory communications-signal analyzer



At the top, the CS35000 presents a frequency-hopping RF signal in the time domain. At the bottom is the signal's spectrum. In the middle, you see the signal amplitude displayed versus both frequency and time. Frequency is on the horizontal axis; time is on the vertical axis and increases as you move upward.

What used to be Celerity, a division of L3 Communications, is now the Cupertino, CA, division of Aeroflex, the company that owns several other well-known RF-instrument manufacturers, including the former Marconi Instruments and IFR Systems. Aeroflex is the CS35000-series BSA (broadband-signal analyzer) and recorder family. Although *EDN* rarely covers product reintroductions, today's CS35000 is so much more capable than the system Celerity introduced two years ago that the announcement is truly newsworthy.

Aeroflex says that the BSA, whose prices range from $65,000 to $350,000, is the only instrument that can simultaneously capture several RF signals having bandwidths as great as 600 MHz and display the modulation in multiple ways in real time. The views include time- and frequency-domain (spectrum) representations as well as a single color-graded view of amplitude versus both frequency and time. The company has built systems that acquire as many as 16 signals, but the system architecture can handle much larger numbers. According to Aeroflex, few, if any, other RF-signal analyzers accept more than two inputs.

Despite its ability to perform real-time extraction of signals applied to carriers via complex schemes, such as 1024 QAM (1024-level quadrature-amplitude modulation), the analysis sometimes can't keep pace with the signal—for example, in a military-communications system that hops to a different carrier frequency 77,000 times per second. For such situations, you can equip each channel with as much as 16 Gbytes of memory. The system can then analyze its acquired data at 60 hops/sec—approximately 1/1300 of real time. In fact, if you want to grasp what appears on the display as it appears, you must run the analysis at a still-lower speed.

New analysis software includes modules for demodulation of amplitude- and frequency-modulated signals and frequency-shift- and minimum-shift-keyed signals, determination of adjacent-channel power ratios, error-vector magnitude, and signal statistics. Other new features include simultaneous parameter analysis and parameter-based triggering.

—by Dan Strassberg

▶**Aeroflex**, 1-800-835-2352, 1-316-522-4981, www.aeroflex.com.

TESTER KEEPS YOUR CABLES IN HARNESS

Engineers spend lots of money on high-end test equipment and then often resort to jerry-built, basic ohmmeter-type tests for their cables. But these crude setups are always time-consuming and often inconsistent, so a commercial cable tester, such as the Signature 1100R+ from Cirris Systems, may be a wise purchase.

Cables are relatively simple but still a source of potential headaches. You can quickly and consistently test them with the Signature 1100R+ system.

This $1995 unit tests as many as 1024 points (or more using optional expander units) and detects resistance of 0.001Ω to 100 kΩ, checking for opens, shorts, crossed wires, high-resistance errors, and insulation resistance up to 5 MΩ. The system learns what a good cable is from your known-good sample cable, or you can download test information via a serial port. You get your test results as fast as you can plug those cables in, on a four-line/20-character display as well as a pass/fail LED.—by Bill Schweber

▶**Cirris Systems Corp**, 1-801-973-4600 www.cirris.com.

DILBERT *By Scott Adams*

▶**InStat/MDR finds that 14.4% of US consumers currently use a wireless phone as their primary phone, with the remaining 85.6% still using a landline as their primary phone.**

Imaging competitors choose divergent paths to a nebulous destination

At first glance, Texas Instruments' $15 (100,000) TMS320DM320, with its prominent dual ARM9 and C54x DSP cores inside, may look identical to the earlier generation $13 DM310. However, whereas the DM310 used a 144-MHz ARM925, the DM320 uses a 160-MHz ARM926EJ-S, along with a sequencer. In the DM320, TI also includes the earlier $11 DM270's memory-traffic controller, supporting chips, modules, and host CPUs with both multiplexed—that is, SDRAM—and nonmultiplexed buses, versus the DM310's less comprehensive SDRAM-only controller.

The DM320 enhances the capabilities and speed of the DM310's eight-MAC (multiply-accumulate) imaging coprocessor and preview engine, and it provides a glueless interface to LCDs. Other additions include a hard-wired DCT (direct-cosine-transform) accelerator block, On-The-Go support in the 12-Mbps USB controller, and various chip-to-chip interfaces. The anticipated performance results of all this fine-tuning speak for themselves (**Table 1**). TI forecasts that, with first engineering samples now in hand and undergoing debugging, it will be able to ramp the DM320 into volume production by the fourth quarter; the fact that the DM320 shares its precursors' 0.13-micron process will assist in this ramp-up. Beta development software is now available, and TI plans a general development-tool rollout for early next quarter.

The incremental hardware acceleration TI has added to successive processor generations draws the company ever closer to the hard-wired approach that competitors such as NuCore Technology have long espoused (see "Imaging chip set speedily delivers the bits," *EDN*, Aug 3, 2000, pg 28). However, aside from the opponents' common use of an ARM9 processor core, significant implementation differences remain. TI, after all, leverages a DSP that has general-purpose roots, whereas NuCore relies on imaging-optimized circuitry. Kyocera (www.kyocera.com) is now shipping 3 million- and 5 million-pixel cameras that contain NuCore chip sets; the cameras can capture near-infinite-length bursts of 3.5 and three frames/sec, respectively. (Nonvolatile-storage capacity places the only limitations on the length of the bursts.)

According to NuCore, if it weren't for front-end sensor and back-end flash-memory performance bottlenecks, the 3 million-pixel camera's sustained bursts could hit five frames/sec.

Aside from NuCore's imaging-centric digital-processing approach, the other reason for the architecture's speed is the inclusion of a separate analog-based chip for white balance, black-level calibration, and other sensor-optimization functions instead of a reliance on DSP cycles to implement those functions. The two-chip combo of NDX-1260 analog and SiP-1270 digital processors for CCD-based systems costs $16 (1 million); if your design employs a CMOS sensor, you need to purchase only the $13.50 SiP-1270. The two companies' chip announcements come on the heels of both near-term euphoria and long-term uncertainty about the viability of the stand-alone-camera market. Camera-inclusive cell phones on the low end and still-image-enhanced camcorders encroaching from above may, by the decade's end, squeeze out digital still cameras, even with video enhancements.

—by Brian Dipert

▶**Texas Instruments**, 1-972-995-2011, www.ti.com.
▶**NuCore Technology**, 1-408-907-7100, www.nucoretech.com.

TABLE 1-PERFORMANCE CAPABILITIES OF VARIOUS TI IMAGE PROCESSORS

	DM320	DM310	DM270	DSC25
Still image (millions of pixels/sec)	9.4	7.1	4.4	2.2
MPEG-4 simple profile	30 frames/sec, VGA	30 frames/sec, QVGA	15 frames/sec, VGA	24 frames/sec, QVGA
MJPEG (millions of pixels/sec)	32	18	16	8.1
H.264 baseline profile	20 frames/sec, QCIF	10 frames/sec, QCIF	10 frames/sec, QCIF	Eight frames/sec, QCIF
Preview engine (pixel clock, MHz)	100	40	40	40

Be a SATA superstar

If *EDN*'s recent appetizer on serial ATA whetted your appetite for knowledge about this subject, you might want to try Intel Press' *Serial ATA Storage Architecture and Applications* as your next course (see "Speedy simplicity," *EDN*, Jan 22, 2004, pg 33). Co-authors Knut Grimsrud and Hubbert Smith have extensive credentials in the field: Knut is Intel's principal engineer for SATA 1.0 and SATA II and was the technical working group chairman during SATA 1.0 definition, and Smith is a program manager with Intel's Platform Networking Group and the chairman of the Serial ATA II cable/connector focus group.

The comprehensive, $54.95 book (ISBN 0-97717861-8-6) is remarkably up to date, including coverage of port multipliers and the second generation 3-Gbps bus variant. As the inevitable SATA evolution continues through its estimated 10-year lifetime, you'll be able to keep abreast of the alterations and enhancements by monitoring the Intel Press Web site.—by Brian Dipert

▶**Intel Press**, 1-503-264-2169, www.intel.com/intelpress.

Bus advancements improve cell-phone connections

THE EVER-INCREASING amount of data flowing between various subsystems in modern cell phones, coupled with unrelenting pressure to reduce the phones' cost and size, creates considerable engineering challenges that two interconnect innovations strive to solve. Focusing first on the image-sensor-to-application processor (for camera-inclusive phones) and application-processor-to-display links, National Semiconductor has evolved the WhisperBus technology that it acquired when it bought Vivid Semiconductor to come up with the MPL (Mobile Pixel Link) bus. Traditional multibit parallel-LVCMOS interfaces are bulky, and they become increasingly noisy and power-hungry as their speeds climb.

MPL, in contrast, is a single-ended, two-wire (data and strobe), bidirectional, low-swing-current-mode approach that, in its first silicon implementation, can provide 83-Mbps point-to-point throughput—for example, 320×240-pixel frames at 18-bit color depth and 60-frame/sec video rates. National's first MPL-enabled products are the 85-cent (1000) LM2501 in a 24-bump CSP, which can implement an 8-bit YUV camera-to-processor interface, and the $1.26 LM2502 in 49-contact LLC, whose two data channels support 16-bit processor buses and dual displays. National expects that, in the long term, it will license its MPL transceiver cores for integration into others' chips rather than remain as a supplier of standalone devices. To stimulate overall market growth, the company offers the specifications for MPF in an open, royalty-free manner, similar to the approach that Silicon Image (www.siliconimage.com) took with DVI a few years ago.

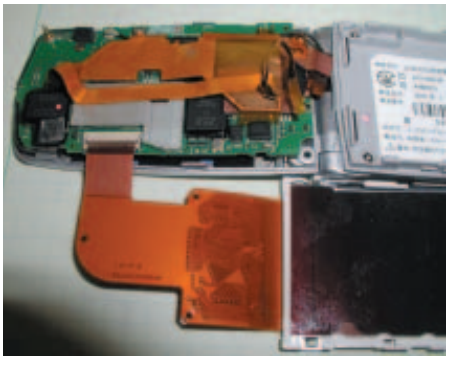
With its low-voltage dual-port memories, IDT (International Device Technology) focuses on the bidirectional bus that links the application and baseband processors in cell phones. Latest generation CDMA-1X EV-DO, 802.11b and other leading-edge wireless networks exceed 1-Mbps speeds and, in the process, overwhelm the 1.5-Mbps (minus software and protocol overhead) UART- or low speed USB interprocessor-communication channels in today's phones. IDT's alternative approach comprises a family of memory-mapped, 1.8V, dual-port RAMs, including the 70P248 and 70P258 low-power variants, which also offer I/O-voltage flexibility to 3.3V LVCMOS levels. All devices are now available in sample quantities and will enter volume production next quarter; **Table 1** provides product-family details.—by Brian Dipert

▶**Integrated Device Technology**, 1-408-727-6116, www.idt.com.

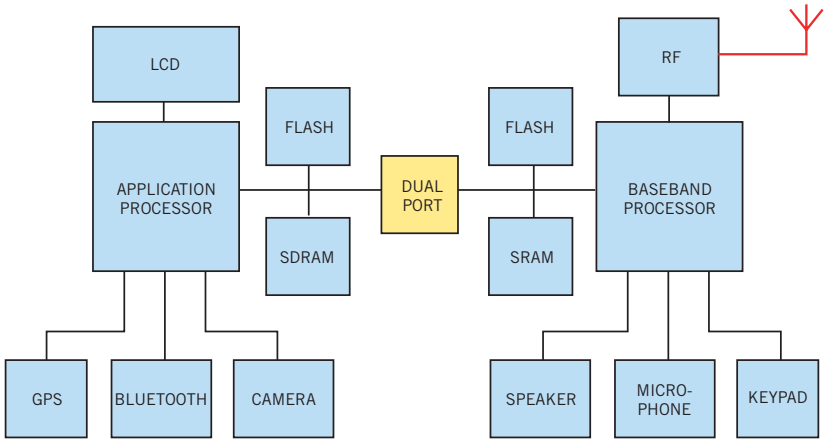
▶**National Semiconductor**, 1-408-721-5000, www.national.com.

TABLE 1–KEY 1.8V, DUAL-PORT-RAM SPECS

Part	Configuration	Package	Price (1 million)
70P35	8k×18	Fine-pitch BGA, TQFP	$3.50
70P34	4k×18	Fine-pitch BGA, TQFP	$2.50
70P258	8k×16	Fine-pitch BGA	$3.50
70P248	4k×16	Fine-pitch BGA	$2.50
70P25	8k×16	Fine-pitch BGA, TQFP	$3.50
70P24	4k×16	Fine-pitch BGA, TQFP	$2.50



(a)



(b)

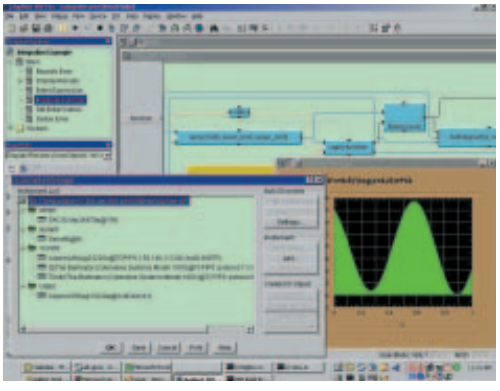
National Semiconductor focuses on improving today's cumbersome sensor-to-processor and processor-to-display links (a), whereas IDT ensures that ever-faster wireless protocols don't swamp the interprocessor bus (b).

▶**InStat/MDR forecasts PDA shipments to have a 6.5% compound-annual-growth rate from 2003 to 2008 and forecasts shipments to reach 10.8 million units in 2004.**

T&M-application-development package should please loyal users and attract new ones

Agilent Technologies' VEE (Visual Engineering Environment) graphical package for developing measurement, control, test, and data-acquisition applications doesn't have the largest market share, but it does have a loyal following. Agilent says that Version 7.0's enhancements to the open, standards-based environment will make those followers even more loyal and bring new ones into the fold. The enhancements support a wider range of programming styles and enable developers to more intuitively accomplish even more test-system-development tasks, thus allowing more time to focus on design challenges.

The enhancements include quick, simple access to VEE from within the Microsoft .NET framework, an open, industry-standard programming environment that expands VEE's customization capabilities. Users need not purchase any other .NET applications; the framework is an integral Windows component for building and running next-generation software applications and Web services. For example, the framework makes it easy to programmatically create files, send an e-mail report, or invoke a Web page.



VEE Pro 7.0 optimizes instrument connectivity with an easy-to-use instrument manager.

Easy-to-use development tools for VEE include undo and redo for faster program development; property editing to allow quick and easy changes to any design- or user-interface control properties; and expanded panel-editing features, such as visible grid, rubber-band, and object alignment, to simplify programming layout. The product also supports direct LAN- and USB-connected instrumentation using industry-standard protocols and support for industry-standard IVI-COM instrument drivers.

VEE Pro 7.0 sells for $1495. Upgrades from previous versions of VEE are also available, with prices starting at $389.

—by Dan Strassberg

▶**Agilent Technologies**, 1-800-452-4844, www.agilent.com/find/vee.

TCAM engine hits 18 Mbits with dual LA-1 Interfaces

NetLogic Microsystems' new NSE5512GLQ network-search engine operates as fast as 250 MHz, has 18 Mbits of table storage, and supports dual LA-1 (look-aside) interfaces, as defined by the Network Processing Forum. Many NPU (network-processing-unit) designs require network-search engines to include multiple NPUs—one for ingress processing and one for egress processing. Two LA-1 ports on the same search-engine device enable ingress and egress to share table resources. Applications for the TCAM (ternary-content-addressable-memory) NSE5512GLQ include multiservice switches, wireless infrastructure, enterprise, and edge routers that need to offload functions such as IPv4 and IPv6 packet forwarding and classification or require packet-classification and traffic-management capabilities for firewalls, intrusion-detection systems, load balancing, broadband access, and access-control lists.

The device supports arbitration of requests across the two LA-1 interfaces, optional in-band or out-of-band table management, host-based TCAM-table management, a database-parity-scan engine, and interfaces for a general-purpose host CPU and associated data SRAM. Each device can support as many as 512,000 IPv4 and as many as 128,000 IPv6 routing entries, and you can cascade it without search-latency penalty. Clock rates include 250 MHz for NPUs, 66 MHz for host CPUs, and 133 MHz for associated data SRAM.

A dual-search capability enables the search engine to execute searches on two logical tables using the same key, a feature useful for independent table searches, such as for access-control lists and quality of service, which conserves both interface bandwidth and table resources by eliminating the need to replicate commonality between look-up address tables. The device can return as much as 256 bits of associated data as two results.

With a 1V core, the search engine comes in a 900-ball FCBGA package measuring 31×31×1 mm. It is pin- and software-compatible across 4.5-, 9-, and 18-Mbit devices, and it is footprint-compatible with the previous generation NSE4000GLQ family. The development kit includes an evaluation card that plugs directly into the Intel (www.intel.com) Angel Island and Aleutian Island development platforms, NPU microcode, an API, and simulation models.

Selling for $300 (sample quantities), the NSE5512GLQ is available for sampling and will begin volume production in the second quarter.—by Nicholas Cravotta

▶**NetLogic Microsystems Inc**, 1-212-533-9090, www.netlogicmicro.com.

▶**According to the International Biometric Group, biometrics, a $1 billion industry today, will reach $4.6 billion by 2008.**