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October 2001

Phase-Locked Loops – characteristics and applications

1.0 Abstract

The function of a complete phase-locked loop (PLL) feedback system was explored through the characterisation of the Philips HEF4046B complementary metal oxide semiconductor (CMOS) integrated circuit (IC). Applications of interest were investigated: fixed frequency multiplication (50 Hz→204.8 kHz) with infinite input-locked noise rejection, demodulation of frequency modulated waveforms (≈200 kHz carrier with <12.5 kHz) and clean-signal clock regeneration—as with digital data transmission pulse synchronisation. Phase comparators (PC) type one and two of the 4046 were tested, recording waveform and transfer characteristics at ≈100 kHz, using a dual-phase shift test circuit. In conjunction with the 4046's voltage-controlled oscillator (VCO)(studied for an output of f=0 to >1Mhz), basic closed-loop PLL operation was achieved for 42-112 kHz logic signals. All configurations performed to theory, allowing experimental confirmation of PC1/2 loop stability, *ad hoc* resistor-capacitor (RC) filter requirements, capture ($2f_C$) and lock ($2f_L$) frequency range, input/output phase difference and harmonic centre-frequency (f_o) locking. Frequency multiplication [PC2], demodulation [PC1/2] and clock regeneration [PC1] were performed using a suitable phase comparator, whilst observing their transient responses and operation range. Although advanced PLL stability and filter characteristics were not directly tested, they are well supported by theory and are worthy of further study.

2.0 Introduction

A *phase-locked loop* consists fundamentally of two parts: a *phase detector*, which discriminates between the phase of two input signals, and a *voltage-controlled oscillator*, with its output frequency depending on the input voltage. Under the right conditions, this feedback system ensures that the local VCO produces an identical frequency output to the input—matching it with a fixed phase. Although PLLs might appear to be an obscure electronic nicety, applications are surprisingly wide-ranging and commonplace. They are often used in frequency synthesis and multiplication, signal demodulation and noise-rejection. Common examples include: the demodulation of amplitude modulated or frequency modulated signals in radio receivers[1] and in automatic station tuning; the removal of mains interference in cathode-ray tube displays in televisions and computer monitors; and in the synchronisation of signals from a noisy source (e.g. magnetic storage media such as floppy disks), where a clean clock-signal at the same data bit-rate is required.

Although it may not be necessary to completely understand the intricate workings of a *'black-box'* PLL integrated circuit, it is essential to have a sound comprehension of its behaviour—such that it can be used with confidence. The approach taken in this report is to generalise the characteristics of the HEF4046, and to outline a means of implementing it in some specific applications.

[1] Note that the PLL is configured differently to decode FM signals compared to AM signals

3.0 Theoretical Background

Due to the nature of the electronics involved, detailed background notes and theory are provided—and should be referred to at the reader's discretion[2].

Overview

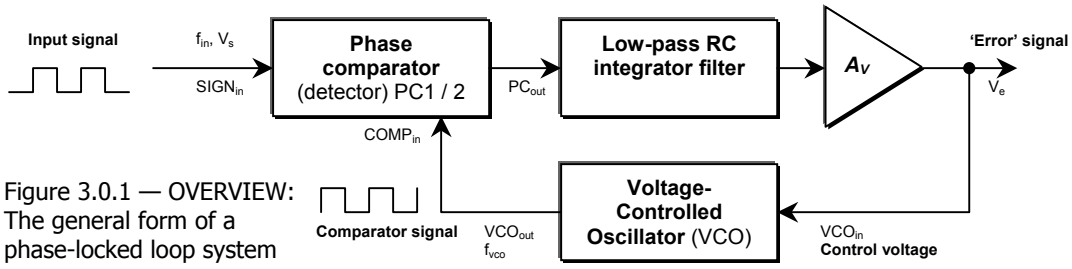
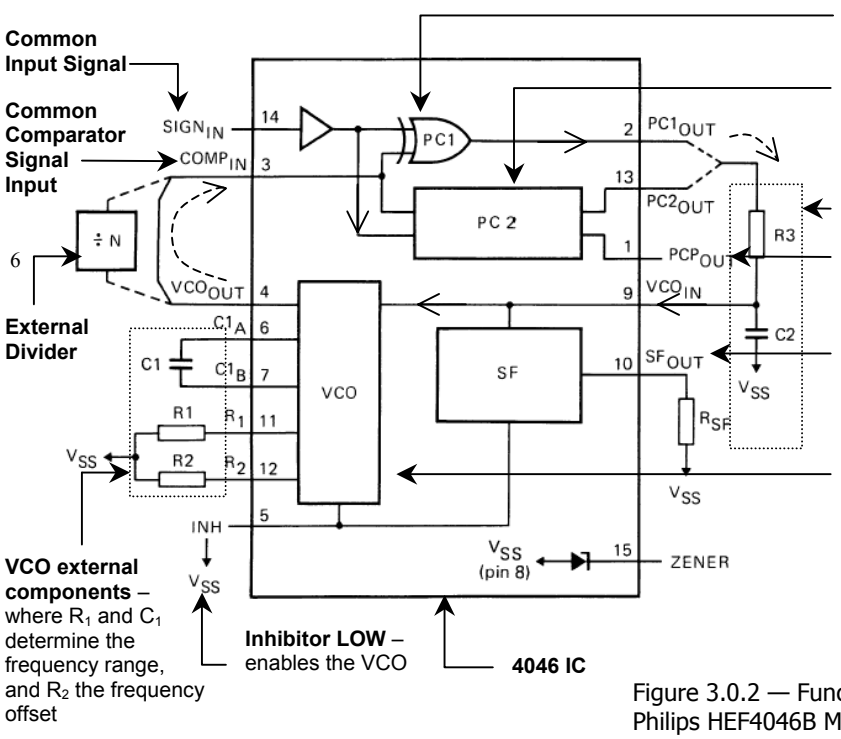


Figure 3.0.1 — OVERVIEW: The general form of a phase-locked loop system

[3]

Figure 3.0.1 (above) summarises the basic outline loop structure of a PLL, used to stay in sync with an input signal. The HEF4046B is a single chip phase-locked loop IC, consisting of a linear VCO and two different onboard phase comparators with common signal input amplifier and comparator pins. Figure 3.0.2 (below) shows the functional schematic of the 4046. When the signal produced by the VCO does not match the input frequency at $SIGN_{in}$, the resultant 'error' signal after filtering and amplification, causes the VCO frequency to move towards that of the input signal. Under suitable conditions[4], the VCO should therefore be able to lock[5] onto the input frequency, maintaining a constant phase relationship.



[7]

Figure 3.0.2 — Functional diagram of the Philips HEF4046B MSI 16-pin DIL plastic IC

[2] Detailed PLL analysis as a control system using small-signal stability analysis is not included in this report. For details see Page 648 – Chapter 9.29 – The Art of Electronics – 2nd Edition – Horowitz & Hill - CUP
[3] Adapted from Figure 9.67 - Page 644 – Chapter 9.29 – The Art of Electronics – 2nd Edition – Horowitz & Hill - CUP
[4] See section 3.3
[5] References to a PLL locking onto a signal typically describes the situation where the system is able to produce an output at the frequency of the input. Where this is not the case, the PLL is described as being out of lock.
[6] See the later section on applications in frequency multiplication, demodulation and clock signal regeneration
[7] Adapted from Figure 1 – Page 2 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995

3.1 Phase Comparators

Both phase comparator types compare two logic level input frequencies (signal and comparator) and produce an output that is a direct measure of their relative phase difference. If instead they differ in frequency, the PC provides a periodic output at that difference.

Phase comparator type 1—XOR gate

PC1 consists purely of an EXCLUSIVE OR gate driven by analogue or digital square wave signals. Figure 3.1.1 (below) illustrates a typical example response.

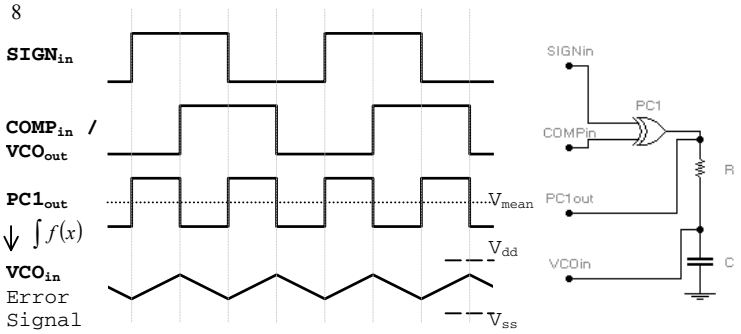


Figure 3.1.1 — Typical input / output waveforms for PC1

The mark-space ratio of $PC1_{out}$ depends upon the phase difference of the inputs—with identical signals giving a LOW output, and π out of phase signals producing a HIGH output.

In this example, the input logic waveforms are π/2 out of phase, producing a x2 frequency PC1 output signal, with a 50% duty factor and a mean output voltage of ½V_{dd}.

As the mean output voltage of $PC1_{out}$ is directly dependent upon the phase difference of the two input signals, a simple linear response (as shown in figure 3.1.2 – below) can be predicted.

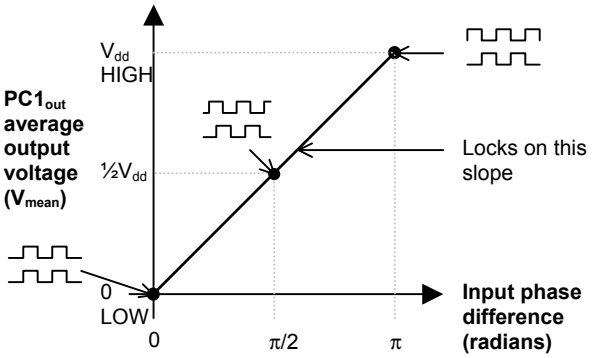


Figure 3.1.2 — Signal-to-comparator inputs phase difference response for phase comparator 1—demonstrating linear behaviour

In the above example of figure 3.1.1, the output yields a ½V_{dd} output, given the π/2 input phase difference.

Phase comparator type 2—edge-controlled digital memory network circuit

PC2 consists of four flip-flops, control gating and a 3-state output based on n/p-type field effect transistors (FETs) (see figure 3.1.3 below)—responding only to positive-going edges of the input signals.

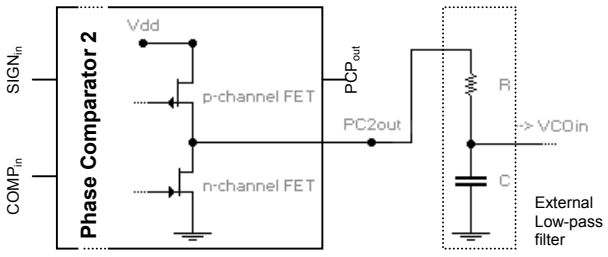


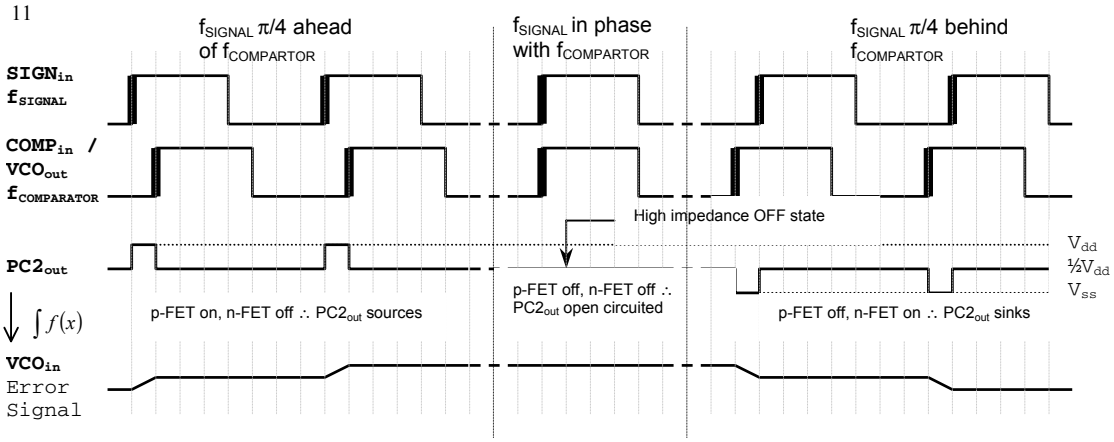
Figure 3.1.3 – An overview of the PC2 output: a dual FET capacitor drive circuit

There are three different output states:

- $PC2_{out}$ sinking current
- $PC2_{out}$ sourcing current
- $PC2_{out}$ open-circuited

[8] Adapted from Figure 4 – Page 4 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995
[9] Adapted from Figure 3 – Page 4 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995

As with any group of logic gate processes, the exact response of PC2 given any input conditions can be modelled using a logic state diagram[10]. Figure 3.1.4 (below) briefly summarises common PC2 scenarios.



Phase comparator two sinks or sources current for a time corresponding to the phase difference between the two input signals—remaining off (open circuited) at all other times. This results in PC2 pulses about the high impedance off state. The mark-space ratio of $PC2_{out}$ therefore depends directly on the input phase difference

Figure 3.1.4 — Typical input / output waveforms for PC2, responding to positive-edge going transitions (marked in bold)

Given the way in which the lead-lag phase comparator (PC2) operates, and its similarities with PC1, we could expect yet another simple linear relationship (as illustrated below in figure 3.1.5).

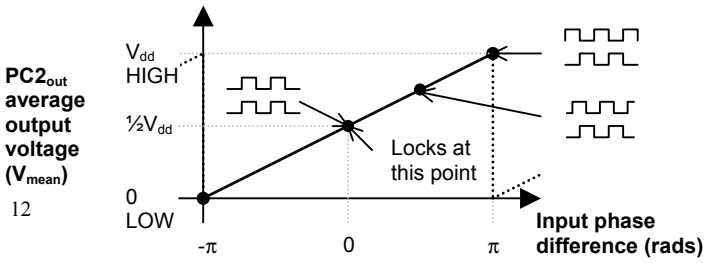


Figure 3.1.5 [left] — Signal-to-comparator inputs phase difference response for phase comparator 2—demonstrating repeated linear behaviour (compare figure 3.1.2)

A relative phase shift in either direction away from in-phase, results in an output voltage above or below the ½V_{dd} point.

3.2 Voltage–controlled oscillator

The linear voltage-controlled oscillator uses one external capacitor (C_1) and two external resistors (R_1 / R_2) to configure its range of operation. Adjusting the voltage level at VCO_{in} between V_{ss} and V_{dd}, thus varies the VCO_{out} square-wave output frequency. Figure 3.2.1 (right) shows the typical correlation between the external resistors and the output frequency range. Figure 3.2.2 (overleaf) represents the schematic of a similar VCO.

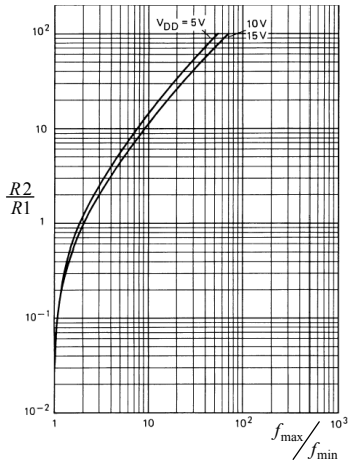


Figure 3.2.1 [right] — The typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min} 13

[10] See Figure 6 – Page 6 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995
[11] Adapted from Figure 5 – Page 5 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995
[12] Adapted from Figure 9.70 - Page 645 – Chapter 9.27 – The Art of Electronics – 2nd Edition – Horowitz & Hill - CUP
[13] Source: Figure 9 – Page 12 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995

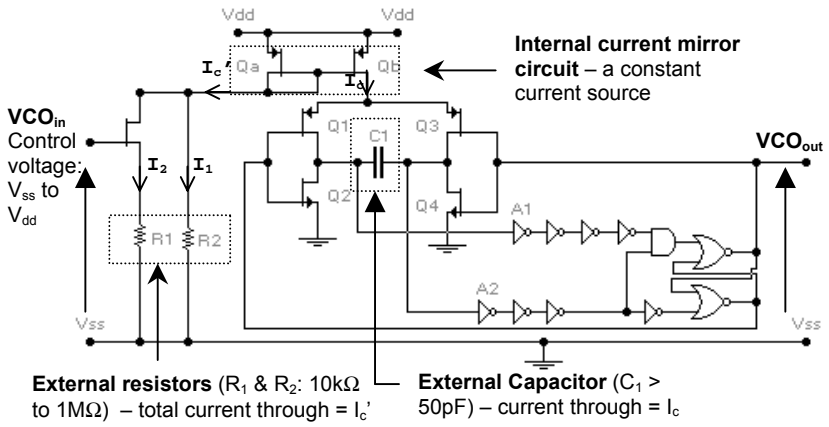


Figure 3.2.2 — A Voltage-controlled oscillator circuit (similar to the HEF4046B VCO) using a capacitor driven from CMOS output stages

External capacitor C_1 is alternate charged in both directions, through a cycle. If FET Q_A and Q_B are identical, the capacitor charging current (I_c) is equal to the input current ($I_c'=I_1+I_2$)

Resistor R_1 and capacitor C_1 controls the frequency range of the VCO, whilst R_2 enables it to provide a frequency offset, if necessary.

3.3 Basic closed phase-locked loop operation

At the most fundamental level, we can form a PLL using only a looped phase comparator and voltage-controlled oscillator—such as in the case of a PC1 based PLL[14]. This seems like a straightforward feedback system, comparable to an op-amp feedback circuit. Crucially, however, the PLL system *measures phase*, but responds by *adjusting frequency*. This introduces a $\pi/4$ phase shift into the loop.

Consequently, an external LC filter must be present in order to operate PC2 in a complete PLL. This is required so that the series of pulses from the three state output of PC2 is able to adjust the voltage across the capacitor—depending upon the relative phase and frequency difference between the two input signals. It is this voltage across the capacitor that is feed into the VCO input, upon which the VCO output frequency depends. Figure 3.3.1 (below) briefly outlines the potential PC2 PLL scenarios.

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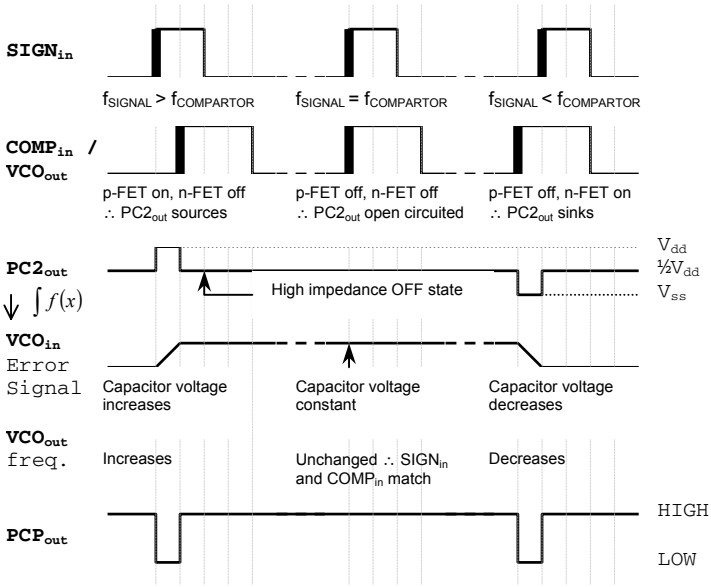


Figure 3.3.1 — Example waveforms for a PC2 phase-locked loop

❶ PC2 respond to transitions only from positive-going edges of the input signals (marked in bold)—regardless of duty factors

❷ The comparator consequently sinks or sources current for a time corresponding to the phase difference—remaining off (open circuited) at all other times

❸ $PC2_{out}$ therefore varies the voltage across the capacitor in the LC filter—which is feed into the VCO input, varying the VCO output frequency accordingly to bring $COMP_{in}$ into synchronism with $SIGN_{in}$

❹ Ultimately, a PC2 phase locked condition is achieved and is indicated by PCP_{out} = HIGH

[14] Stability analysis shows that a basic PLL system without a filter is inherently stable. However, practical applications of PLLs in this way are limited.
[15] Adapted from Figure 5 – Page 5 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995

A PC2 phase-locked loop with LC filter is therefore always able to maintain zero phase difference between the input signal and output signal, produced by the VCO. This differs from a PC1 PLL, which cannot maintain this condition across a range of frequencies (as illustrated in figure 3.3.2 below).

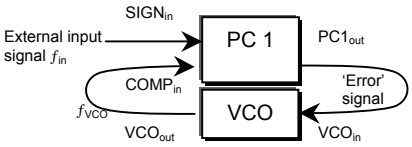


Figure 3.3.2 — Phase difference between signals for a PC1 PLL (based on the phase relationship determined previously in figure 3.1.1)

f_{min}, f_o, f_{max} corresponds to the minimum, central and maximum frequency, respectively, that the VCO can handle.

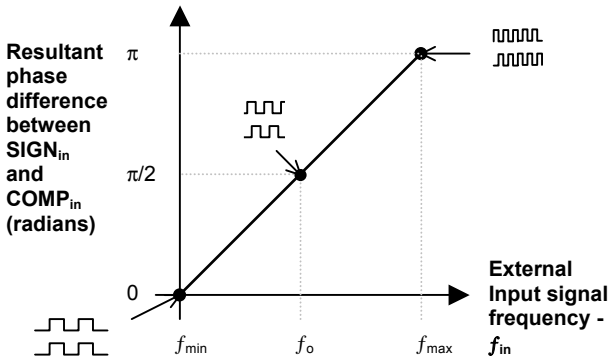


Table 3.3.1 (below) summarises the intended design characteristics of both comparator types[16], used in a PLL. These will be verified in the course of this investigation.

Characteristic	Phase Comparator 1	Phase Comparator 2
No input signal to the PLL at SIGN$_{in}$	The VCO in the PLL system adjusts to the centre frequency[17] (f_o)	The VCO in the PLL system adjusts to the minimum frequency (f_{min})
Phase difference between signals: SIGN$_{in}$ and COMP$_{in}$	π/2 at the central frequency (f_o), tending to 0 and π at the end of the lock range ($2f_L$)	ALWAYS a zero phase difference in lock
PLL locks onto harmonics of the central frequency (f_o)	Yes – it is possible	No
Rejection of input signal noise	High	Low
Lock[18] ($2f_L$) and capture[19] ($2f_c$) frequency range	Dependent upon the low-pass filter characteristics; ($f_c < f_L$)	The lock and capture range are identical ($f_c = f_L$)

3.4 PLL applications: outlined

Frequency multiplication

A PLL can be readily used to generate a fixed integer multiple of an input frequency. This is achieved with a signal divider placed in the feedback loop between the VCO and phase comparator. There are, however, many other (possibly easier) ways of performing frequency multiplication. The PLLs key distinguishing feature,

[16] Adapted from Page 9 – Philips Semiconductors HEF4046B MSI Phase-Locked Loop Product Specifications – January 1995
[17] The centre frequency (f_o) is the frequency of the VCO when VCO$_{in}$ is ½V$_{dd}$
[18] The lock frequency range ($2f_L$) corresponds to the range of the input signal on which the PLL will stay locked, if it was initially in lock. This equals the full VCO frequency range from f_{max} to f_{min}
[19] The capture frequency range ($2f_c$) corresponds to the range of the input signal on which the PLL will lock, if it was initially out of lock

however, is its ability to lock onto and follow[20] a regular input signal—even where noise is present on that waveform. This means that the reproduced signal is a clean copy (or clean multiple) of the input signal—a process of noise-rejection.

FM demodulation

In frequency modulation, the original waveform is encoded in a carrier signal by variation of its frequency. A typical phase-locked loop can therefore be locked to the incoming signal for demodulation. As the voltage varying the VCO's output frequency is proportional to the original waveform, this is therefore the desired demodulated signal.

Clock regeneration

In data transmission, pulses are synchronised to a transmitting-side clock signal, and typically sent across a single channel link. At the receiving end, a clean clock signal needs to be generated for comparison. This allows the received pulses, which may be distorted or noisy from the transmission medium, to be interpreted. By locking a standard PLL to the received data signal, a regenerated clock signal can be sourced from the output of the VCO.

4.0 Experimental work and characterisation

Phase Comparator Characterisation

4.1 Method: Phase Comparator

Phase comparators type one and two were independently tested by the application of two identical[21] ($f \approx 100$kHz) square wave CMOS signals, with an adjustable phase difference between them ($-\pi < \theta < \pi$). These were produced by a dual phase-shift test circuit and fed into the input ($SIGN_{in}$) and comparator ($COMP_{in}$) terminals of the HEF4046 (as in figure 4.1.1 below).

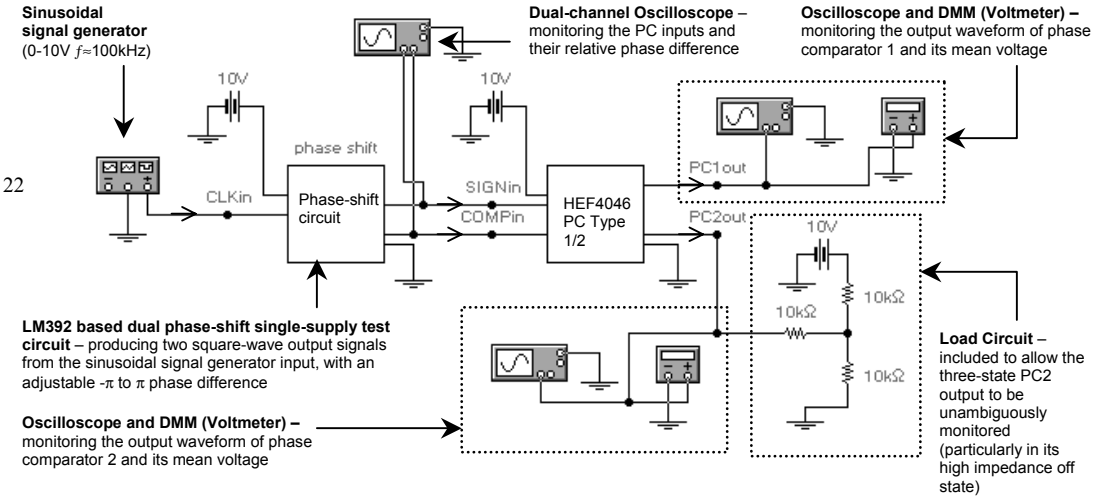


Figure 4.1.1 — A combined circuit representation of the set-up used to characterise HEF4046 phase comparators type one and two

[20] Once a PLL is locked to the frequency of an input signal, it will track this as long as the rate of change of the input frequency is not overly large
[21] The square waveforms were produced from a single sinusoidal oscillator, external to the dual-phase shift circuit, and therefore are indistinguishable
[22] Although shown monitoring the outputs of PC1 and PC2 simultaneously in this figure, these were in fact performed separate—however there is of no consequence.

The phase difference between the two PC inputs was varied from -π to π, allowing the output waveforms to be observed and recorded from the oscilloscopes. Its transfer characteristics (the mean PC output voltage dependence on the two input signals phase difference) were also measured across this range[23] (to allow comparison to figure 3.1.2 and 3.1.5).

4.2 Results: Phase Comparator

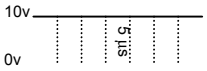
Figure 4.2.1 and 4.2.2 (below) represents the transfer characteristics measured for PC1 and PC2, respectively[24].

Figure 4.2.1 — Phase dependent transfer characteristic for phase comparator 1

PC1 output waveforms:

(A) – With zero phase difference, PC_{out} gave a constant 0V output $\therefore V_{ss}$

(B) – For an (almost) π phase difference, PC_{out} gave a nearly constant 10V output (V_{dd}):



(C) – For π/2, PC_{out} produced a 10V 200kHz square-wave with a nearly 1:1 mark-space ratio

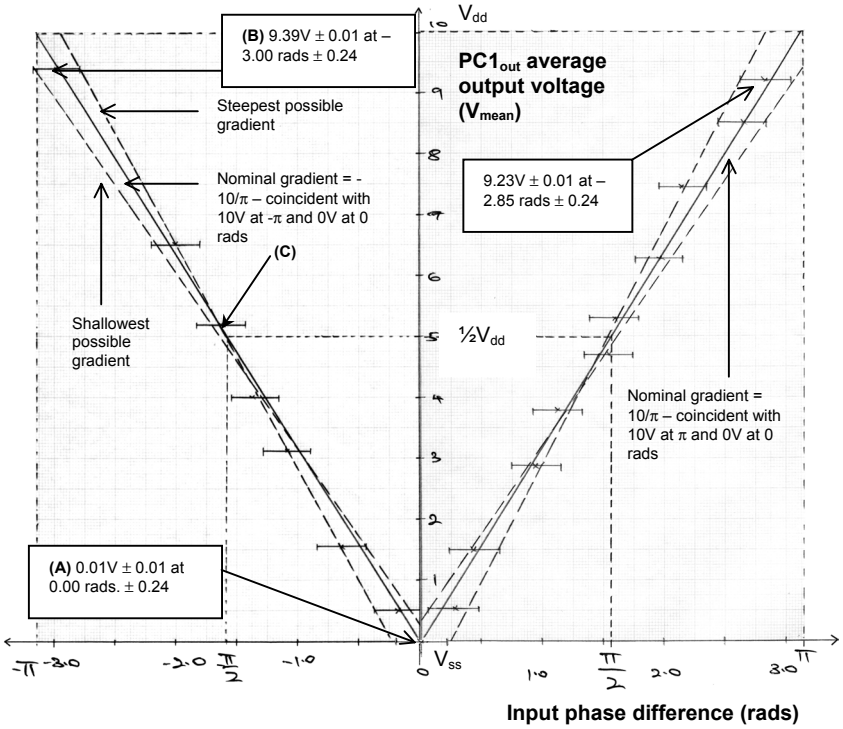
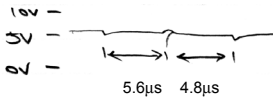


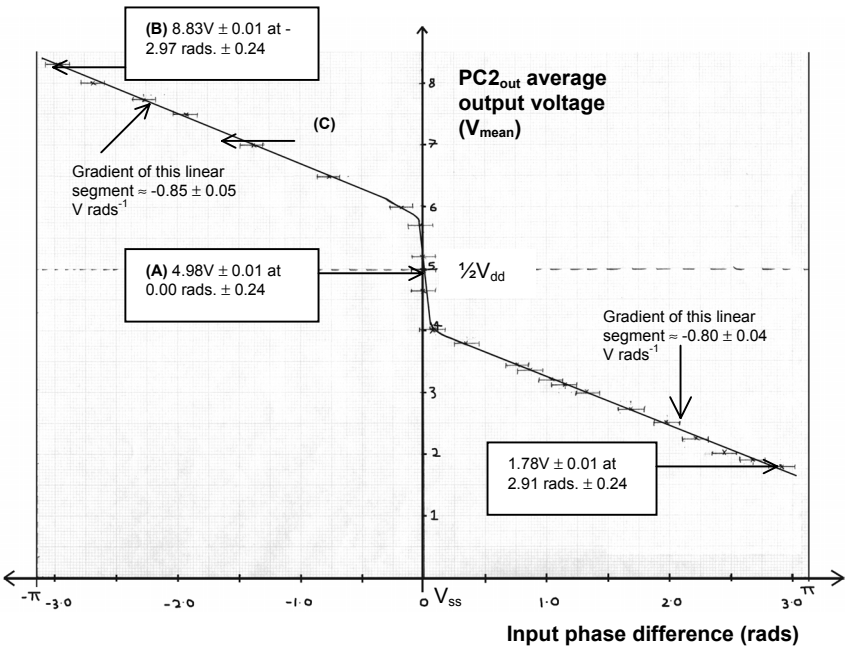
Figure 4.2.2 — Phase dependent transfer characteristic for phase comparator 2

PC2 output waveforms:

(A) – With zero phase difference, PC_{out} gave a (slightly noisy) constant 5V (½V_{dd}) output:



(B) & **(C)** – see overleaf

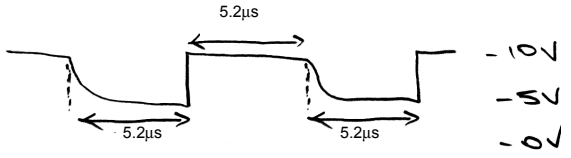


[23] Although figure 4.1.1 shows the DMMs and oscilloscopes connected to the PC outputs simultaneously, these were measured/observed separately due to the capacitance effects caused by the x10 oscilloscope scope probes used

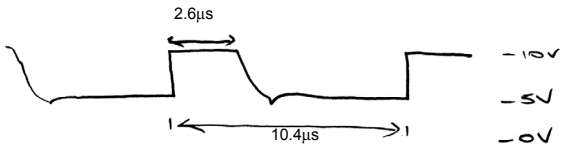
[24] Y-axis error bars are not shown due to their negligible size at this scale

PC2 output waveforms (cont'd):

(B) – For an (almost) π input phase difference, PC_{out} produced a square-wave output between 5V (½V_{dd}) and 10V (V_{dd}) with a mark-space ratio of 1:1 (shown right). 5.2µs here, translates into a frequency of ≈100kHz.
[Likewise, an identical output between 0 (V_{ss}) and 5V (½V_{dd}) is produced for the opposite (almost) π input phase difference].



(C) – For ≈π/2, PC_{out} produced a square-wave output between 5V (½V_{dd}) and 10V (V_{dd}) (shown right). The two input signals had a phase difference corresponding to 2.6µs between falling edges, and 10.4µs between rising edges.



4.3 Discussion: Phase Comparator

Phase Comparator 1

The results from the characterisation of phase comparator one do not appear to reveal any surprises at all! In part, this can be attributed to the simple and well-documented behaviour of such a standard XOR logic gate, of which it is entirely composed. Figure 4.2.1 (the results for PC1) matches well with the theoretical result (figure 3.1.2), showing a distinct and clean linear relationship between the input phase difference and the mean output voltage. Furthermore, it is also not surprising to see that the resultant graph is symmetric about the y-axis—as a relative phase difference in one direction is identical to a relative phase difference in the opposite sense.

Due to the nature of the phase-shift test-circuit that was used, a shift of exactly ±π was never achieved. Nevertheless, the nominal gradient lines shown on figure 4.2.1 were chosen to deliberately coincide with the expected points at zero and π for V_{dd}. We can see that this fits easily within the maximum and minimum gradients quoted for the measurement error bars—providing a perfect (though often suspiciously good) match with the aforementioned theory.

The range of PC1 output waveforms observed is also in agreement with our earlier understanding (figure 3.1.1)—illustrating the transition from a continuously high output at π to a continuously low output at zero, through the diminishing time width of individual square-wave pulses.

Phase Comparator 2

The most prominent feature in the otherwise linear behaviour of figure 4.2.2 (the transfer characteristics for PC2) is its sudden output voltage shift, offsetting the trend line. This response cannot reasonably be attributed to poor observation, given the number of sampled points and relatively small reading errors found. The question we are left to face is: *Is this a fundamental property of a type two comparator?* Figure 3.1.5 (the theoretical result) does not give a clear indication of this either way.

Unlike PC1, which is the simplest possible phase comparator, PC2 consists of an arrangement of logic processes and operations. Crucially, PC2 differs from PC1 in that its output operates as a source and sink of current. This raises questions

concerning the presence and configuration of the load circuit, used to monitor PC2's output[25].

Nevertheless, the trend-line plotted in figure 4.2.2 consists of at least two distinct linear segments, separated by a narrow 'transition' region around the zero phase difference point. These two lines possess very similar (potentially identical) gradients of approximately -0.8 V rads^{-1}. It is interesting to note that (ignoring the trend-line offset) this is exactly half the predicted gradient value (of $10/2\pi \approx 1.6$) in figure 3.1.5[26]. The implications of this are once again not obvious.

We also observed that the average PC2 output voltage ranges from ≈8.8V to ≈2.9V—which, even with extrapolation using the trend-lines, does not coincide with V_{dd} or V_{ss} for a $\pm\pi$ phase difference. The third output condition (a high impedance off state) does however occur as expected at $\frac{1}{2}V_{dd}$, where the phase difference is zero.

The presence of dominant linear sections in figure 4.2.2, and the observed output waveforms, does nonetheless add weight to our earlier theoretical understand of the PC2 waveform responses (shown in figure 3.1.4).

Voltage-Controlled Oscillator Characterisation

4.4 Method: Voltage-Controlled Oscillator

The voltage-controlled oscillator was individually tested by applying a 0-10V variable input voltage to its input (VCO_{in}), and by monitoring the resultant square-wave output signal. Figure 4.4.1 (below) outlines the set-up used.

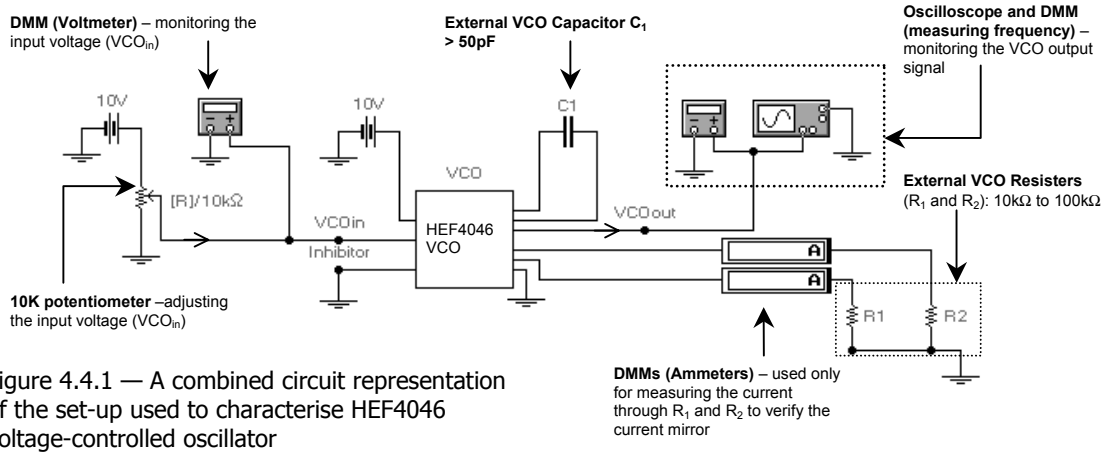


Figure 4.4.1 — A combined circuit representation of the set-up used to characterise HEF4046 voltage-controlled oscillator

In order to check the VCO current mirror circuit, the current through R_1 and R_2 was measured, with the current through C_1 determined by observing its oscilloscope trace—for R_1, R_2 = 100K and C_1 = 1000pF. The dependence of the oscillator output frequency range was then recorded for a variety of resistor and capacitor combinations: $10k\Omega \leq R_1 \leq \infty$, $10k\Omega \leq R_2 \leq \infty$, $100pF \leq C_1 \leq 3300pF$.

[25] Using a resistance other than 10kΩ between the load circuit potential divider and $PC2_{out}$, resulted in incoherent waveform distortions, observed on the oscilloscope trace. This raises the question as to whether or not this is indicative of a problem with the presence of a load circuit.
[26] A further observation is that the predicted PC2 transfer characteristics (as in figure 3.1.5) show a positive gradient, compared to the measured results (figure 4.2.2). This is purely a manifestation of the way in which the relative phase comparison was chosen.

4.5 Results: Voltage-Controlled Oscillator

Regardless of the external components tested, the output of the VCO was at all times a cleanly formed square wave, at a controlled single frequency.

Current mirror:

- Current through R_1 = 76.5µA ± 0.05µA
- Current through R_2 = 75.3µA ± 0.05µA

∴ The total current through the resistors **($I_{resistors}$) = 151.8µA ± 0.1µA** [27]

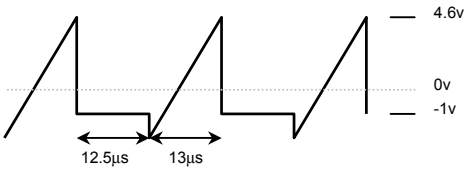


Figure 4.5.1 [Left] — The waveform observed on the oscilloscope at the $C1_a$ side of the VCO capacitor (identical to the $C1_b$ side which is π shifted)

Now from figure 4.5.1, we find that $\frac{dV}{dt} = 5x10^5\, Vs^{-1}$. As $I = c\frac{dV}{dt}$

∴ The total current through the capacitor **($I_{capacitor}$) = 500µA ± 50µA**

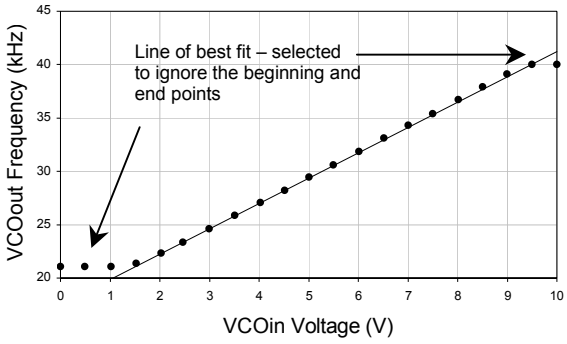
∴ **$I_{capacitor}$ is approximately 3 times greater than $I_{resistor}$**

Figure 4.5.2 (below) illustrates the relationship between the input voltage and the output frequency.

Figure 4.5.2 — A typical plot of the VCO_{in} control voltage against the resultant VCO_{out} square-wave output frequency.

R_1 = 100kΩ, R_2 = 100kΩ, C_1 = 1000pF – providing a VCO frequency range of ≈ 21 to 40 kHz for 0 to 10V

Line of best-fit gradient: $K_o \approx 1.53x10^4\, rads\, s^{-1}\, V^{-1}$



[28]

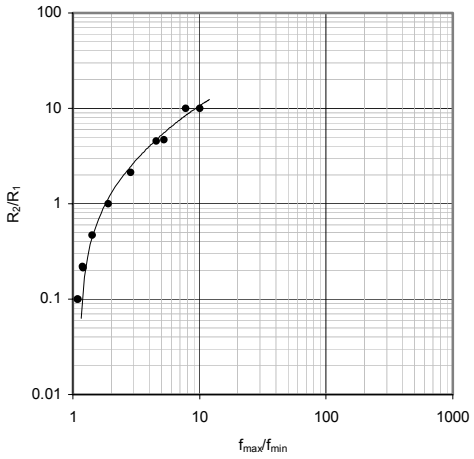
The dependence of the VCO frequency range obtained on R_1 and R_2, for a constant capacitance, is represented in figure 4.5.3 (below).

Figure 4.5.3 — A log-log plot of R2/R1 as a function of the ratio f_{max}/f_{min} (the maximum and minimum frequency produced by the VCO output for the particular external component selected)

Based on data obtained where C=1000pF. V_{dd} = 10V

Fitted with a 2nd order polynomial trend line

[Compare to figure 3.2.1]



[27] The current through VCO_{in} is negligible

[28] A typical VCO plot for all sensible external component choices. Note that error bars are insignificant on the chosen scale.

VCO component choice observations:

From the general data obtained[29], we find that R_2 purely controls the VCO offset from—shifting it away from outputting a zero frequency signal at 0V if an R_2 resistor is present (i.e. $R_2 \neq \infty$). The VCO frequency range is controlled by R_1 and C_1: reducing the range as $R_1 \rightarrow \infty$ or by increasing C_1.

4.6 Discussion: Voltage-Controlled Oscillator

It is interesting to note the mismatch between the current through the VCO resisters and the current through the VCO capacitor. Referring to figure 3.2.2, we can only conclude that the VCO's internal current mirror circuit is not perfect—assuming the circuit diagram shown in this figure is a realistic representation for the 4046.

Figure 4.5.2 illustrates the near-linear behaviour of the VCO, across the input voltage range—faltering only at the extremes. This slight imperfection remains trivial, as long as one keeps away from the ends of the range if a high degree of linearity is desired. Nevertheless, a VCO used in a phase-locked loop does not need to be particularly linear for the PLL to function properly. If, however, the VCO is found to be highly non-linear, it would result in the loop gain varying considerably with signal frequency—and consequently requiring improved loop stability.

By comparing figures 4.5.3 and 3.2.1 (the measured and expected plots of resistor ratio against frequency range ratio), we see that they are virtually indistinguishable—providing confirmation of the independent manufacturer's data. Clearly, the relationship shown in these log-log plots is not a straightforward one. The second order polynomial trend line added to figure 4.5.3 is not satisfactory, and does not extrapolate well compared with higher f_{max}/f_{min} values shown in figure 3.2.1.

Overall, the 4046 voltage-controlled oscillator appears to behave as expected, and is satisfactory for use in a complete phase-locked loop.

Basic Closed Phase-Locked Loop Operation

4.7 Method: PLL Operation

The complete phase-locked loop was constructed (as shown in figure 4.7.1 overleaf) and feed off an adjustable 50-100kHz buffered square wave signal source (into $SIGN_{in}$). This frequency range was matched by the choice of external VCO components[30] ($R_1 = 22k\Omega$, $R_2 = 47k\Omega$, $C = 1000pF$ ∴providing a VCO frequency range of ≈ 42kHz to 112kHz). The phase relationship between the input and output signals was therefore observed by varying the input frequency—using an oscilloscope and separate DMM frequency meters to monitor these waveforms at all times. Stability, capture characteristics, lock range, and harmonic locking were also tested and measured.

[29] The largest VCO frequency range tested was: 0 to 1088kHz with $R_1 = 10k\Omega$, $R_2 = \infty$, C_1=100pF
[30] These were selected given our previous VCO data gathered in section 4.5

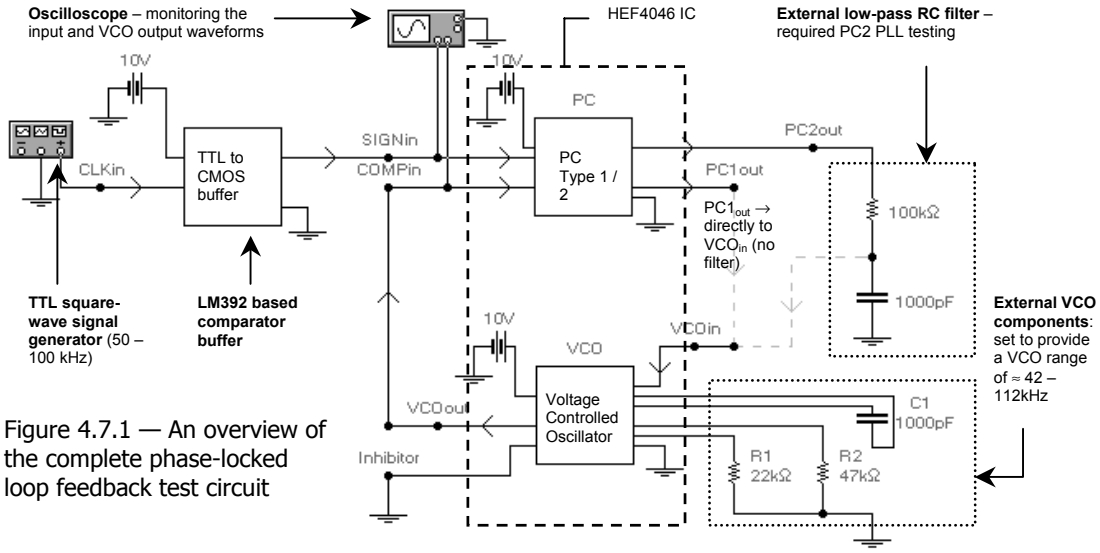


Figure 4.7.1 — An overview of the complete phase-locked loop feedback test circuit

4.8 Results: PLL Operation

With the VCO configured, as shown in figure 4.7.1, the resultant available output frequencies were measured as[31]:

f_{out} = 112.0 kHz at +10V f_{out} = 74.3 kHz at +5V f_{out} = 41.5 kHz at 0V

Phase Comparator 1 PLL (no filter):

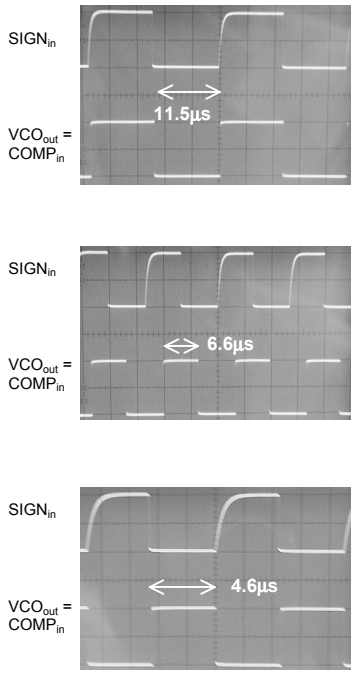


Figure 4.8.1 [above] — The PC1 PLL response to variation in external input frequency

Observations notes (PC1):

- With no external input signal, VCO_{out} frequency → 61.5 kHz ≈ f_o
- *Capture range* ($2f_c$)(from initially out of lock) ≈ 42.8 to 112.6 kHz ± 0.1 kHz
- *Lock range* ($2f_L$)(initially in lock) ≈ 42.8 to 112.6 kHz ± 0.1 kHz
- $\therefore f_c = f_L$ here
- PC1 was found to be stable across the whole of the lock/capture range
- PC1 was found to be able to lock-on harmonically

[31] A reading error of ± 0.05kHz applies to the values for f_{out}
[32] All three traces correspond to 10V/division vertically ∴ all the waveforms shown are 0-10V

For an input signal outside the range of the voltage-controlled oscillator's configured frequency range, it was possible for a PC1 PLL to achieve a harmonic phase-lock:

1) $SIGN_{in} \approx 127.3$ kHz $VCO_{out} \approx 84.9$ kHz ∴
Related by a factor of ≈ 3/2

2) $SIGN_{in} \approx 21.1$ kHz $VCO_{out} \approx 63.0$ kHz ∴
Related by a factor of ≈ 3

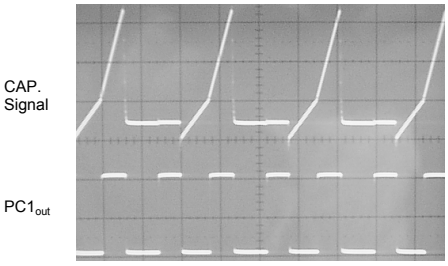


Figure 4.8.2 [left] — The signal on the VCO capacitor for the locked PC1 PLL, compared with the output of phase comparator 1

[Notice that the point at which the gradient of the capacitor signal increases, corresponds to a rising edge of $PC1_{out}$]

Phase Comparator 2 PLL (no filter):

With no filter present, the system appears to only lock at discrete frequencies, of no discernable pattern, within the range of the VCO.

Phase Comparator 2 PLL (with filter):

The PC2 PLL was found to only lock properly within the VCO range, in the presence of a filter[33]. Figure 4.8.3 (below) represents the basic LC and lead-lag LC filter tested with the PC2 PLL.

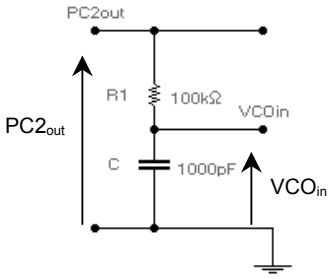
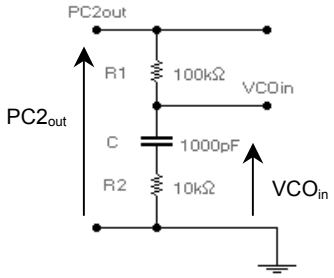


Figure 4.8.3 [Left] — A standard LC filter

[Right] – A lead-lag LC filter, which should provide improved PLL stability

Both of these filters were tested, and appeared to be indifferent with regards to PLL stability, lock or capture range.



Observation notes (PC2):

- With no external input signal, VCO_{out} frequency → 41.8kHz ≈ f_{min}
- When locked, the input signal and VCO output signal were found to be in phase at all times (∴ zero phase difference)
- PCP_{out} was observed to provide a high (+10V) output when PC2 was in lock
- *Capture range* $(2f_c)$(from initially out of lock) ≈ 42.0 to 110.0 kHz ± 0.1 kHz
- *Lock range* $(2f_L)$(initially in lock) ≈ 42.1 to 110.1 kHz ± 0.1 kHz
- ∴ $f_c = f_L$ here
- PC2 was never shown to harmonically lock for an input signal outside the frequency range of the VCO

[33] As detailed filter analysis was not included in this study, filter component choices were determined using a rule of thumb (RC ≈ τ), and was found by trial and improvement. This technique was used with all RC filters employed, in this and subsequent tests.

4.9 Discussion: PLL Operation

Overall, both phase comparators types one and two functioned as expected in a PLL system. Table 4.9.1 (below) summarises and compares these results to the intended design characteristics discussed earlier (table 3.3.1)[34].

Characteristic Tested	Phase Comparator 1 PLL	Phase Comparator 2 PLL
No input signal to the PLL at $SIGN_{in}$	The VCO in the PLL system adjusted to approximately the centre frequency (f_o) ☑	The VCO in the PLL system adjusted to approximately the minimum frequency (f_{min}) ☑
Phase difference between signals: $SIGN_{in}$ and $COMP_{in}$	The phase difference started at zero for $\approx f_{min}$, increasing to $\pi/2$ at $\approx f_o$, and reaching π at $\approx f_{max}$ ☑	Whilst in lock, the phase difference between the input and VCO signal remained zero at all times ☑
PLL locks onto harmonics of the central frequency (f_o)	Yes – harmonic phase locking was observed for an input signal outside the frequency range of the VCO ☑	No harmonic locking was observed at any time ☑
Rejection of input signal noise	Not tested directly	Not tested directly
Lock ($2f_L$) and capture ($2f_c$) frequency range	It was found that $f_c = f_L$ in the absence of an RC filter	The lock and capture range were found to be identical ($f_c = f_L$) ☑

There are several points of particular interest worth mentioning. Firstly, we have found that the free running frequency of the PC1 PLL (61.5kHz) is slightly lower than the *defined* central frequency (74.3kHz), f_o, where the input VCO voltage is $\frac{1}{2}V_{dd}$. If we assume that these should match, it would tend to suggest that the maximum voltage supplied to the input of the VCO is always lower than 10V when it functions as part of the PLL. Alternatively, of course, this result can be used to argue that a PC1 PLL does not adjust to its central frequency in the absence of an input signal. Either way, further information is needed to clarify this.

For both PC1 (in the absence of a filter) and PC2 (with an LC filter included), we find that the capture and lock range appear to be equivalent. These results appear to agree with the quoted specifications—however further testing of a PC1 PLL with an LC filter present is required to indicate whether the filter itself has the described effect of reducing the capture range.

From figure 3.3.2, concerning the behaviour of PC1 in a PLL, we can now confirm the linear relationship (discussed earlier), between the phase difference and the external input signal frequency—resulting in a phase difference of 90^o at the VCO's central frequency[35]. As mentioned before, this is an unsurprising result given the simple construction of a type one comparator. By contrast, PC2 is able to maintain a zero phase difference between the input and VCO produced signal. This difference

[34] ☑ Indicates that a definite agreement was found experimentally with the intended character
[35] The term "central frequency" and "free running frequency" have been used interchangeable in this report. However, in the event that they are not the same—we can define the central frequency to be the VCO's operating frequency with a $\frac{1}{2}V_{dd}$ input, and the free running frequency to be the VCO's output frequency in a PC1 PLL with no signal input.

between PC1 and PC2 is likely to be the dividing line for their use in meaningful practical applications.

PLL applications

4.10 Method: Frequency multiplication

A complete PLL with a lead-lag RC filter was used with a signal divider placed between the VCO and the PC comparator input, as outlined in figure 4.10.1 (below). The VCO component choices were selected to provide: f_{max} = 250kHz, f_o = 204.8kHz and f_{min} = 150kHz.

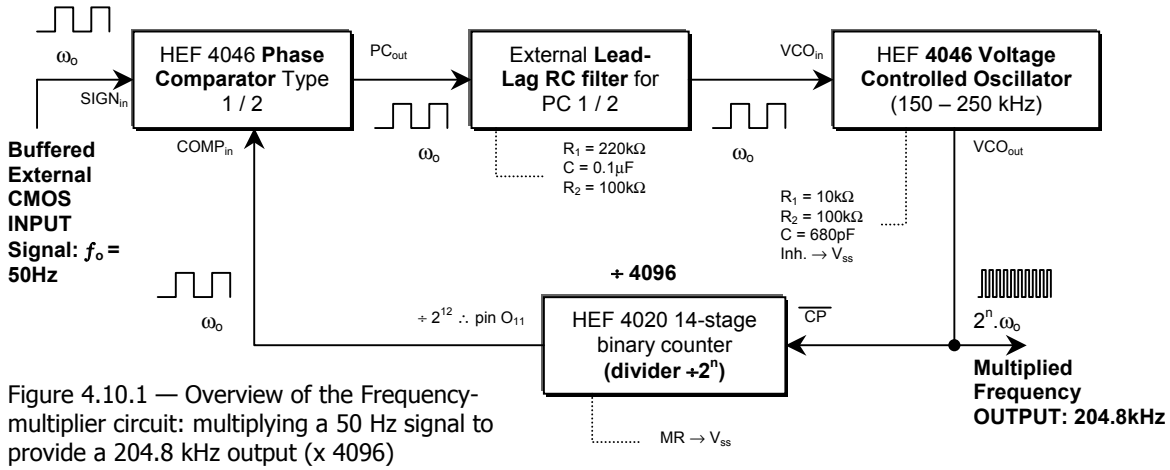


Figure 4.10.1 — Overview of the Frequency-multiplier circuit: multiplying a 50 Hz signal to provide a 204.8 kHz output (x 4096) [compare figure 3.0.2]

Both types of phase comparator were tested, observing the input and output waveforms using an oscilloscope and separate DMM frequency meters.

4.11 Results: Frequency multiplication

The multiplication factor provided by the PLL circuit was entirely dependent on chosen hard-wired division factor at the binary counter. A division of 2^{12} therefore provided a multiplication factor of 2^{12} (as long as multiplied frequency lied within the preset VCO range).

The circuit performed perfect frequency multiplication using phase comparator two—producing a clean square-wave output of exactly 204.8kHz from a 50Hz input[36].

Observations (PC2 PLL):

- For the VCO configuration quoted above, the multiplied output frequency rose stably up to a ceiling value of ≈ 228kHz—for any input > 50Hz
- Inputs between ≈ 25 - 50Hz resulted in an apparently stable output of as low as ≈ 99kHz—after the settling of some apparently damped harmonic oscillations in the output signal.

[36] As read using the DMM frequency meters

- For input signals < 25Hz, the output signal appeared to oscillate continuously—never achieving a stable output.
- With an input of 50Hz, $PC2_{out}$ always contained at least some square-wave pulses—even though $SIGN_{in}$ and $COMP_{in}$ appeared to be identical signals in frequency and phase.

By contrast, phase comparator one, could not produce a stable output for a 50Hz input from the multiplication circuit. It was, however, possible to obtain a metastable[37] output of ≈ 227kHz with an extremely narrow input range of ≈ 56Hz.

4.12 Discussion: Frequency Multiplication

The results form section 4.11, overwhelmingly indicates that a type-two phase comparator is the only suitable choice for a PLL frequency multiplier. The main reason for this difference between PC2 and PC1 is PC2's ability to provide an output that is in phase with the input signal over the entire VCO frequency range. Crucially, PC1 cannot do this (as we have already seen in section 4.8).

The PLL frequency multiplier works by causing the comparator to lock onto a corresponding sub-multiple of the VCO's oscillator frequency. Consequently, it is this technique that requires the two comparator input signals to be in-phase at all times.

It is also interesting to note that even when the PC2 PLL is in lock (with apparently identical signal and comparator inputs to the phase comparator), the output of PC2 does not remain constant at its high impedance off state. The reason for this is most likely that the filter capacitor is simply not a perfect voltage reservoir, and thus needs to be adjusted to maintain the VCO_{out} frequency.

In summary, PC2 is the only sensible comparator to use in frequency multiplication—by virtue of its zero phase difference character, inability to harmonically lock, and ability to provide a lock / capture range that is equal to the VCO's frequency range.

4.13 Method: FM demodulation

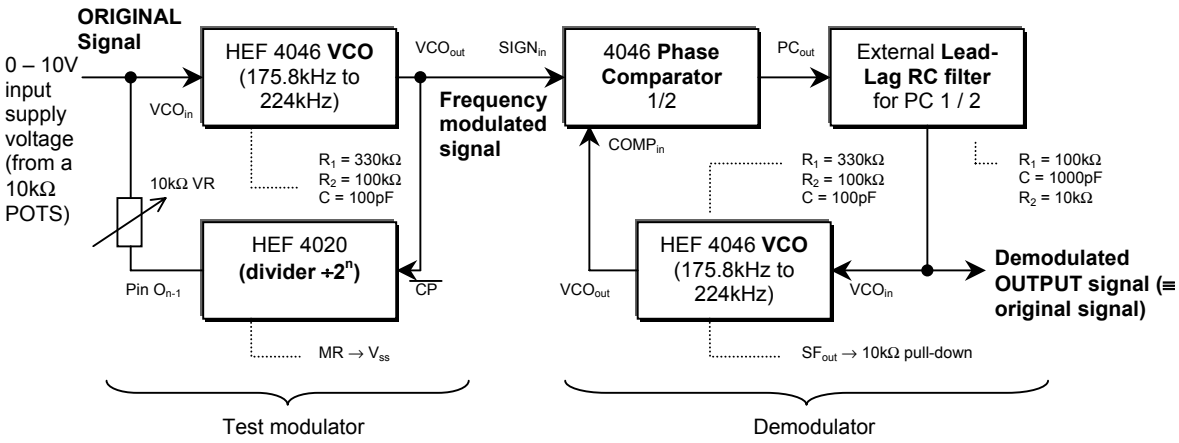


Figure 4.13.1 — Overview of the FM demodulation test circuit

[37] I.e. if the input was varied slightly away from 56Hz, the multiplied output signal became unstable

A complete modulation and demodulation test circuit was set-up, represented in figure 4.13.1 (previous page), in order to test it for a carrier signal of ≈ 200kHz modulated by a 10kHz signal. The demodulated signal was then monitored on an oscilloscope, from the demodulation VCO's SF_{out} output[38]—in order to avoid loading the external lead-lag RC PLL filter.

4.14 Results: FM demodulation

The test modular VCO was adjusted to provide a 200.0kHz carrier signal, with a modulated signal of 12.50kHz (using the divider setting of ÷ 2^4), as in figure 4.14.1.

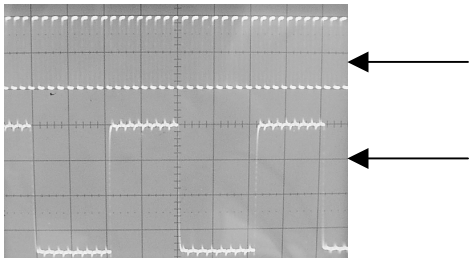


Figure 4.14.1 [Top trace] — The frequency modulated signal produced by VCO_{out}, consisting of ≈ 179 kHz and ≈ 208kHz squares waves

[Bottom trace] – The original 12.50kHz square-wave signal (to be modulated) at VCO_{in}

Using a modulator divider of ÷ 2^4

Figure 4.14.2 and 4.14.3 show the demodulated signal (taken from SF_{out}), compared to the original input signal for PC1 and PC2 respectively.

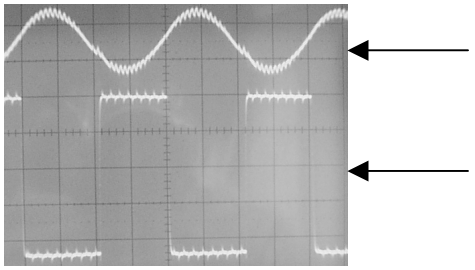


Figure 4.14.2 [Top trace] — PC1 demodulator circuit - The demodulated signal (measured from SF_{out}), with a period of ≈ 80μs

[Bottom trace] – The original 12.50kHz square-wave signal (to be modulated) at VCO_{in}

Using a modulator divider of ÷ 2^4

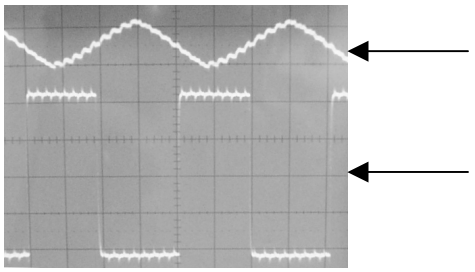


Figure 4.14.3 [Top trace] — PC2 demodulator circuit - The demodulated signal (measured from SF_{out}), with a period of ≈ 80μs

[Bottom trace] – The original 12.50kHz square-wave signal (to be modulated) at VCO_{in}

Using a modulator divider of ÷ 2^4

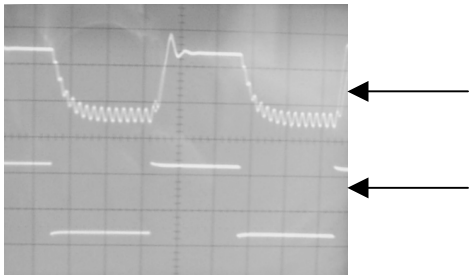


Figure 4.14.4 [Top trace] — PC1 demodulator circuit - The demodulated signal (measured from SF_{out}), with a period of ≈ 2.65ms

[Bottom trace] – The original 0.391 kHz square-wave signal (to be modulated) at VCO_{in}

Using a modulator divider of ÷ 2^9

[38] The signal from SF_{out} was passed through yet another lead-lag filter, before being viewed on the oscilloscope. This filter had: R_1 = 100kΩ, R_2 = 10kΩ and C = 100pF.

By using a larger division factor in the modulator test circuit, Figure 4.14.4 (previous page) shows a great improvement in the demodulated square-wave signal—for a much lower original signal frequency. A very similar result was also obtained using PC2 instead of PC1.

Observations:

- For both PC1 and PC2, a modulator division of $\div 2^4$ was the smallest possible that could be used, and still produce a demodulated signal from which the original frequency (if not waveform shape) could be identified.
- Both PC1 and PC2 otherwise required a modulator division of at least $\div 2^8$ to provide visually recognisable demodulated square waveform.
- For a modulator division of $\div 2^{11}$, the rising transient response of the demodulated waveforms produced was relatively clean—with similar transients periods from both PC1 and PC2 lasting around 0.4ms of a 5ms pulse.

4.15 Discussion: FM demodulation

Both phase comparators type one and two appear to be able to perform frequency demodulation in a satisfactory manner. Nevertheless, by examining the traces shown in figure 4.14.2 and 4.14.3, we can argue in favour of PC2. Although both the demodulated waveforms do not resemble a distinct square wave, by considering the Fourier components of a square waveform, we come to appreciate that a triangular PC2 output is closer than a sinusoidal PC1 output.

It is also interesting to consider the relationship between the quality of the demodulated waveform and the frequency of the original signal. For both comparators we found that a lower frequency original signal, translated into a better quality demodulated square-wave—compared to a higher frequency original signal. The exact reason for this is not entirely clear, but it is likely to be highly dependent upon the external lead-lag filter configuration used in the PLL decoder. In order to fully understand the behaviour we have observed, a detailed understanding of filter implementation and further experimental testing is required.

4.14 Clock Regeneration

Due to a lack of resources, clock regeneration was not systematically tested in the course of this investigation. However, preliminary experimentation suggested that a standard PLL loop could be satisfactorily used to produce a regular clock output from an intermittent series of inputs. Of the two phase comparators, PC2 appeared to have difficultly locking onto such an intermittent input—an attribute most likely associated to its slow response time. Conversely, PC1 appear to have no such difficulty (given its faster response rate), and is therefore likely to be the preferred phase comparator in this application. Evidently, further study into this application is required and recommended.

5.0 Conclusions

In the course of this investigation, we have been successful to a high degree in testing, characterising and verifying the separate functional components of the HEF 4046B phase-locked loop: phase comparators type one and two, and the voltage-controlled oscillator. We have thus been able to show beyond doubt that it behaves in accordance with theory (or at the very least, behaves in a predictable and reliable fashion).

Of critical importance is the potential to use a PLL in a practical application, such as those outlined in this report: frequency multiplication, FM demodulation and signal regeneration. In all three cases, we have found evidence to support the PLL as being a suitable candidate to achieve the desired results.

As neither the 4046 PLL IC nor its applications have been exhaustively tested—there is clearly much scope left for further research. A detailed understanding of the PLL filter configuration and stability analysis is urgently required for a more complete overview, and is therefore especially recommended for further study.

6.0 References

1. Newnes Electronic Circuits Pocket Book – Ray Marston – Volume Two – A Butterworth-Heinemann Book
2. The Art of Electronics – 2nd Edition – Paul Horowitz and Winfield Hill – Cambridge University Press
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4. Phase-Locked Loop Integrated Circuits – Dr J R A Cleaver – Cavendish Laboratory, Cambridge University