DATA SHEET

74F1763
Intelligent DRAM controller (IDC)

Product specification
Supersedes data of 1989 Nov 17
IC15 Data Handbook

1999 Jan 08

Philips
Semiconductors

PHILIPS

Intelligent DRAM controller (IDC) 74F1763

FEATURES

- DRAM signal timing generator
- Automatic refresh circuitry
- Selectable row address hold and $\overline{RAS}$ precharge times
- Facilitates page mode accesses
- Controls 1 MBit DRAMs
- Intelligent burst-mode refresh after page-mode access cycles

PRODUCT DESCRIPTION

The Philips Semiconductors Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the 74F1764 Dual Port Dynamic RAM Controller. It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{RAS}$ for the entire access cycle rather than the pre-defined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{RAS}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{DTACK}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{ALE}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after length page-mode access cycles. With a maximum clock frequency of 100 MHz, the F1763 is capable of controlling DRAM arrays with access times down to 40 nsec.

TYPE	f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

ORDERING INFORMATION

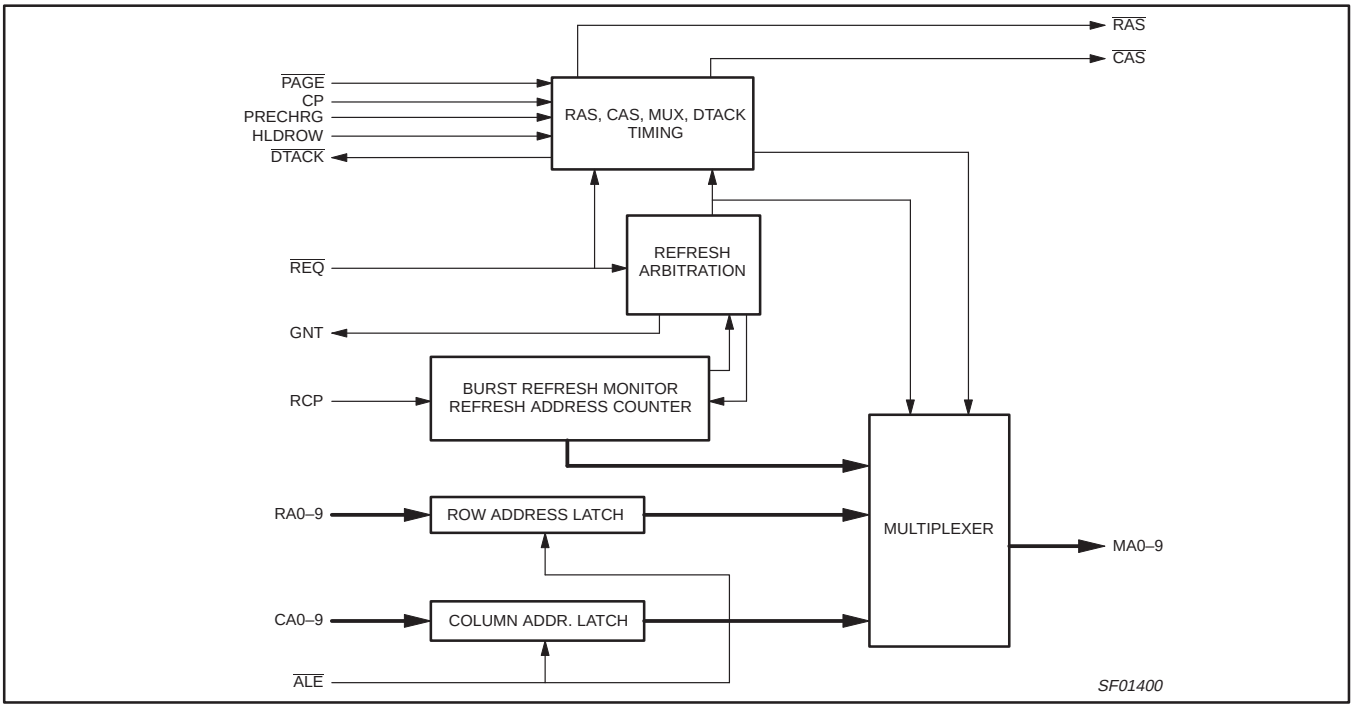
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C TO 70°C	PKG DWG #
48-pin Plastic DIP	N74F1763N	SOT240-1

INPUT AND OUTPUT LOADING FAN-OUT TABLE[NO TAG]

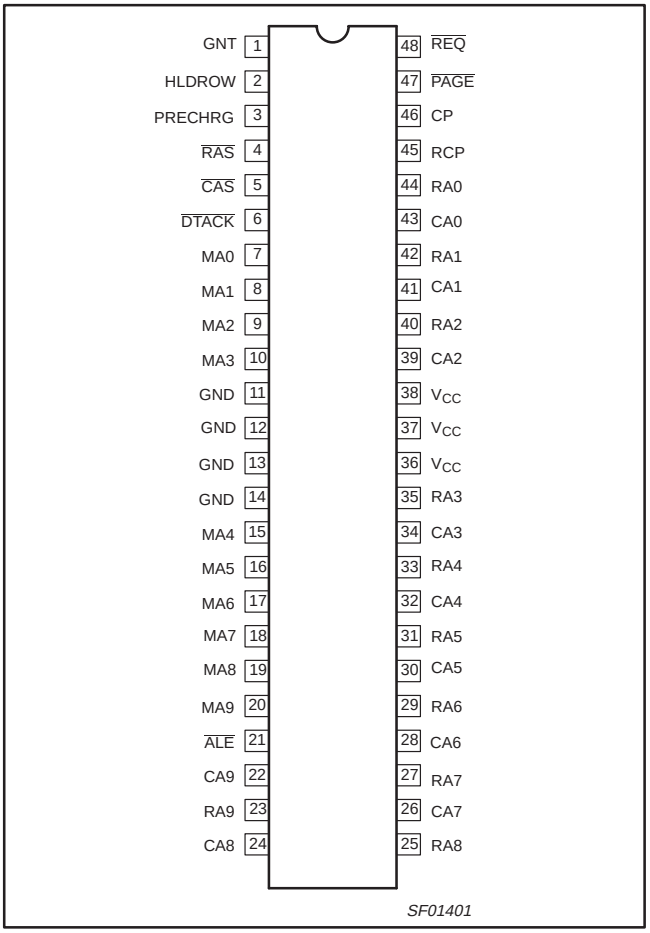
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request Input	1.0/1.0	20 μA/0.6 mA
CP	Clock Input	1.0/1.0	20 μA/0.6 mA
$\overline{PAGE}$	Page Mode Select Input	1.0/1.0	20 μA/0.6 mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20 μA/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 μA/0.6 mA
$\overline{DTACK}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 μA/0.6 mA
RA0–9	Row Address Inputs	1.0/1.0	20 μA/0.6 mA
CA0–9	Column Address Inputs	1.0/1.0	20 μA/0.6 mA
$\overline{ALE}$	Address Latch Enable Input	1.0/1.0	20 μA/0.6 mA
$\overline{RAS}$	Row Address Strobe Output	NA	35 mA/60 mA
$\overline{CAS}$	Column Address Strobe Output	NA	35 mA/60 mA
MA0–9	DRAM Address Outputs	NA	35 mA/60 mA

NOTES:
One (1.0) FAST Unit Load is defined as 20 μA in the HIGH state and 0.6 mA in the LOW state.
FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

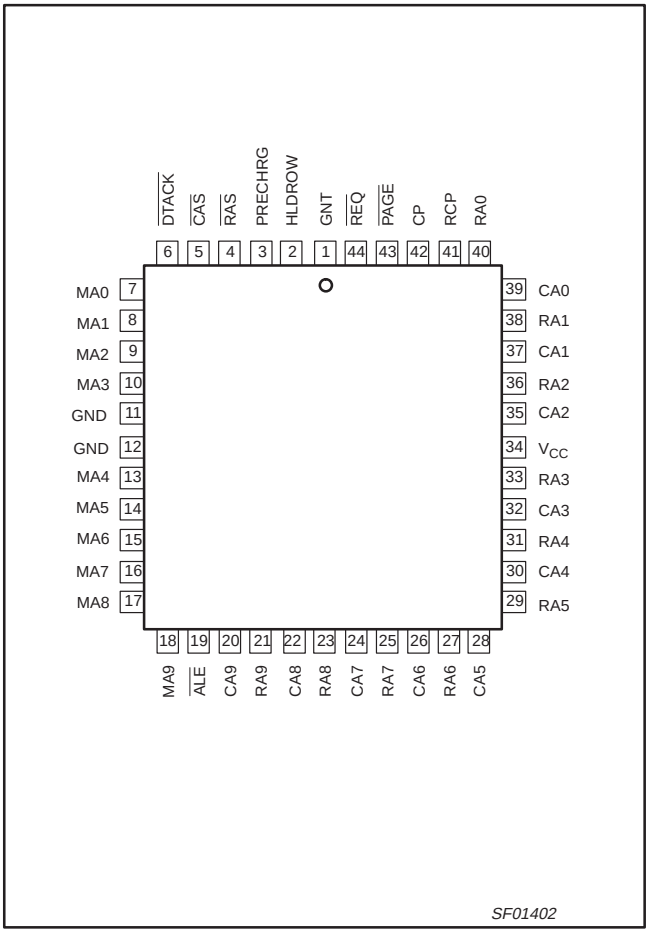
BLOCK DIAGRAM



DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS DIP	TYPE	NAME AND FUNCTION
$\overline{REQ}$	48	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
GNT	1	Output	Active High Grant output. When High indicates that a DRAM access (inactive during refresh) cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{PAGE}$	47	Input	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{RAS}$ asserted for as long as the $\overline{PAGE}$ input is Low and $\overline{REQ}$ is asserted Low.
HLDROW	2	Input	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{RAS}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle after $\overline{RAS}$ is asserted.
PRECHRG	3	Input	$\overline{RAS}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	Input	Clock input. Used by the Controller for all timing and arbitration functions.
RCP	45	Input	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{DTACK}$	6	Output	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{REQ}$ input and asserted four clock cycles after the assertion of $\overline{RAS}$, 3-stated when $\overline{REQ}$ goes High.
RA0–9	44, 42, 40, 35, 33, 31, 29, 27, 25, 23	Inputs	Row Address inputs.
CA0–9	43, 41, 39, 34, 32, 30, 28, 26, 24, 22	Inputs	Column Address inputs. Propagated to the MA0–9 outputs 1 CP clock cycle after $\overline{RAS}$ is asserted, if HLDROW = 0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{RAS}$	4	Output	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle regardless of the $\overline{PAGE}$ input. Also asserted for four clock cycles during processor access if the $\overline{PAGE}$ input is High. If $\overline{PAGE}$ is Low, $\overline{RAS}$ is negated upon negation of $\overline{PAGE}$ or $\overline{REQ}$, whichever occurs first.
$\overline{CAS}$	5	Output	Active Low Column Address Strobe. Always asserted 1.5 CP clock cycles after the assertion of $\overline{RAS}$. Negated upon negation of $\overline{REQ}$. HLDROW input pin does not affect $\overline{RAS}$ to $\overline{CAS}$ timing.
MA0–9	7–10, 15–20	Output	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{ALE}$	21	Input	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A High level will latch the RA0–9 and CA0–9 inputs.
V_{CC}	36–38		+5V ±10% Supply voltage.
GND	11–14		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with most signal timing being a function of the CP input clock.

Arbitration

Once the DRAM's $\overline{RAS}$ precharge time has been satisfied, the $\overline{REQ}$ input is sampled on each rising edge of the CP clock and an internally generated refresh request is sampled on each falling edge of the same clock. When only one of these requests is sampled as active the appropriate memory cycle will begin immediately. For a memory access cycle this will be indicated by GNT and $\overline{RAS}$ outputs both being asserted and for a refresh cycle by multiplexing refresh address to the MA0–9 outputs and subsequent assertion of $\overline{RAS}$ after 1/2CP clock cycle. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated $\overline{RAS}$ precharge time.

Memory access

The row (RA0–9) and column (CA0–9) address inputs are latched when $\overline{ALE}$ input is High. When $\overline{ALE}$ is Low the input addresses propagate directly to the outputs. When GNT and $\overline{RAS}$ are asserted, after a $\overline{REQ}$ has been sampled the RA0–9 address inputs will have already propagated to the MA0–9 outputs for the row address. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the column address (CA0–9) inputs are propagated to the MA0–9 outputs. $\overline{CAS}$ is always asserted one and one-half CP clock cycles after $\overline{RAS}$ is asserted. If the $\overline{PAGE}$ input is High, $\overline{RAS}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{DTACK}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs until the $\overline{REQ}$ input is negated (see timing waveforms).

Row address hold times

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{RAS}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{RAS}$ is asserted.

$\overline{RAS}$ precharge timing

In order to meet the $\overline{RAS}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{RAS}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{RAS}$, depending on the state of the PRECHRG input. If the PRECHRG input is Low, $\overline{RAS}$ remains High for at least 4 CP clock cycles. If the PRECHRG input is High $\overline{RAS}$ remains High for at least 3 CP clock cycles.

Refresh timing

The refresh address counter wakes-up in an all 1's state and is an up counter. The refresh clock (RCP) is internally divided down by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and servicing any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{RAS}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{PAGE}$ input as shown in the timing waveforms. In this mode, the controller does not automatically negate $\overline{RAS}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{CAS}$ output can be gated on and off while changing the column address inputs to the controller, which will propagate to the MA_0–MA_9 address outputs and provide a new column address. This is only useful if the $\overline{ALE}$ input is Low, enabling the user to charge addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Philips Semiconductors application note AN218. The driving characteristics of the 74F1763 are the same as those of the 74F765 shown in the application note.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current[1]			–15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15 mA	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
			I_{OH2}[3] = –35 mA	±5% V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24 mA	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60 mA	±5% V_{CC}		0.35	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{OS}	Output current[5]	V_{CC} = MAX, V_O = 2.25V			–100		–225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX					220	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is transient current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is transient current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $RL = 70\Omega$		
			MIN	TYP	MAX	MIN	MAX	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		4	2		4		ns
8	$\overline{REQ}$ High hold time after CP(↑)[1]		0			0		ns
9	$\overline{REQ}$ High pulse width[2]		1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	ns
10	Propagation delay CP(↑) to GNT High		8.5	11	13.5	8.5	15.5	ns
11	Propagation delay $\overline{REQ}$(↑) to GNT Low		8.5	10.5	13	8.5	14	ns
12	$\overline{ALE}$ pulse width Low		4	1		4		ns
13	RA0–9, CA0–9 High or Low setup to $\overline{ALE}$(↑)		2	0		2		ns
14	ALE(↑) to RA0–9, CA0–9 High or Low hold		1	0		1		ns
15	Propagation delay RA0–9, CA0–9 High or Low to MA0–9[3]	$\overline{ALE}$ Low	4	7.5	11	4	14	ns
16	Propagation delay $\overline{ALE}$(↓) to MA0–9		5.5	8.5	13	5.5	15	ns
17	Propagation delay CP(↑) to $\overline{RAS}$(↓)		8.5	10.5	12.5	8.5	14	ns
18	$\overline{RAS}$(↓) to MA0–9 (column address) skew	HLDROW = 1	1/2tcp – 2	1/2tcp + 2	1/2tcp + 5.5	1/2tcp – 2.5	1/2tcp + 7	ns
19	$\overline{RAS}$(↓) to MA0–9 (column address) skew	HLDROW = 0	1tcp – 2	1tcp + 2	1tcp + 5.5	1tcp – 2.5	1tcp + 7	ns
20	$\overline{RAS}$(↓) to $\overline{RAS}$(↑) skew	PAGE = 1	4tcp + 1.5	4tcp + 3.5	4tcp + 6	4tcp + 1	4tcp + 6.5	ns
21	Propagation delay CP(↑) to $\overline{RAS}$(↑)		12	14	16.5	12	18.5	ns
22	Propagation delay REQ(↑) to RAS(↑)[4]		14.5	17.5	20	14	24	ns
23	Propagation delay CP(↓) to $\overline{CAS}$(↓)		6	8	10	6	11	ns
24	Propagation delay $\overline{PAGE}$(↑) to $\overline{RAS}$(↑)[4]		10	12.5	15	10	17	ns
25	$\overline{RAS}$(↓) to $\overline{CAS}$(↓) skew		1.5tcp–4.5	1.5tcp–2.5	1.5tcp–0.5	1.5tcp–5.5	1.5tcp	ns
26	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		10	12	15	10	17	ns
27	MA0–9 (column address) to $\overline{CAS}$(↓) skew		1tcp – 8	1tcp – 4	1tcp – 0.5	1tcp – 9	1tcp – 0.5	ns
28	MA0–9 (column address) to $\overline{CAS}$(↓) skew	HLDROW = 0	1/2tcp – 8	1/2tcp – 4	1/2tcp – 0.5	1/2tcp – 9	1/2tcp – 0.5	ns
29	Set-up time $\overline{PAGE}$(↓) to CP(↑)		2			2		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ TO $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ RL = 70Ω		
			MIN	TYP	MAX	MIN	MAX	
30	Propagation delay $\overline{REQ}$(↓) to $\overline{DTACK}$(↑)		6	8	11.5	6	12	ns
31	Propagation delay CP(↑) to $\overline{DTACK}$(↓)		7.5	9.5	12	7.5	13	ns
32	Propagation delay $\overline{REQ}$(↑) to $\overline{DTACK}$ (3-state)		9	12	13	9	15.5	ns
33	MA0–9 (refresh address) to $\overline{RAS}$(↓) skew		1/2tcp – 5			1/2tcp – 6.5		ns
34	$\overline{RAS}$(↓) to MA0–9 (refresh address) skew		1tcp – 2			1tcp – 2.5		ns
35	RAS(↑) to RAS(↓) skew (precharge)	PRECHRG = 0	4tcp – 6	4tcp – 3.5	4tcp – 1.5	4tcp – 6.5	4tcp – 6.5	ns
36	RAS(↑) to RAS(↓) skew (precharge)	PRECHRG = 1	3tcp – 6	3tcp – 3.5	3tcp – 1.5	3tcp + 1	3tcp – 6.5	ns

NOTES:
1. $\overline{REQ}$ High hold means that, if $\overline{REQ}$ is High at the rising clock edge, it is guaranteed that the $\overline{REQ}$ input was not sampled as Low.
2. A 50% duty cycle clock is recommended. If the duty cycle of the clock is not 50%, $\overline{REQ}$ should be held high for enough time such that a falling CP clock edge samples $\overline{REQ}$ as High. This is to ensure that refresh cycles don't get locked-up.
3. When $\overline{ALE}$ is Low, the address input latches are in the transparent mode and therefore any changes in the address inputs will be propagated to the MA0–9 outputs. Figure 2 illustrates RA0–9 inputs propagating to the MA0–9 outputs, but later in the cycle, if $\overline{ALE}$ is still Low when the CA0–9 inputs are multiplexed to the MA0–9 outputs the CA0–9 inputs will be in the transparent mode.
4. If $\overline{PAGE}$ is High and $\overline{REQ}$ is Low, $\overline{RAS}$ is automatically negated after approximately 4 CP clock cycles. If $\overline{PAGE}$ is Low and $\overline{REQ}$ is also Low, $\overline{RAS}$ will be negated when $\overline{PAGE}$ goes High. $\overline{RAS}$ will always be negated when $\overline{REQ}$ goes High regardless of the state of $\overline{PAGE}$ input.

TIMING DIAGRAMS

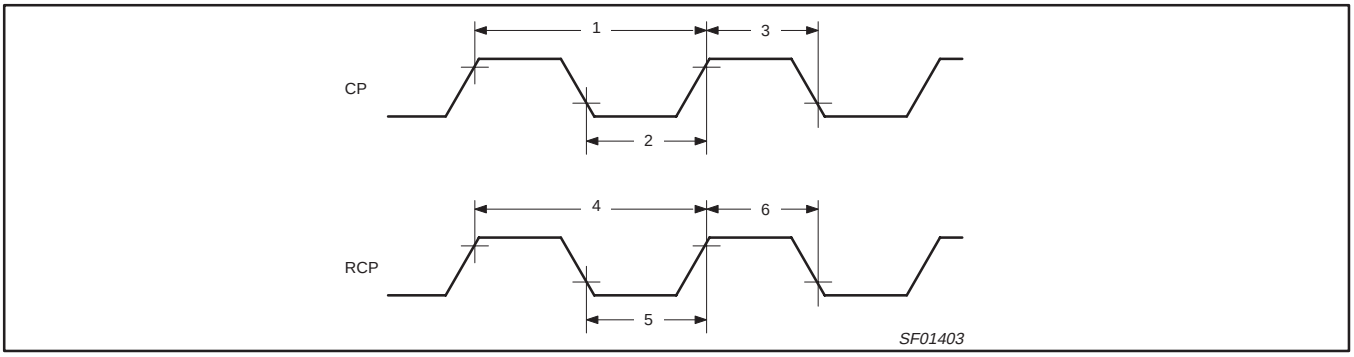
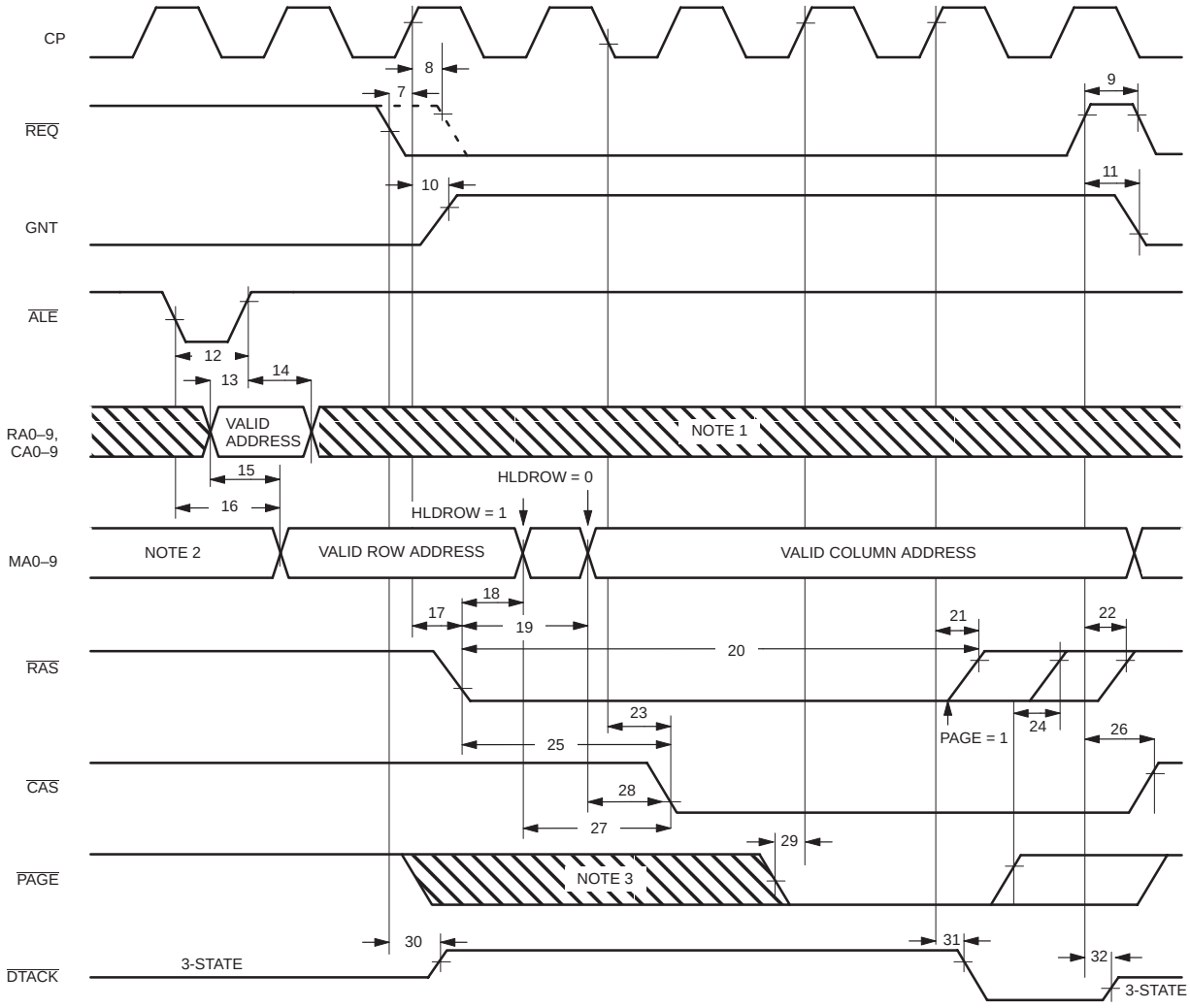


Figure 1. Clock cycle timing

TIMING DIAGRAMS (Continued)

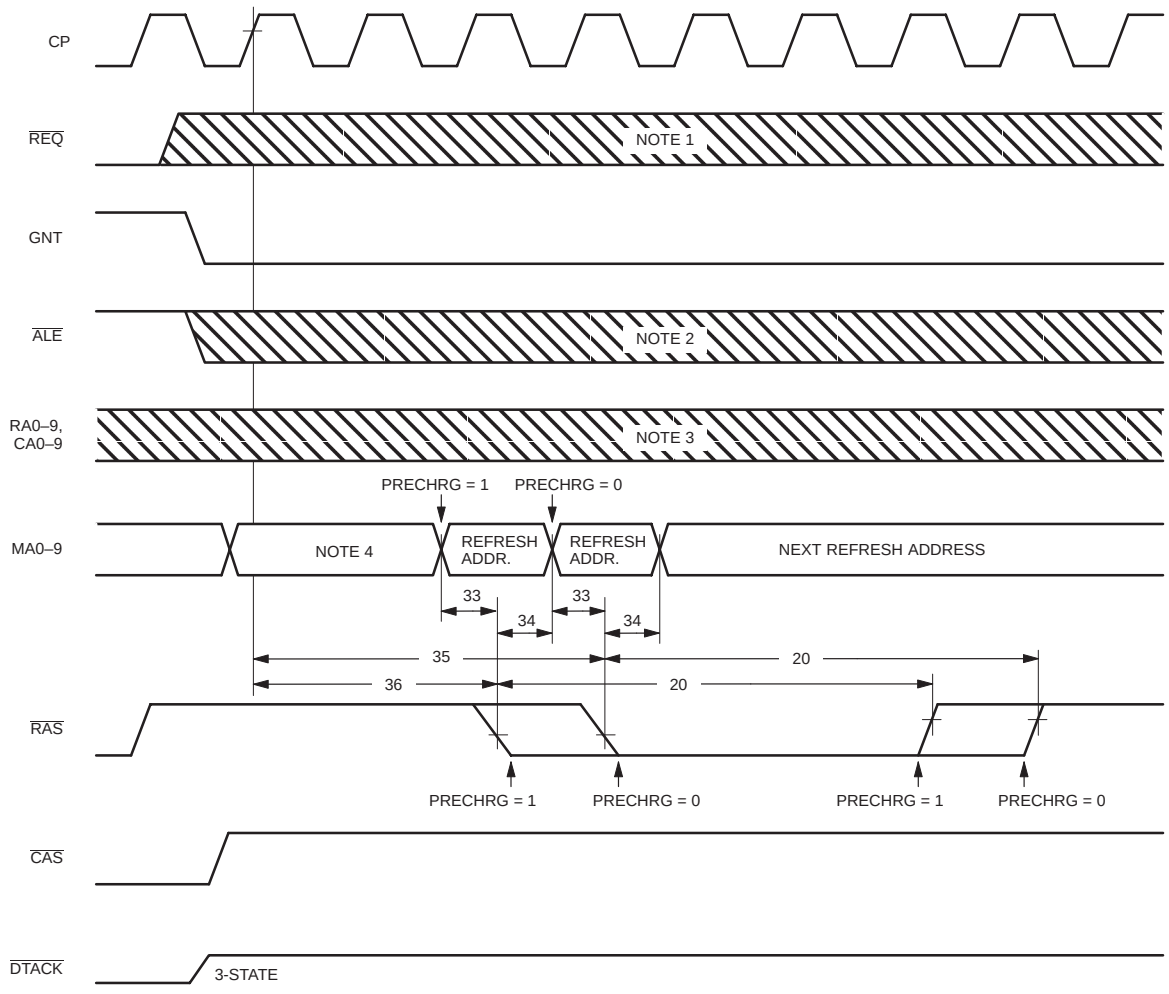


NOTE 1: If the RA0–9 and CA0–9 address inputs are not latched, RA0–9 inputs should remain valid until row address hold time is met and CA0–9 inputs should remain valid until column address hold time is met.
NOTE 2: MA0–9 outputs will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device.
NOTE 3: $\overline{\text{PAGE}}$ input may be asserted anytime before this rising clock edge in order to hold $\overline{\text{RAS}}$ low.

SF01404

Figure 2. Memory access cycle timing

TIMING DIAGRAMS (Continued)

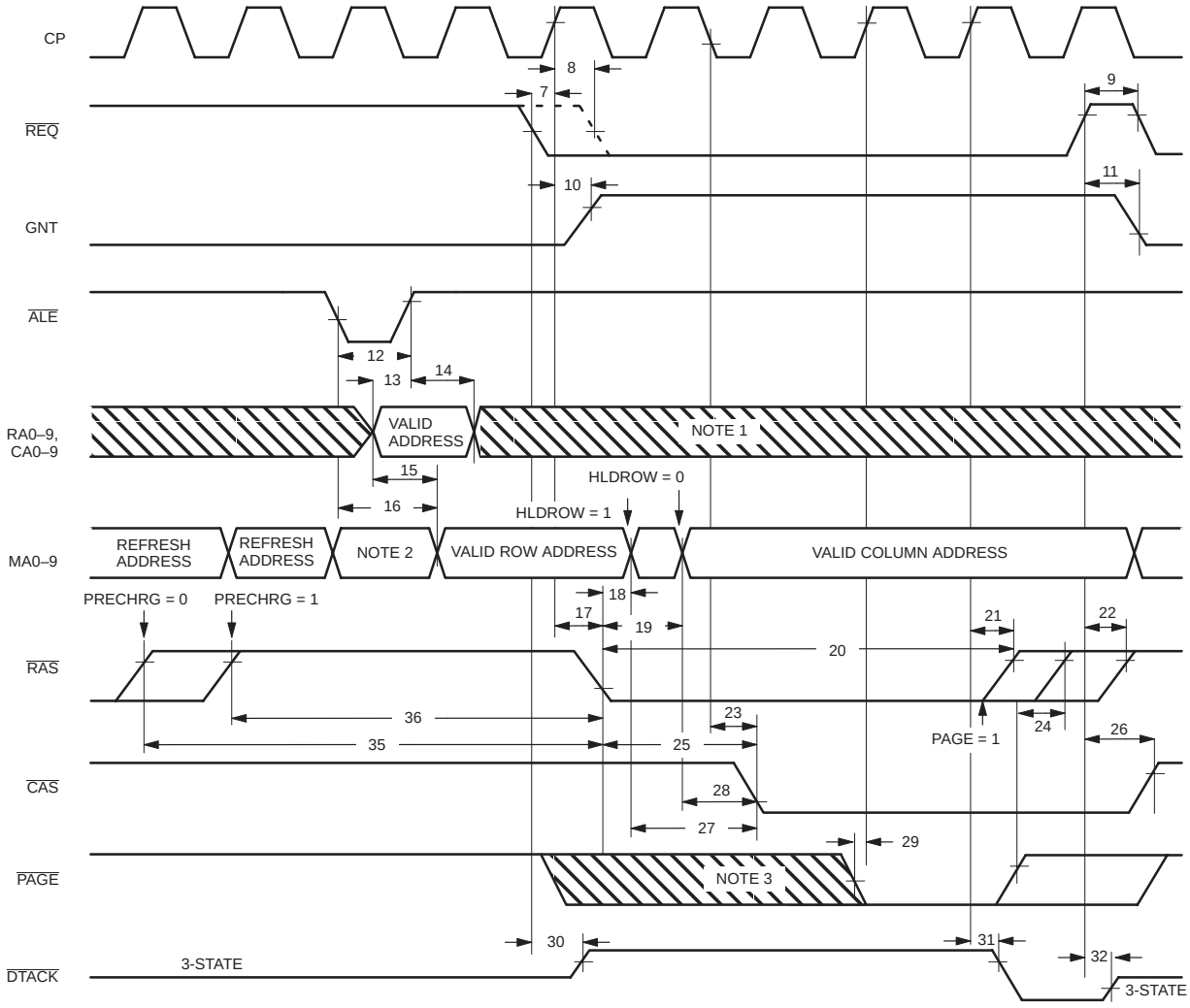


NOTE 1: REQ input is a don't care during a memory refresh cycle. If REQ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, following the refresh cycle and its associated RAS precharge time (see Figure 4).
NOTE 2: RA0–9 and CA0–9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.
NOTE 3: RA0–9 and CA0–9 if in the transparent mode do not propogate to the MA0–9 outputs during a refresh cycle.
NOTE 4: MA0–9 output will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device.

SF01405

Figure 3. Refresh cycle timing following a memory access cycle

TIMING DIAGRAMS (Continued)



NOTE 1: If the RA0–9 and CA0–9 address inputs are not latched, RA0–9 inputs should remain valid until row address hold time is met and CA0–9 inputs should remain valid until column address hold time is met.
NOTE 2: MA0–9 outputs will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device.
NOTE 3: $\overline{\text{PAGE}}$ input may be asserted anytime before this rising clock edge in order to hold $\overline{\text{RAS}}$ low.

SF01406

Figure 4. Memory access cycle timing following a refresh cycle

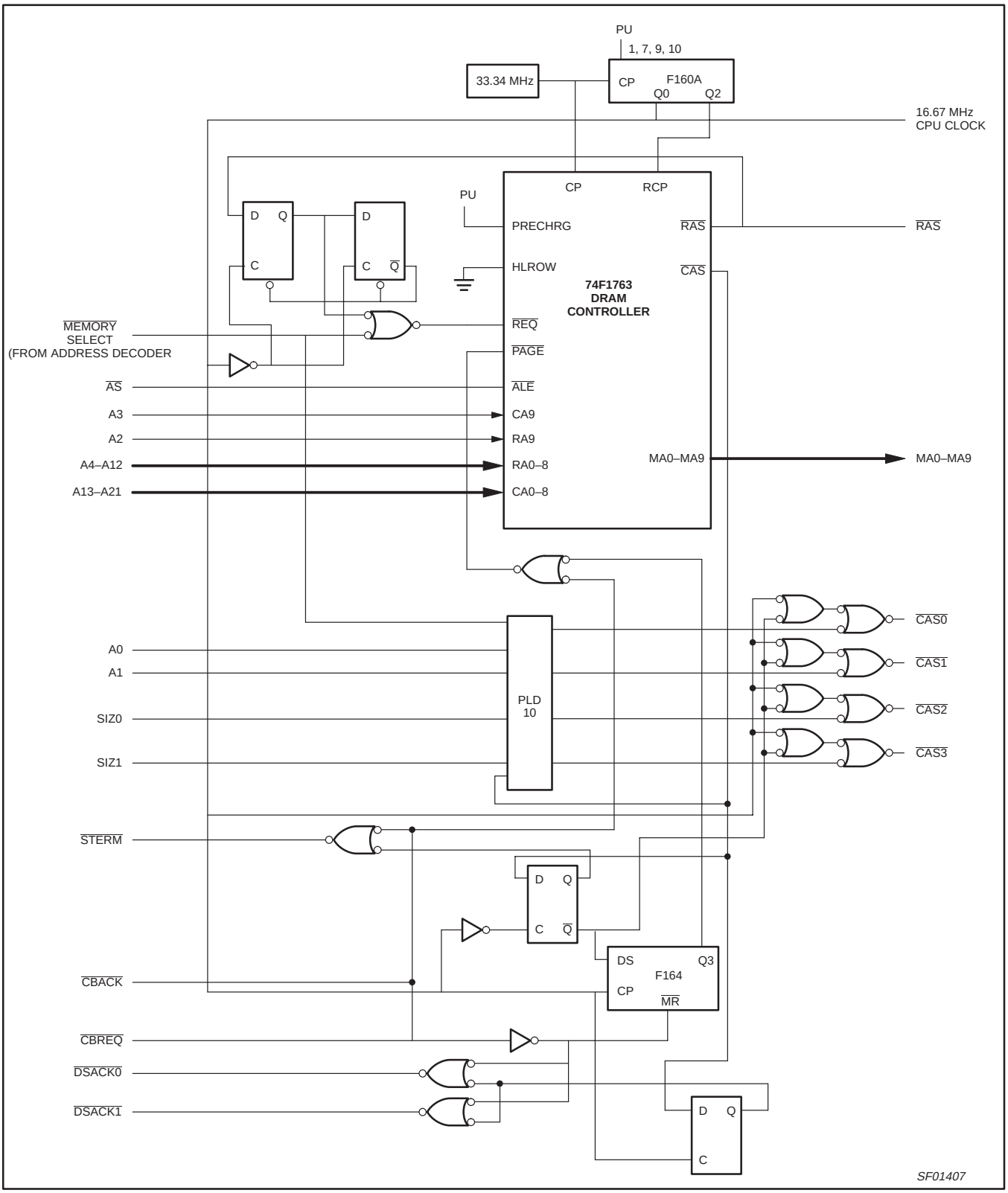
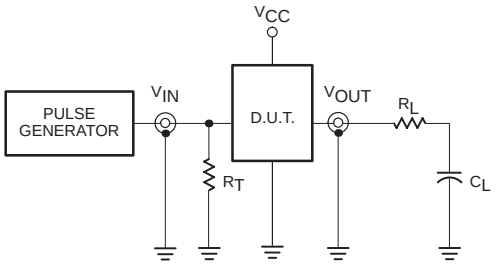
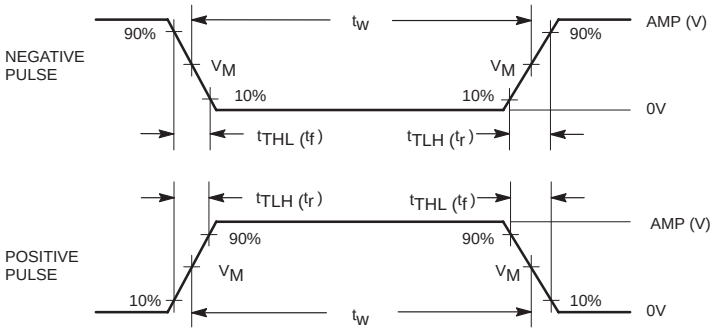


Figure 5. 16.67 MHz 68030 interface with 74F1763 for cache burst mode support using 4Mbytes of 100nsec. nibble-mode DRAMs (Four 32 bit words read to or written from cache in only clock cycles

TEST CIRCUIT AND WAVEFORMS



Test Circuit Simulating RAM Boards



DEFINITIONS:

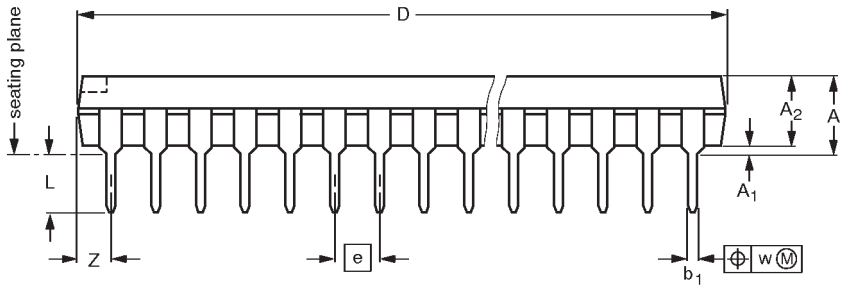
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

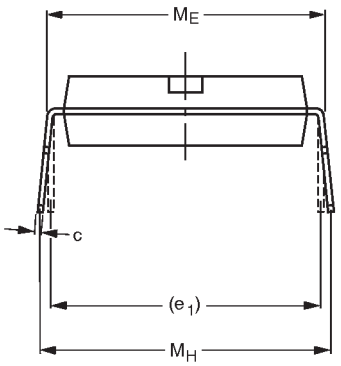
Input Pulse Definition

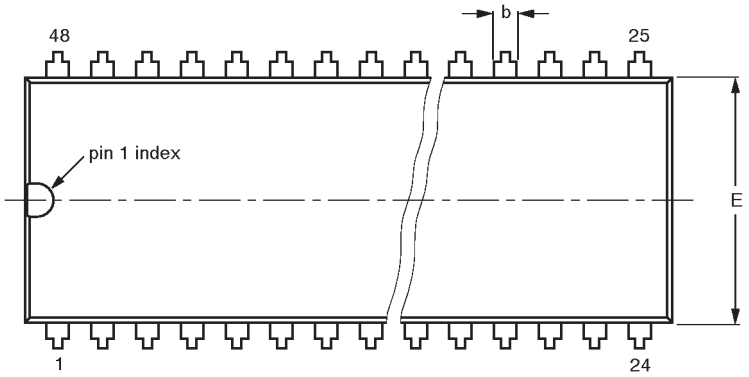
Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

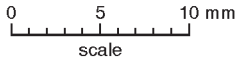
SF01408

DIP48: plastic dual in-line package; 48 leads (600 mil) SOT240-1









DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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