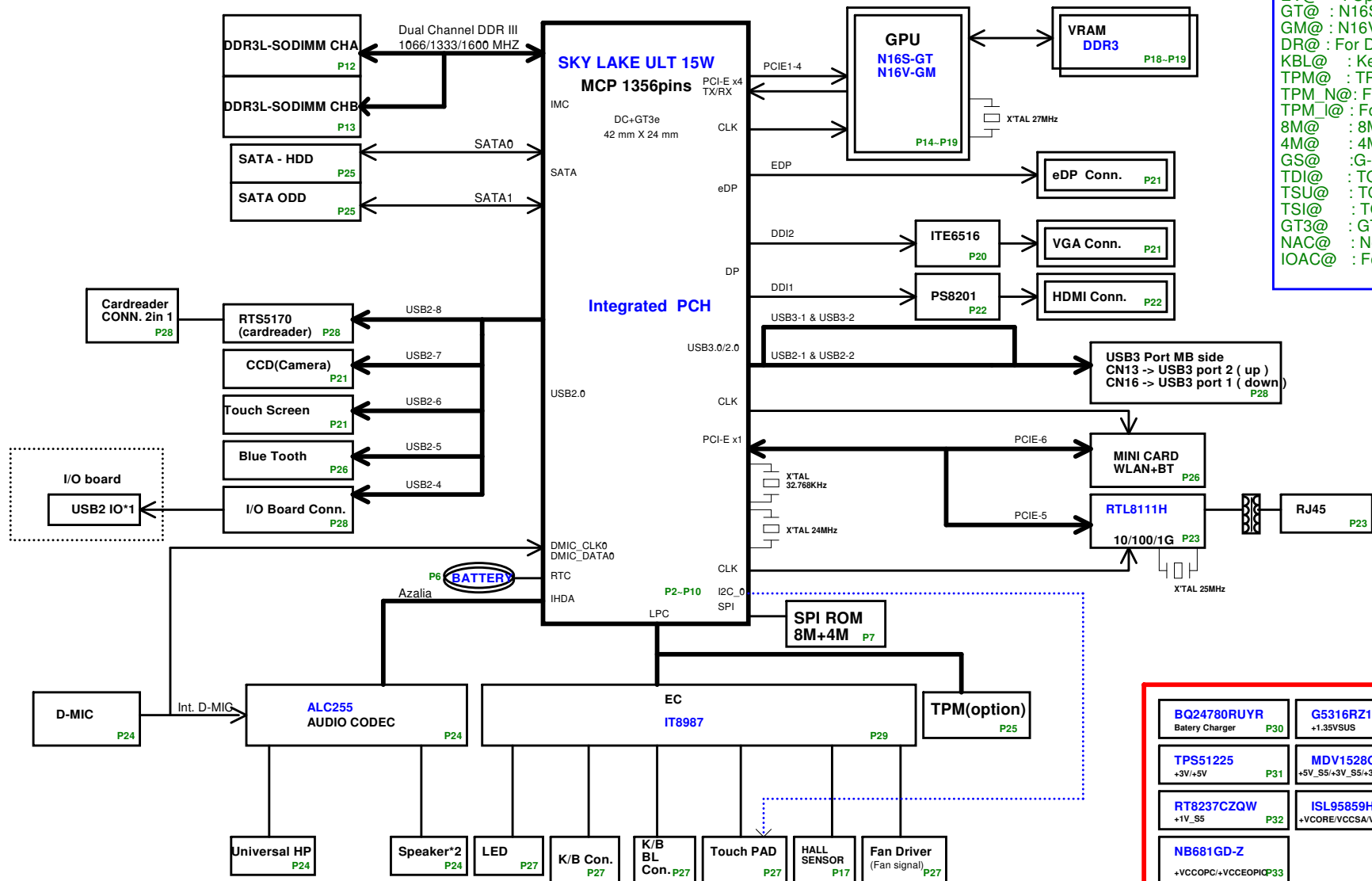


Zoro SL (ZRW) SKL ULT SYSTEM BLOCK DIAGRAM

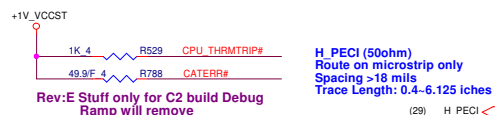
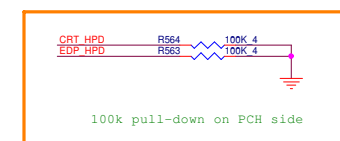
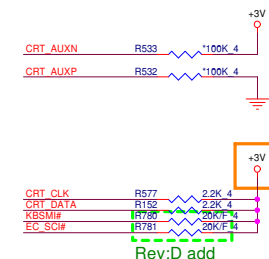
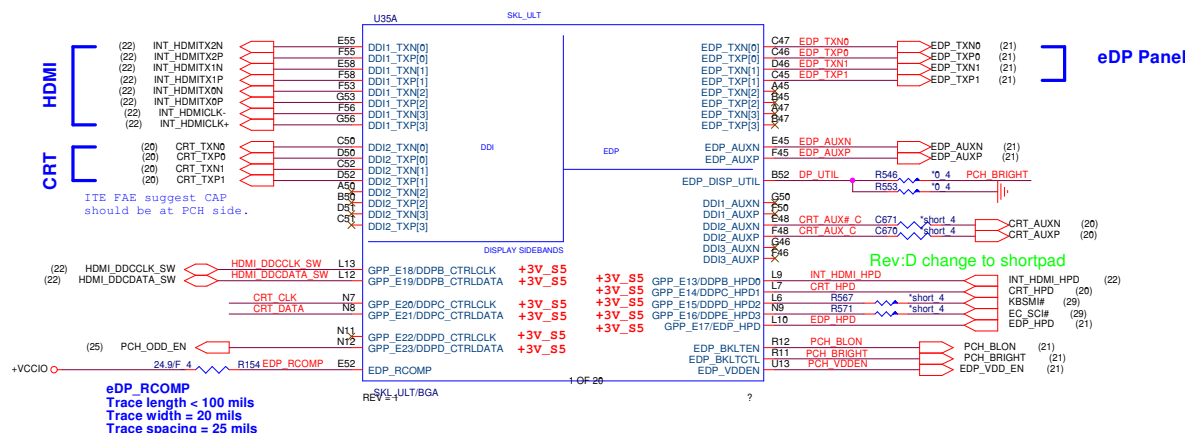


BOM

IV@ : iGPU
 EV@ : Optimus
 GT@ : N16S-GT / GC6
 GM@ : N16V-GM / WO GC6
 DR@ : For Dual Rank (VRAM 8 pcs)
 KBL@ : Keyboard backlight
 TPM@ : TPM
 TPM_N@ : For TPM 2.0
 TPM_I@ : For TPM 1.2
 8M@ : 8M FLASH ROM
 4M@ : 4M FLASH ROM
 GS@ : G-SENSOR
 TDI@ : TOUCH PAD I2C
 TSU@ : TOUCH SCREEN USB
 TSI@ : TOUCH SCREEN I2C
 GT3@ : GT3 CPU
 NAC@ : Non IOAC
 IOAC@ : For IOAC

BQ24780RUYR Battery Charger P30	G5316RZ1D +1.35VSUS P35	Thermal Protection Discharger P40
TPS51225 +3V/+5V P31	MDV1528Q +5V_S5/+3V_S5/+3V/+5V P31	UP1658RQKF +VGPU_CORE P41
RT8237CZQW +1V_S5 P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P38	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P42
NB681GD-Z +VCCOPC/+VCCOPIOP33		

Skylake ULT (DISPLAY, eDP)



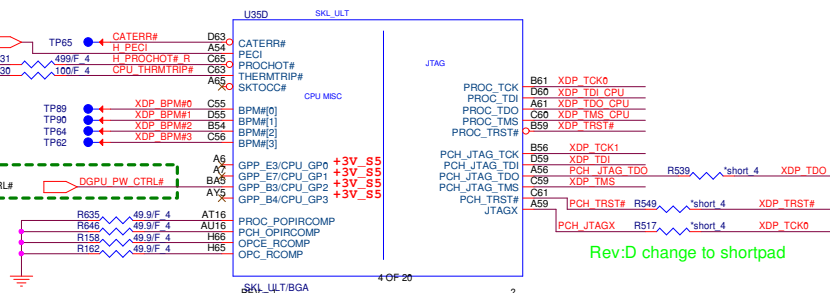
(29,30,36) H_PROCHOT# H_PROCHOT# R5
Avoid 125Mhz THRMTRIP# R5



BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

(4) DGPU_PW.

SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils



Rev:D change to shortpad

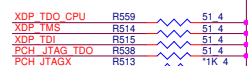
If use Intel DCI USB 3.0 fixture need to short
 1. XDP_TDO <=> XDP_TDO_CPU
 2. XDP_TDI <=> XDP_TDI_CPU
 3. XDP_TMS <=> XDP_TMS_CPU

Rev:F a

PCH JTAG
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

TCK,TMS
Trace Length < 9000mils

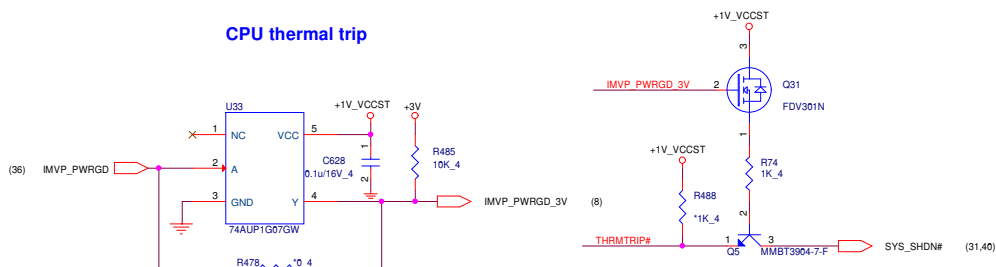
Change to +1V_VCCST 11/6

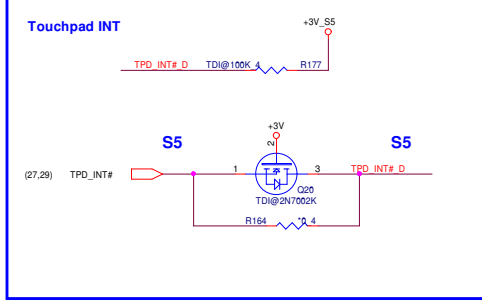








2/16
XDP_TCK1,XDP_TMS
don't need pull up or pull down

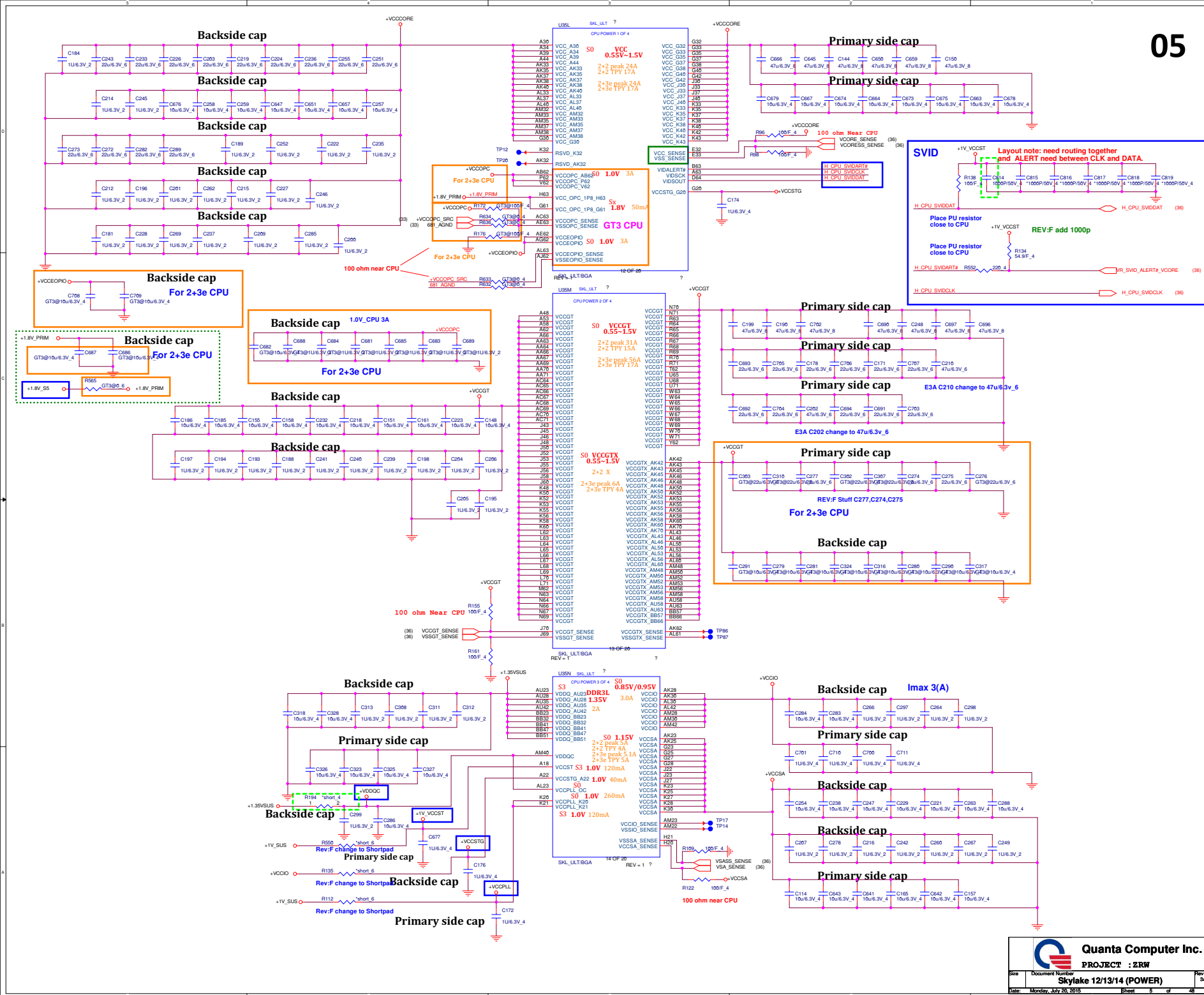
5/29 XDP TCK0 R558 Stuff

CPU thermal trip





Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V 
GPP_B18 (GSPi0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V 
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS(iPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_S5 
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V 
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal 
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	



dGPU PEG4

LAN

WIFI

HDD

ODD

N16S VGA

LAN

Rev:D change to shortpad

Rev:D add for EC reset RTC

1V power plane
0.71 checklist p14

MB USB3.0 CN16 (Charger IC) Down

MB USB3.0 CN13 -> Up

MB USB3.0 CN16 (Charger IC) Down

MB USB3.0 CN13 -> Up

DB USB2.0

BT

Touch Screen

CCD

Card reader

USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

MB U3
DB U2

PCH PU/PD

Add SSD ID 1/14

High is SSD , Low is ODD

Skylake-U used 24 MHz (50 Ohm ESR) XTAL

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

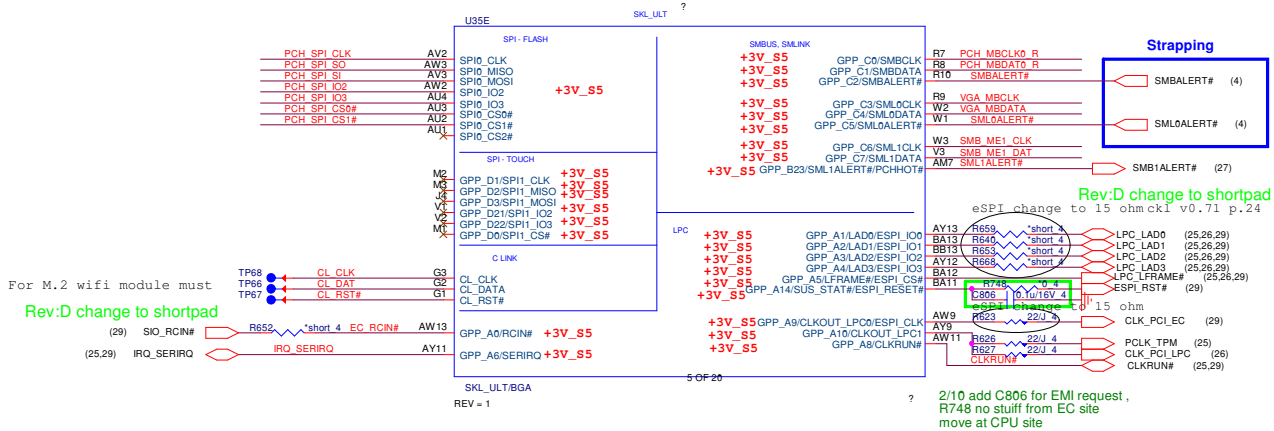
RTC Clock 32.768KHz (RTC)

Trace length < 1000 mils

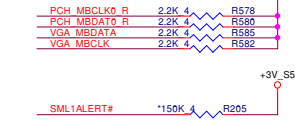
RTC Circuitry (RTC)

On SKL voltage at VCCRTC does not exceed 3.2V

1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032



SMBus



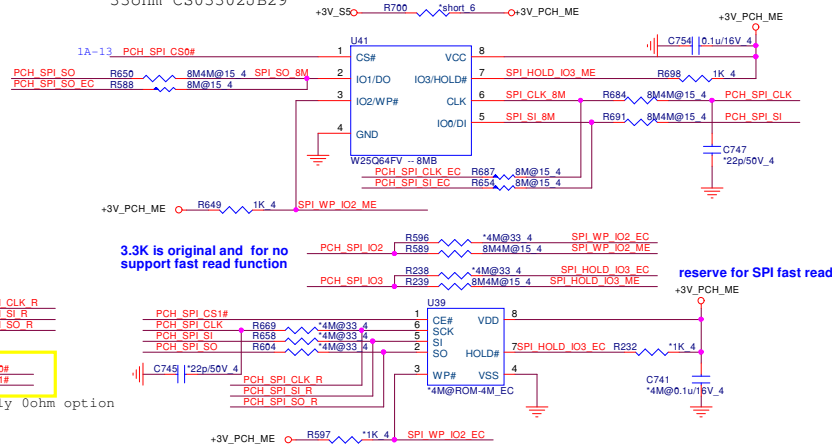
Termination Resistor Requirement for PCH PCHHOT# #
Reserve PU 150K resistor

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZNOQ00	GD25B64CSIGR

PCH SPI ROM(8M+4M)

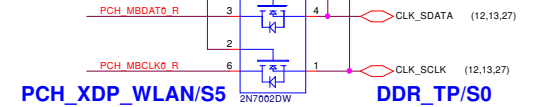
15ohm CS01502JB12
33ohm CS03302JB29

Rev:D change to shortpad

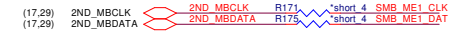


S5

SMBus(PCH)

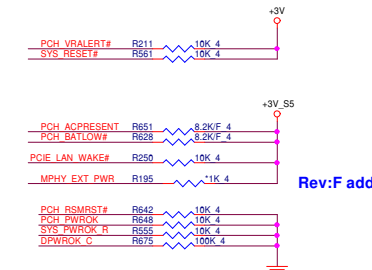
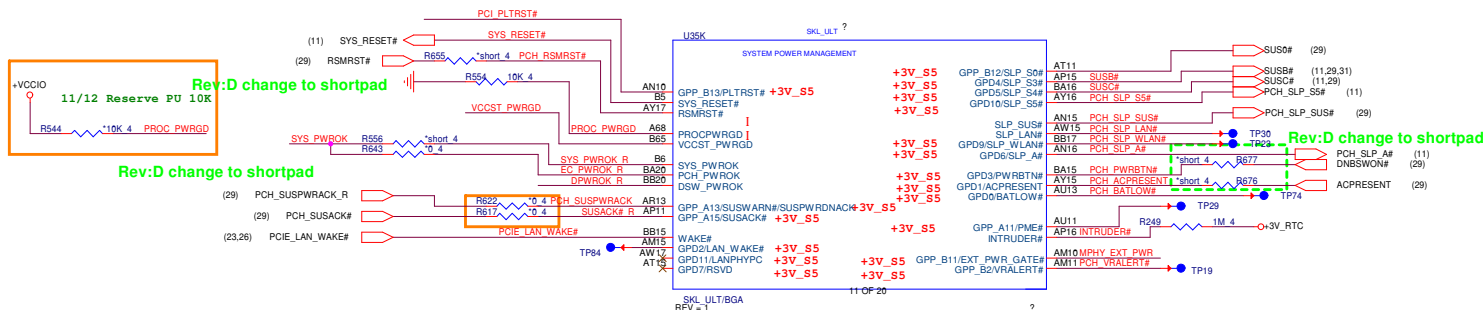


SMBus(EC)

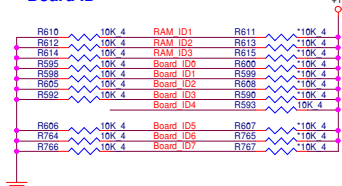


EC/S5

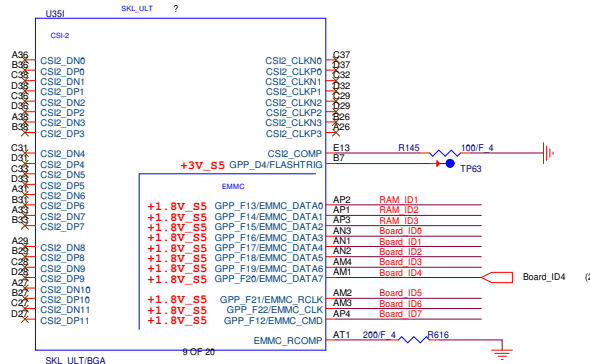
Rev:D change to shortpad



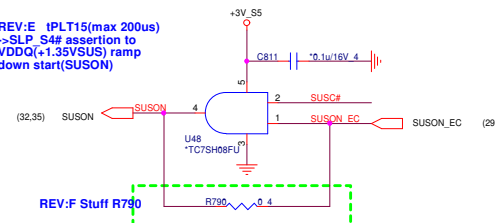
Board ID



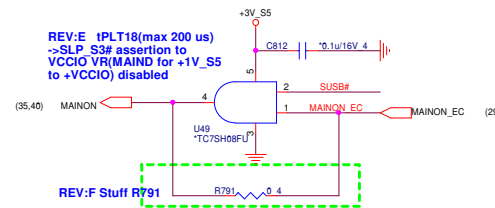
	Low	High		Low	High
BOARD_ID0	VRAM 2GB	VRAM 4GB	BOARD_ID5	Realtek Audio codec	CPU DSP
BOARD_ID1	Non IOAC	IOAC	BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID2	No G-sensor	G-sensor	BOARD_ID7	Reserved (Default)	Reserve
BOARD_ID3	No TPM	TPM			
BOARD_ID4	No touch panel	touch panel			



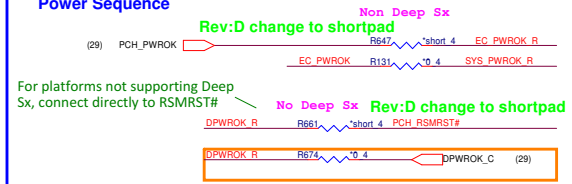
REV:E tPLT15(max 200us)
->SLP_S4# assertion to
VDDQ(+1.35VSUS) ramp
down start(SUSON)



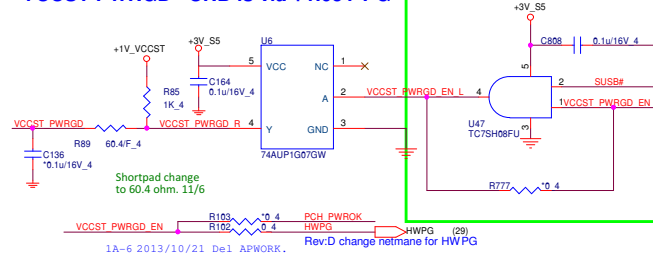
REV:E tPLT18(max 200 us)
->SLP_S3# assertion to
VCCIO VR(MAIND for +1V_S5
to +VCCIO) disabled



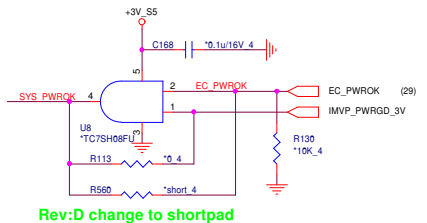
Power Sequence



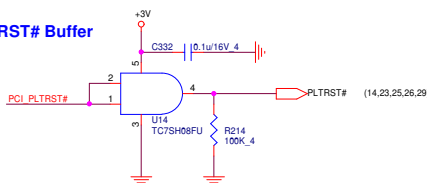
VCCST_PWRGD CRB is via +1.05V PG



SYSPWOK

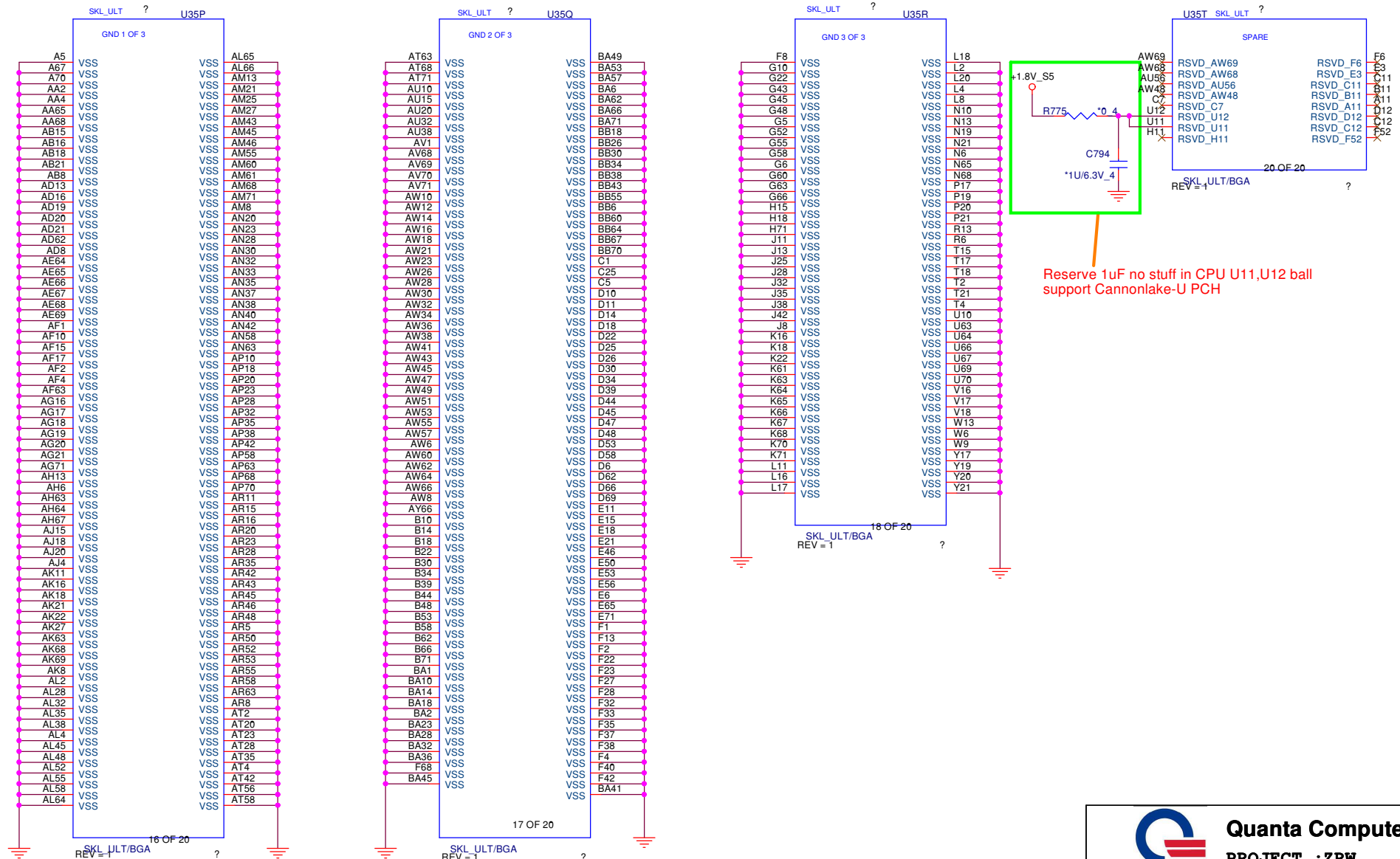


PLTRST# Buffer



A

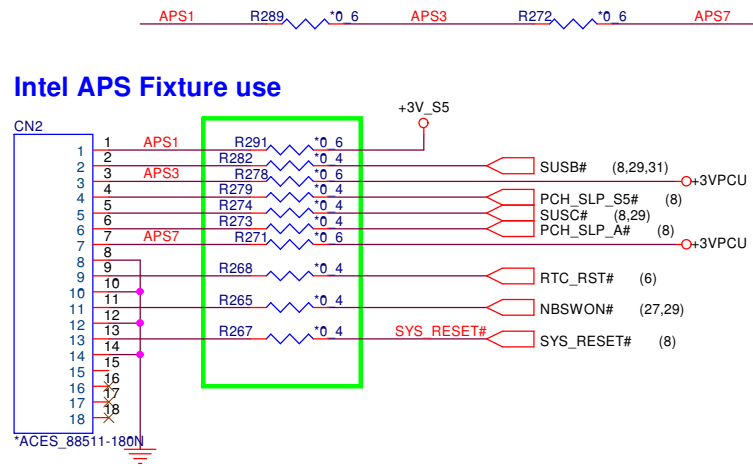
Skylake ULT (GND)

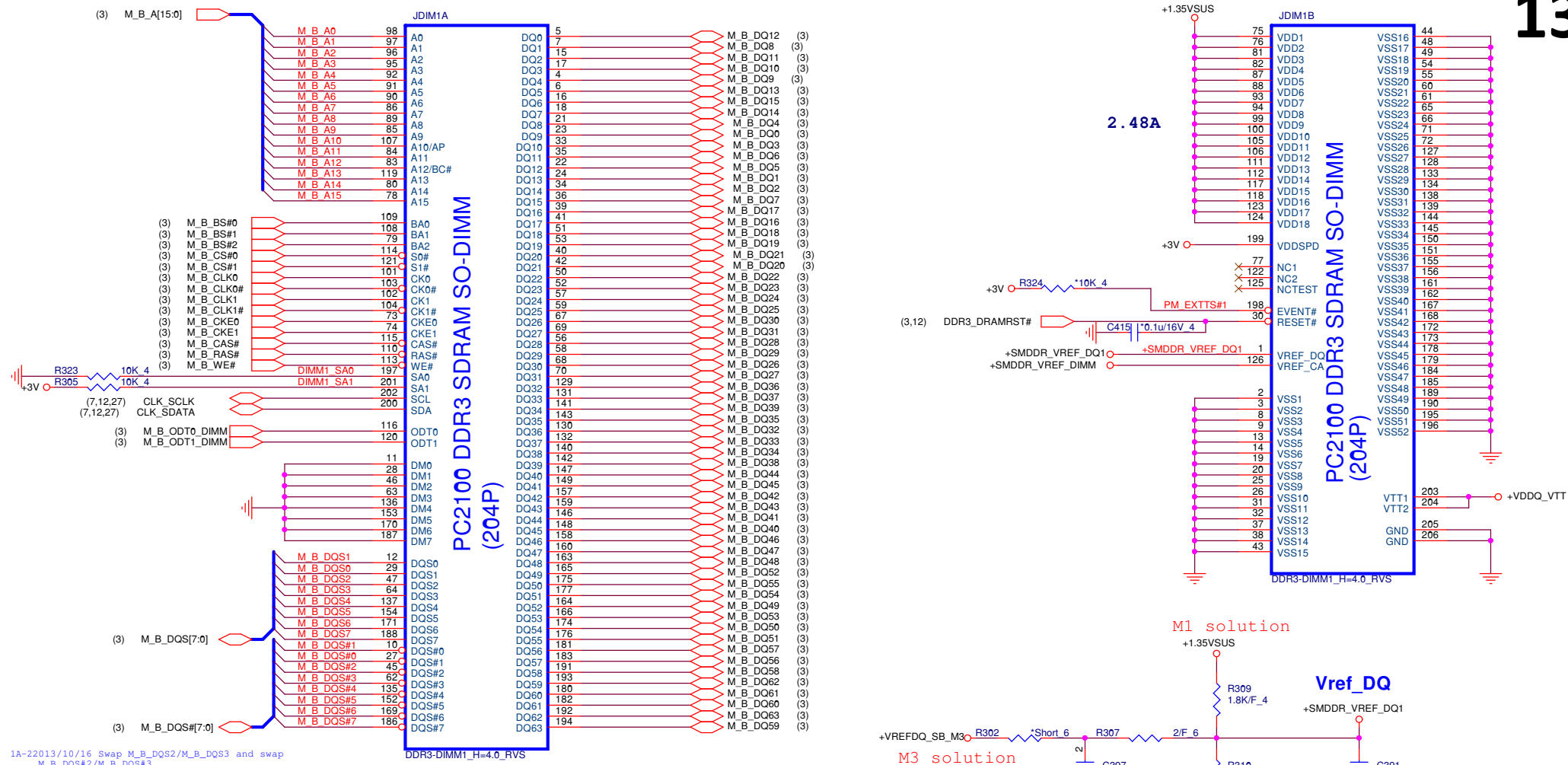


Quanta Computer Inc.

PROJECT : ZRW

Size	Document Number	Rev
	Skylake 10/17/18 (GND)	3A
Date:	Monday, July 20, 2015	Sheet 10 of 48

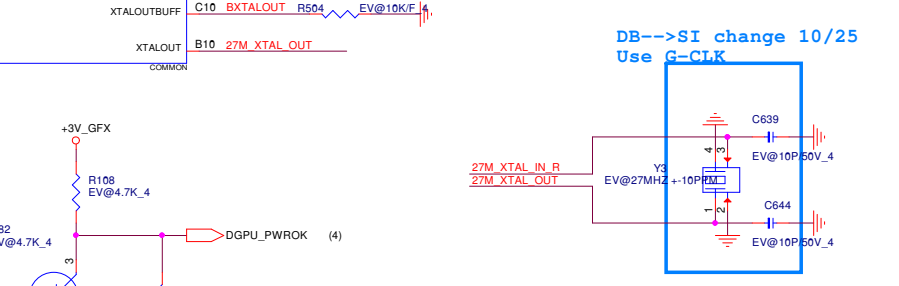
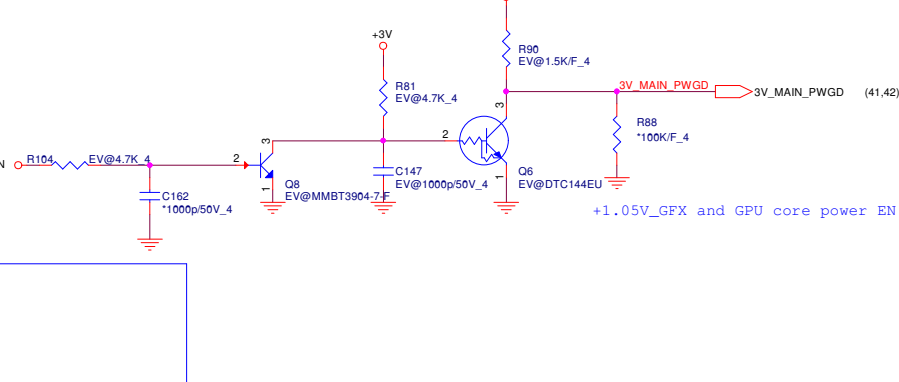
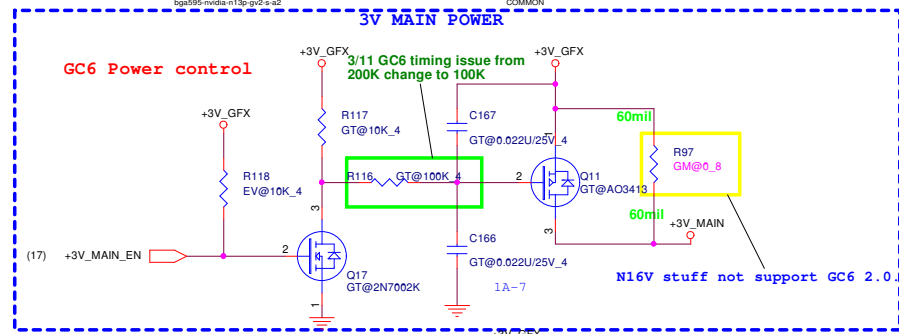
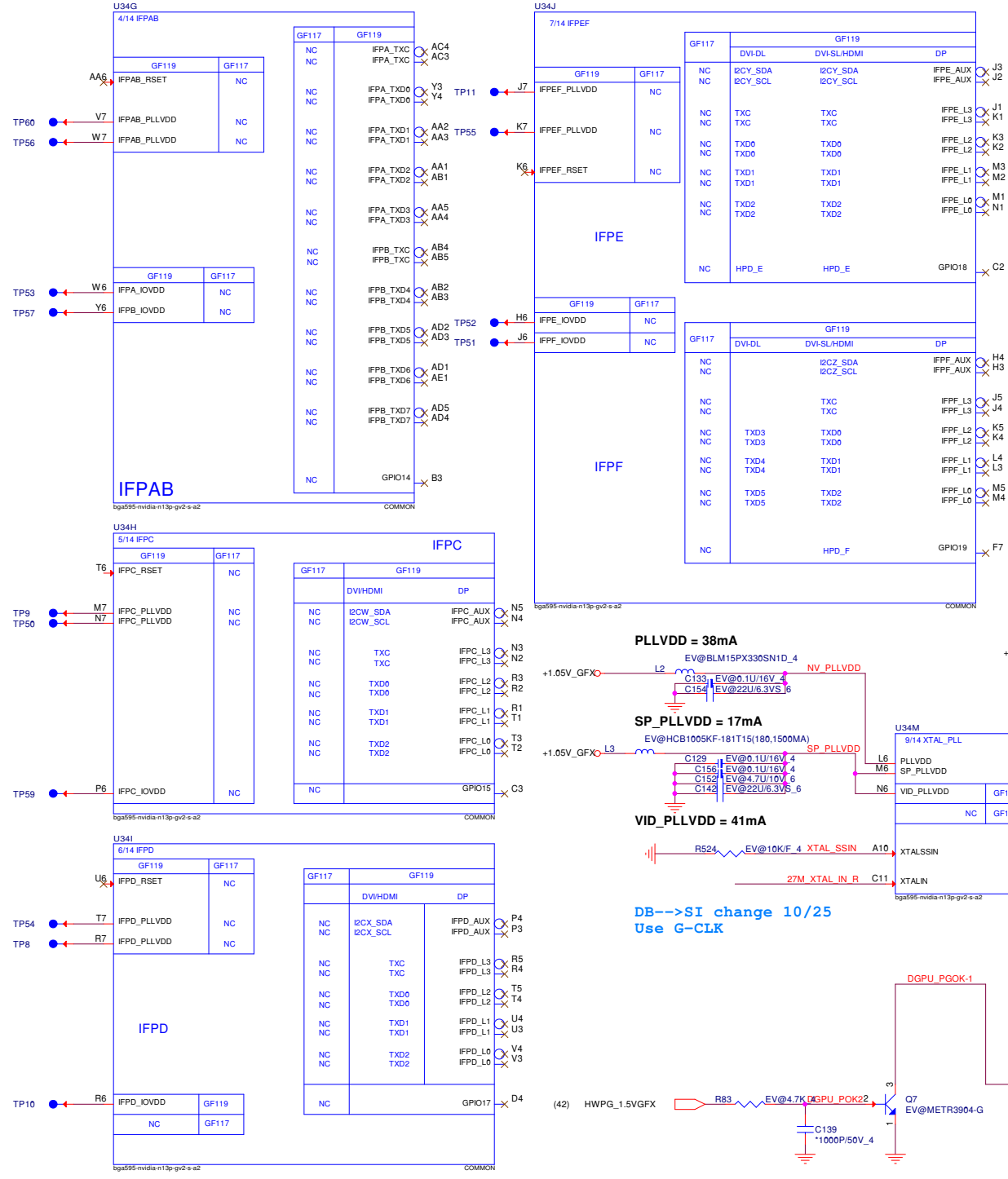




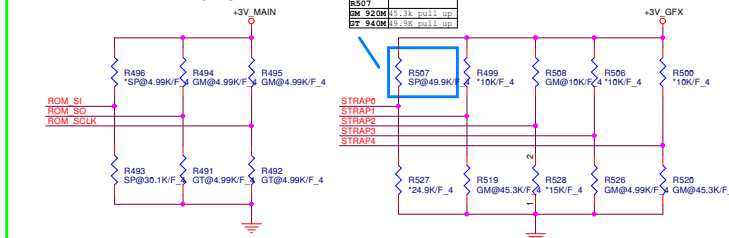
Quanta Computer Inc.

PROJECT : ZRW





N16S-GT/N16V-GM Strapping table



N16S-GT DID=0x1347 [940M]

ROM_SCLK = Stuff 4.99K pull down
 ROM_SO = Stuff 4.99K pull down
 STRAP0 = Stuff 49.9K pull up
 STRAP1 = NC
 STRAP2 = NC
 STRAP3 = NC
 STRAP4 = NC
 ROM_SI = VRAM Configuration follow belowtable

N16V-GM DID=0x1299 [920M]

ROM_SCLK = Stuff 4.99K pull up
 ROM_SO = Stuff 4.99K pull up
 STRAP0 = Stuff 45.3K pull up. (EDID Pan)l
 STRAP1 = Stuff 45.3K pull down. (Gen3 support)
 STRAP2 = Stuff 10K pull up. (DID 0x1299)
 STRAP3 = Stuff 4.99K pull down. (No display out)
 STRAP4 = Stuff 45.3K pull down. (Gen3/max speed)
 ROM_SI = VRAM Configuration follow belowtable

Note: GC6 2.0 is supported by N16x GPU in the GB2B, GB4B-12B, and GB3B-25B packages.

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GT/N16V-GM Strapping table

ROM_SI N16S-GT [940M]
 2G Hynix 128Mx16 --> 34.8K PD
 2G Micron 128Mx16 --> 45.3K PD
 2G Samsung 128Mx16 --> 4.99K PU
 4G Hynix 256Mx16 --> 30.1K PU Single Rank
 4G Hynix 256Mx16 --> 24.9K PU Dual Rank
 4G Micron 256Mx16 --> 10K PU
 4G Samsung 256Mx16 --> 15K PD

ROM_SI N16V-GM [920M Single RAM]
 2G Hynix 128Mx16 --> 20K PD
 2G Micron 128Mx16 --> 30.1K PD
 2G Samsung 128Mx16 --> 34.8K PD
 4G Micron 256Mx16 --> 10K PD
 4G Hynix 256Mx16 --> 10K PU
 4G Samsung 256Mx16 --> 24.9K PD

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Resistor P/N	
4.99K	--> CS24992FB26
10K	--> CS31002FB26
15K	--> CS31502FB24
20K	--> CS32002FB29
24.9K	--> CS32492FB16
30.1K	--> CS33012FB16
34.8K	--> CS33482FB22
45.3K	--> CS34532FB18 GM
49.9K	--> CS34992FB10 GT

ROM_SO
 N16S-GT --> 4.99K PD
 N16V-GM --> 4.99K PU

ROM_SCLK
 N16S-GT --> 4.99K PD
 N16V-GM --> 4.99K PU

STRAP0
 N16S-GT --> 49.9K PU
 N16V-GM --> 45.3K PU

N16S-GM/GT/LP VRAM Configuration Table ROM_SI

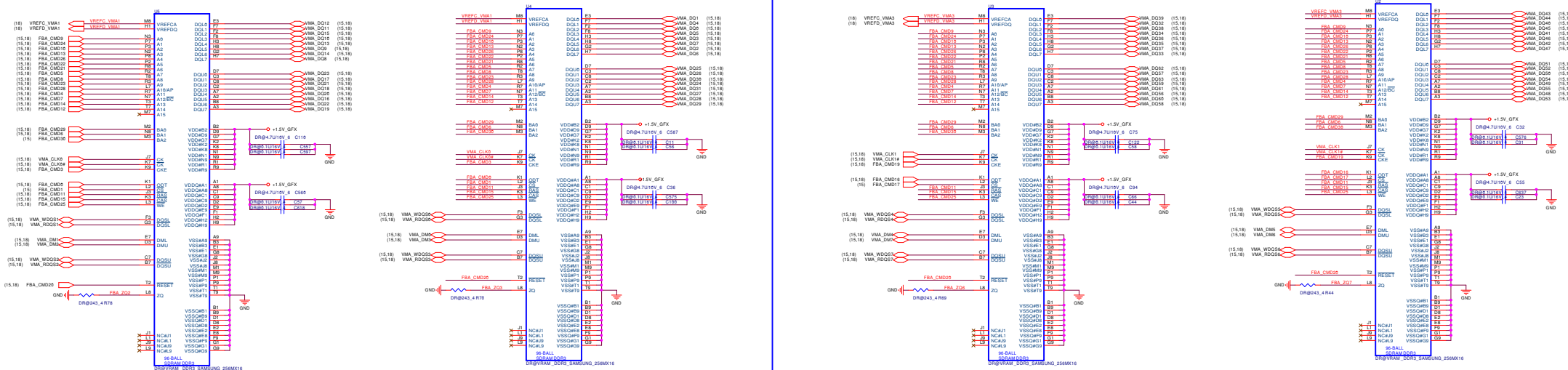
RAMCFG [3:0]	DESCRIPTION	1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0101 0x5	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX C-die	H5TC4G63CFF-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank 2GB
1100 0xC	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX C-die	H5TC4G63ER-N0C	PU 24.9K ohm	AKD5PZDTW03	Dual Rank 4GB
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank Dual Rank
0100 0x2	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG D-die	K4W4G1646D-BC1A	PD 15K ohm	AKD5PGWT504	Single Rank Dual Rank
0100 0x4	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG E-die	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT504	Single Rank 2GB
1101 0xD	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG E-die	K4W4G1646E-BC1A	PU 30.1K ohm	AKD5PGDT504	Dual Rank 4GB

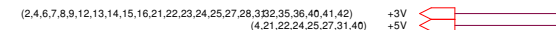
N16V-GM/GL VRAM Configuration Table ROM_SI

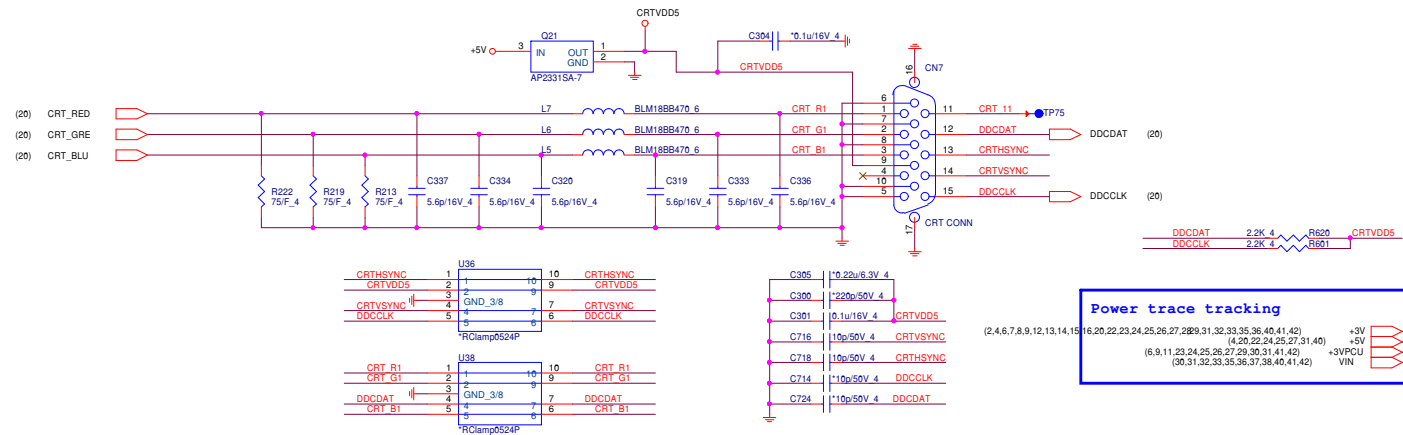
RAMCFG [3:0]	DESCRIPTION	1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank or Single Rank stuffing for Dual Rank
1001 0x9	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		HYNIX C-die	H5TC4G63CFF-N0C	PU 10K ohm	AKD5PZDTW03	
0100 0x4	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG D-die	K4W4G1646D-BC1A	PD 24.9K ohm	AKD5PGWT504	
1010 0xA	DDR3L 256Mx16, 64bit, 4Gb, 1000MHz		SAMSUNG E-die	K4W4G1646E-BC1A	PU 15K ohm	AKD5PGDT504	

N16V-GM strap0~3 table

STRAP0 = Stuff 45.3K pull up. (EDID Panel)
 STRAP1 = Stuff 45.3K pull down. (Gen3 support)
 STRAP2 = Stuff 10K pull up. (DID 0x1299)
 STRAP3 = Stuff 4.99K pull down. (No display out)
 STRAP4 = Stuff 45.3K pull down. (Gen3/max speed)

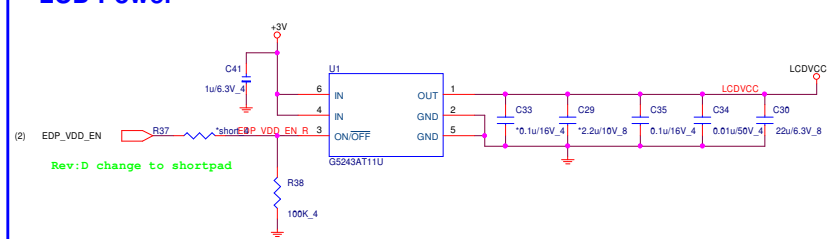






(2,4,6,7,8,9,12,13,14,15) 16,20,22,23,24,25,26,27,28,29,31,32,33,35,36,40,41,42) +3V
(4,20,22,24,25,27,31,40) +5V
(6,9,11,23,24,25,26,27,29,30,31,41,42) +3VPCU
(30,31,32,33,35,36,37,38,40,41,42) VIN

LCD Power



The diagram illustrates the hardware setup for connecting two I2C modules, labeled S5 and S0, through an MCP23017P I/O expander. Module S5's I2C pins are connected to the MCP23017P's VCC, GND, SDA, and SCL pins. Similarly, module S0's I2C pins are connected to the MCP23017P's corresponding pins. The MCP23017P is configured with pull-up resistors (R9, R10, R11, R12) and decoupling capacitors (C1, C2). The circuit also shows the power supply connections for both modules.

S5

(4) I2C1_SDA
(4) I2C1_SCL

+3V

GND

R10 *TSI@0_4

O2

6 1

2

3 4

5

*TSI@2N7002DW

R13 *TSI@0_4

C2 C1

I2C1_SDA_C

I2C1_SCL_C

S0

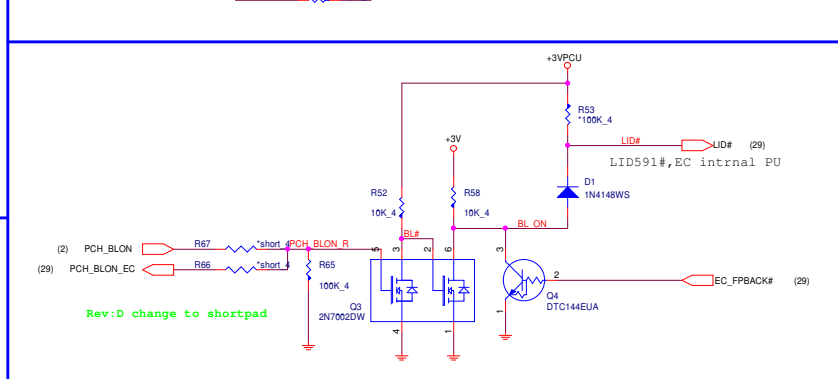
R9 *TSI@10K_4

R12 *TSI@10K_4

VCC

GND

TPD>100kHz, TS=400Khz
Intel design guide suggestion
MCP PIV 10u.
Per inch 3u TS=3x5inch
400KhZto100u =2.4~0.4k.
100KHz 10~100u=9k~1k.



Rev. D
change to
shortpad

+3VPCU

R435 ~100K_4

R434 "short_6

D28 ~VPORT_6

1 2

C556 4.7U10V_6

1 2

LID#

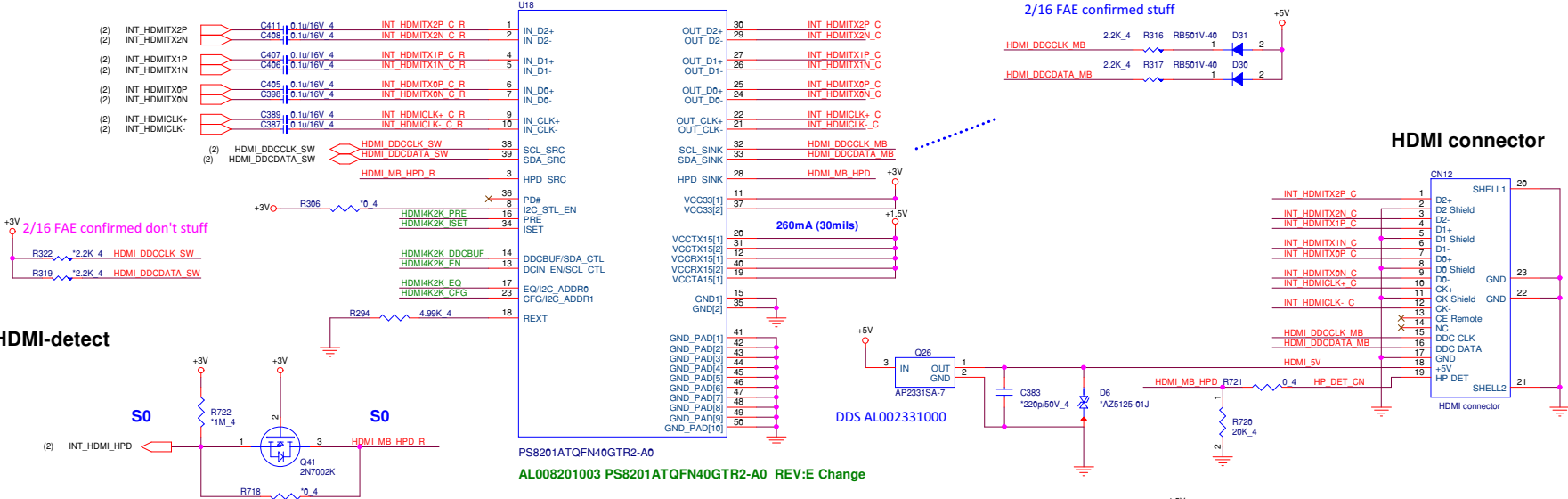
D23 ~VPORT_6

MR1 AH9249NTR-G1

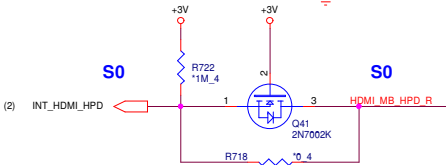
1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

<HDM>

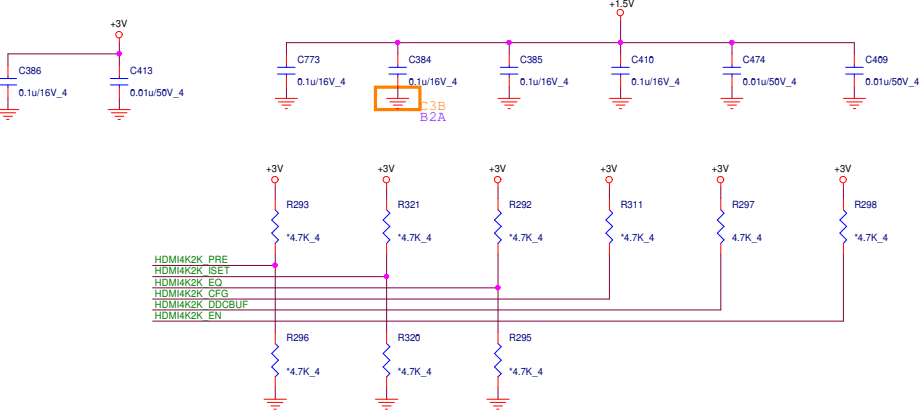
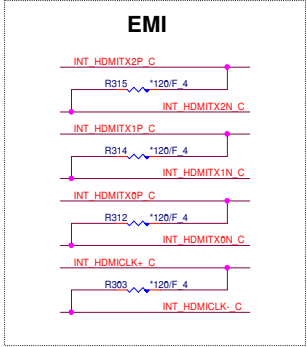
From PCH



HDMI-detect

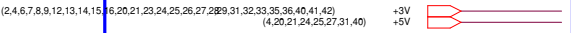


EMI



	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC (Low)	0	dB	default	12.4	dB HDMI ID disable	default, AC coupling input
1 (High)	1.6	dB	+13%	4.3	dB HDMI ID enable	active DDC buffer with default threshold
M	2.5	dB	-13%	8.6	dB N/A	active DDC buffer without internal pull up resistor

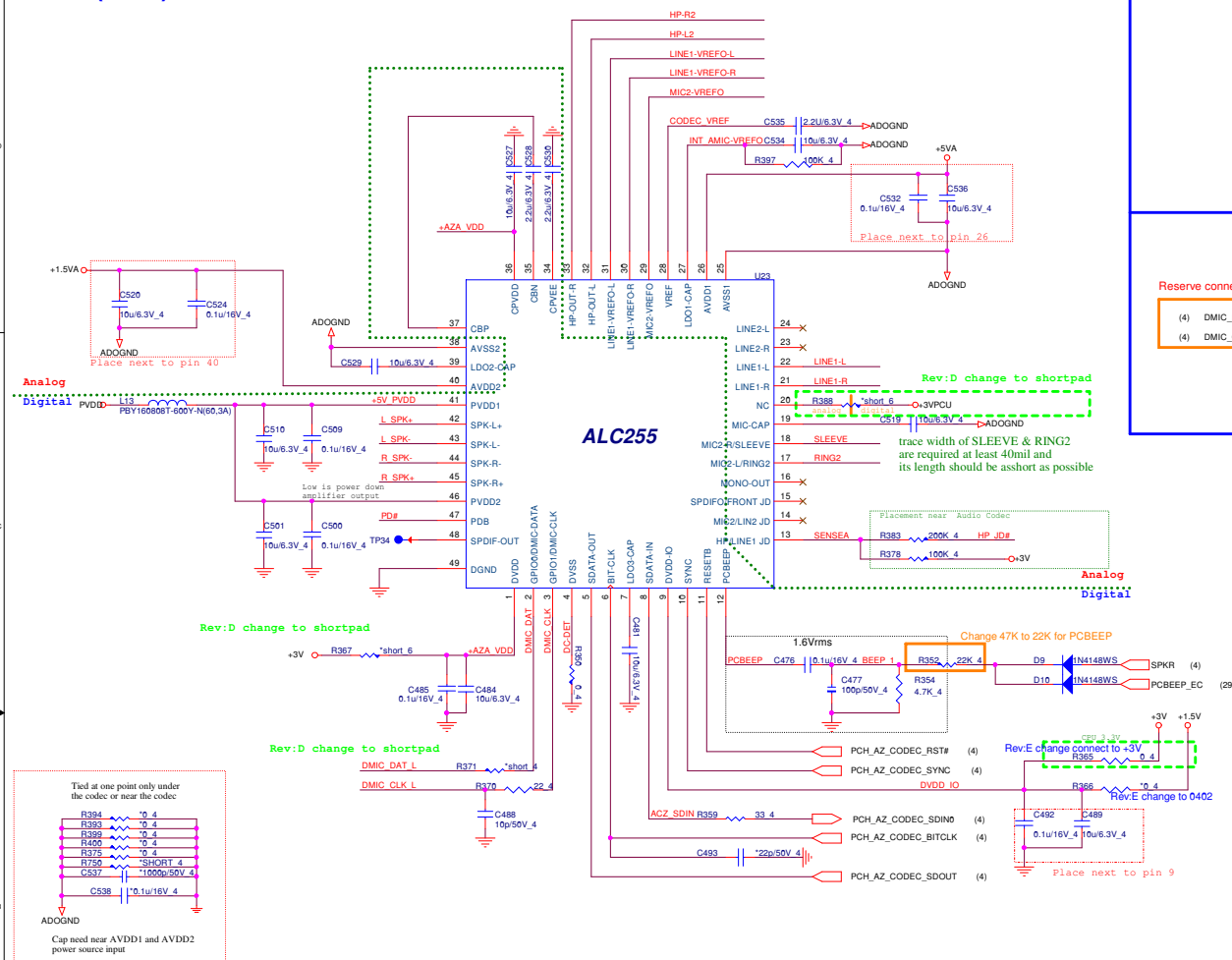
Power trace tracking



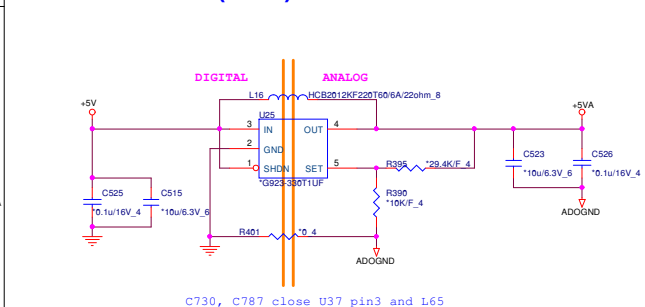
Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

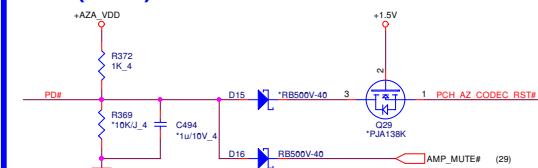
Codec(ADO)



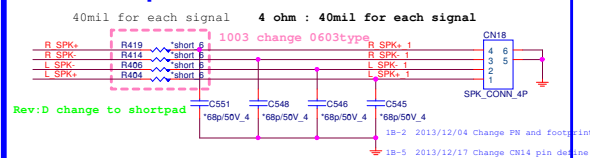
Codec PWR 5V(ADO)



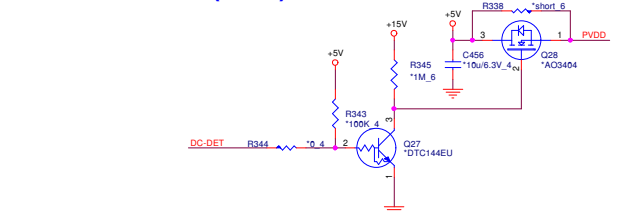
Mute(ADO)



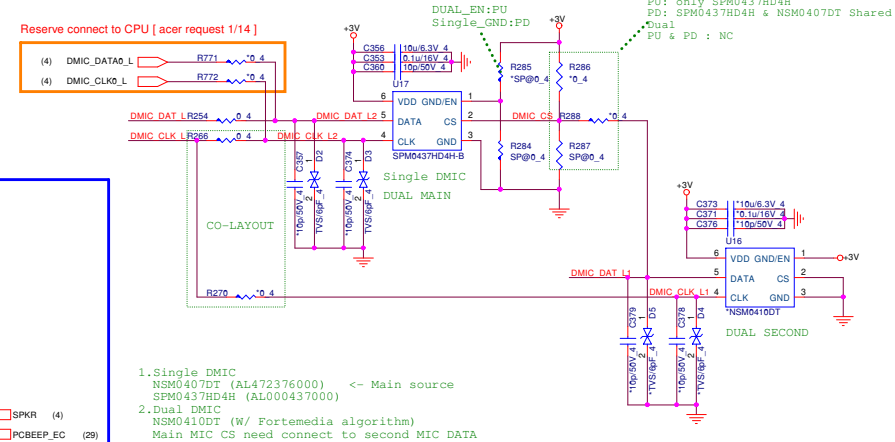
Internal Speaker



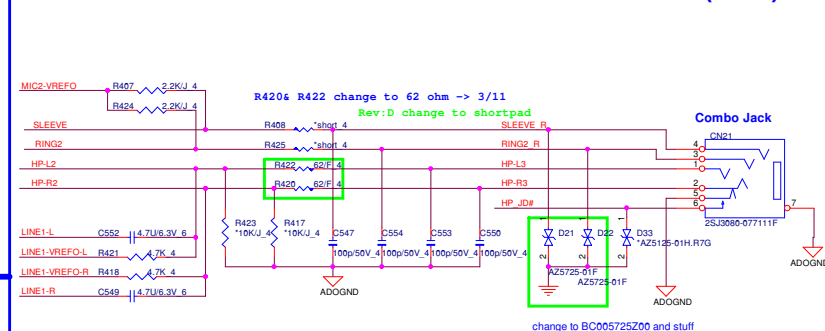
DC-DET circuit(ADO)



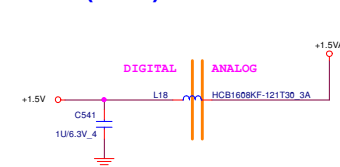
D-Mic (MIC)



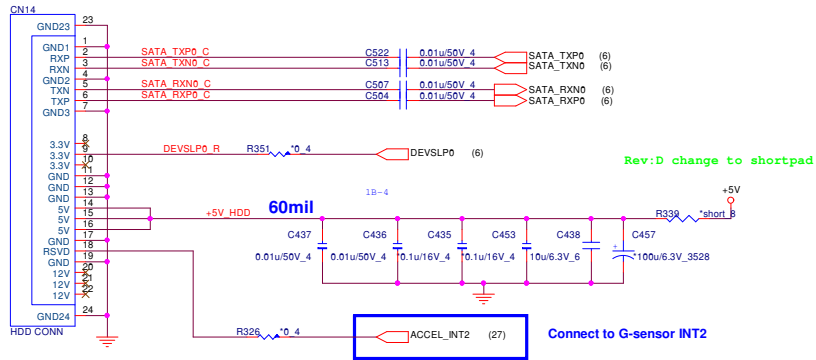
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



Codec PWR 1.5V(ADO)

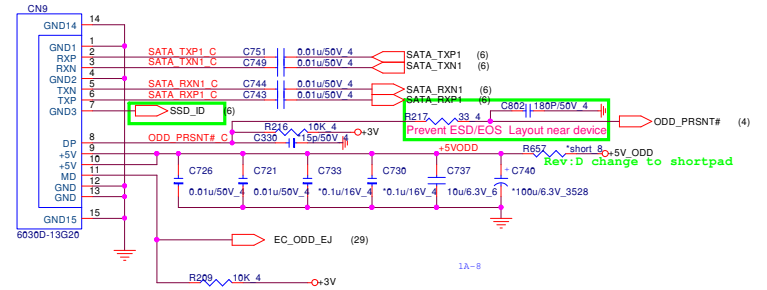


2.5" SATA HDD (HDD)

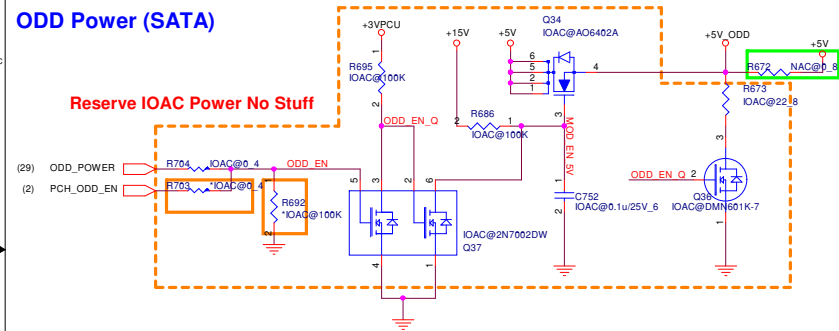


SATA ODD Connector

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ODD Power (SATA)



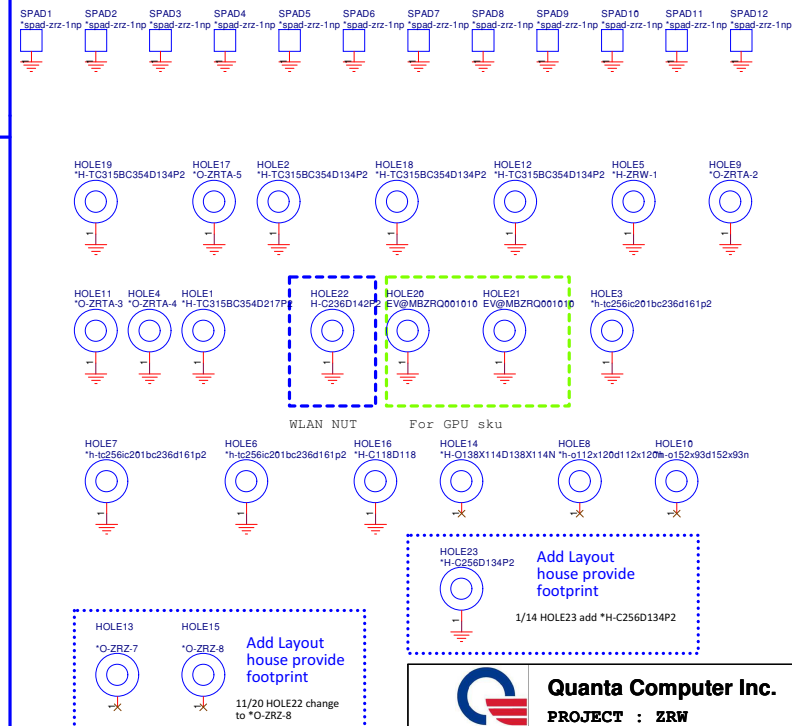
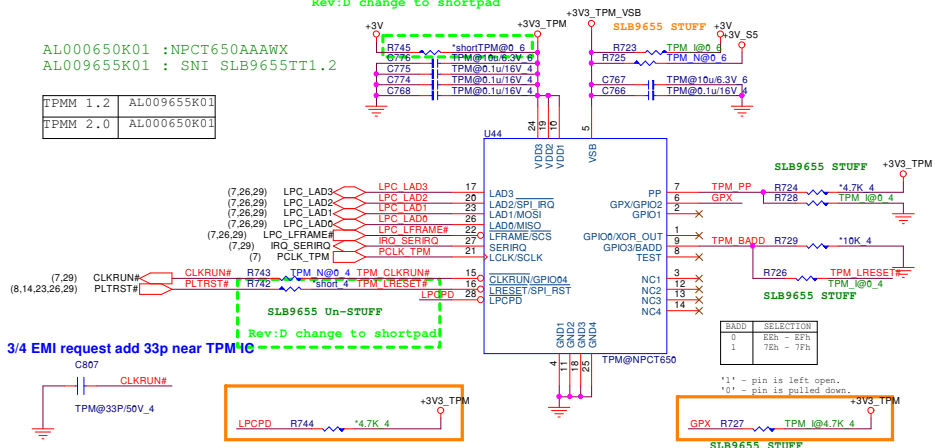
TPM NPCT650 (TPM)

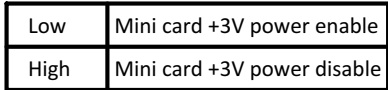
SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)


Rev:D change to shortpad

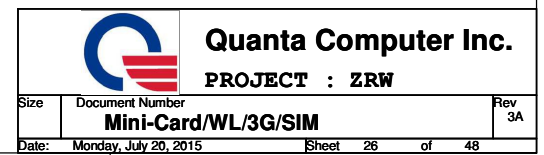
```
AL000650K01 :NPCT650AAAWX
AL009655K01 : SNI SLB9655TT1.2
```

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01

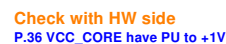


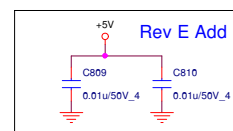
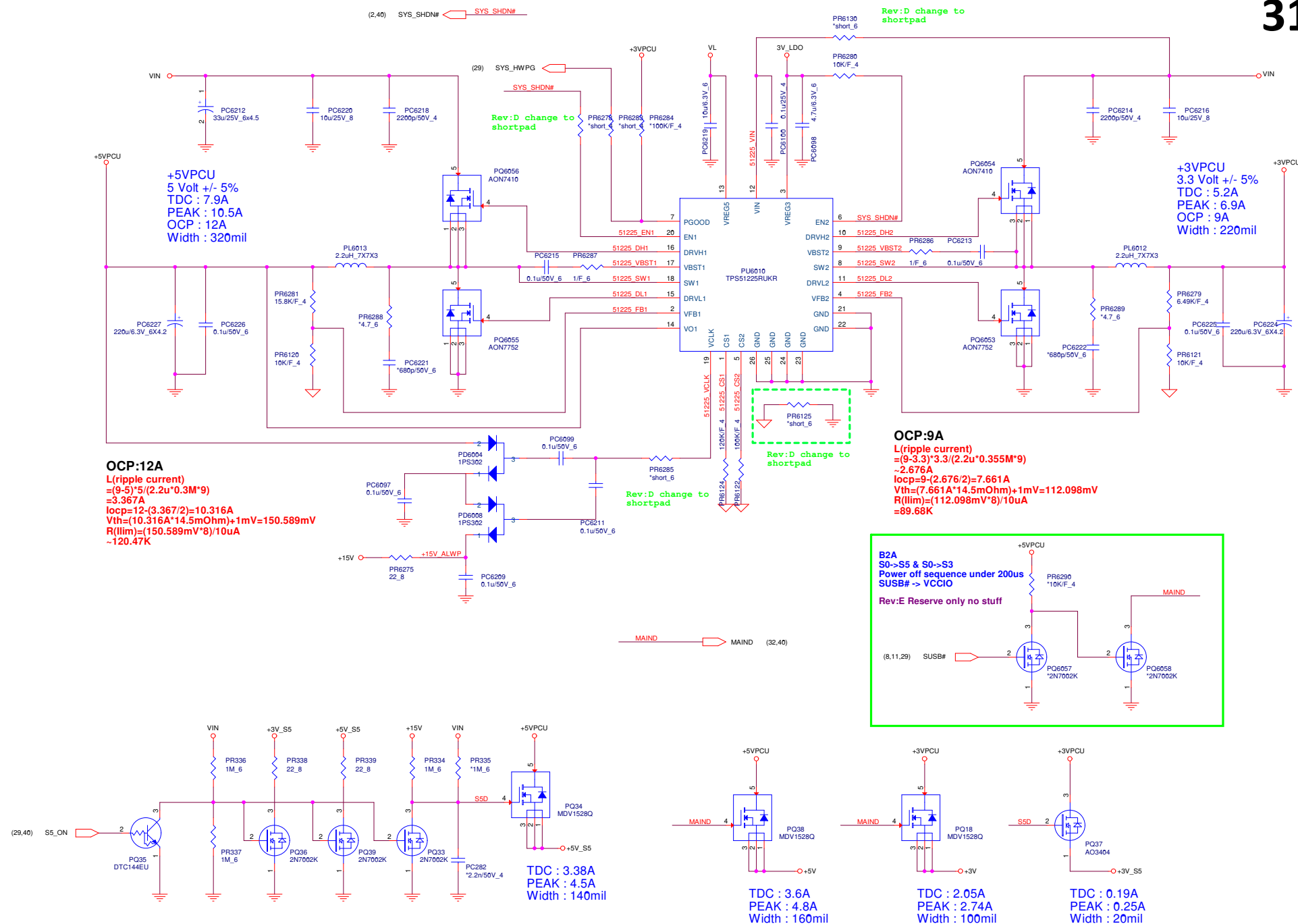


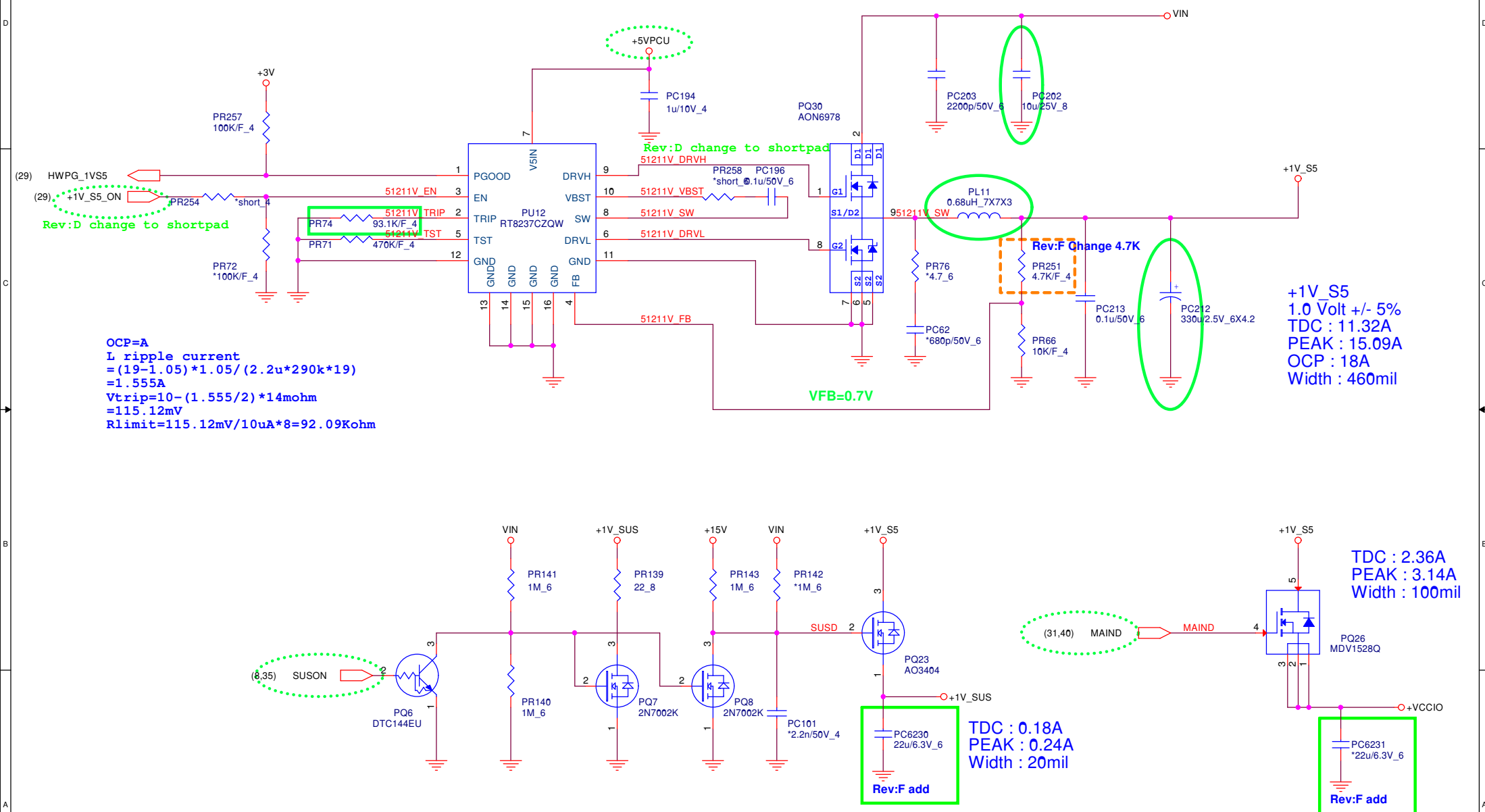
(6) 



Pin connection diagram for the NBSW0601 device. The diagram shows two rows of pins. The left row (pins 1-30) is labeled with pin numbers, pin names (MX0-MX7, MY16-MY26, MY0), and their connections to a CN20 connector, a KB CONN, and a D34 diode. The right row (pins 31-60) is labeled with pin numbers, pin names (MX4-MX7, MY0-MY12, MY16-MY26, MY0), and their connections to an <EMI> connector, various CPx pins (CP5, CP1, CP2, CP3, CP6, CP4), and ground. A green box highlights a section of the right row (pins 31-40) and is labeled 'Prevent ESD/EOS Layout near device'. A red box highlights a section of the right row (pins 41-50) and is labeled 'NBSW0601 (11,29)'. A blue box highlights a section of the right row (pins 51-60) and is labeled '180P/50V_4'. A yellow box highlights a section of the right row (pins 61-70) and is labeled '180P/50V_4'.



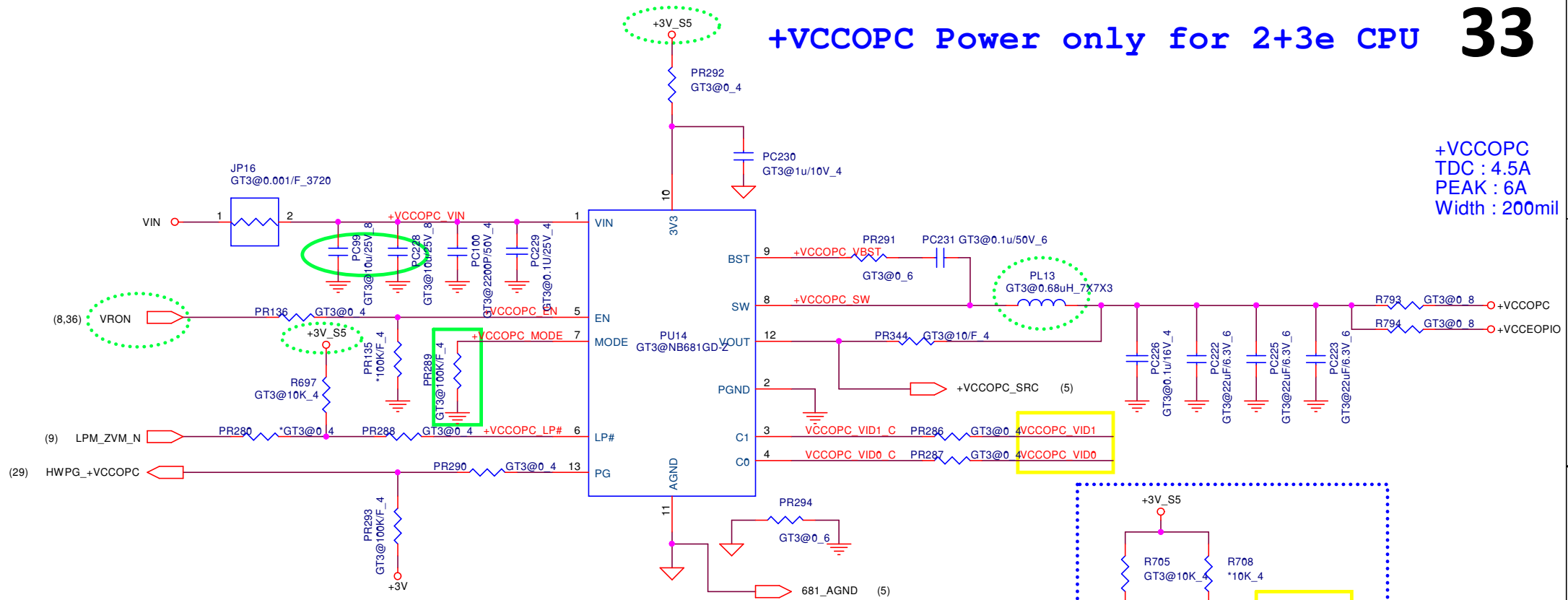




+VCCOPC Power only for 2+3e CPU

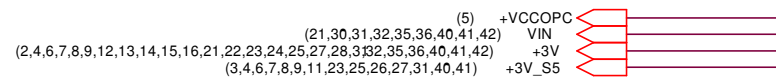
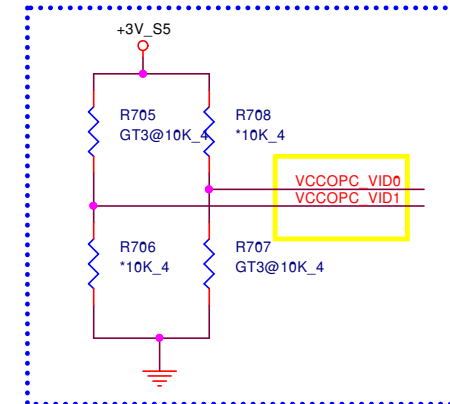
33

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V



D

D

C


C

B

B

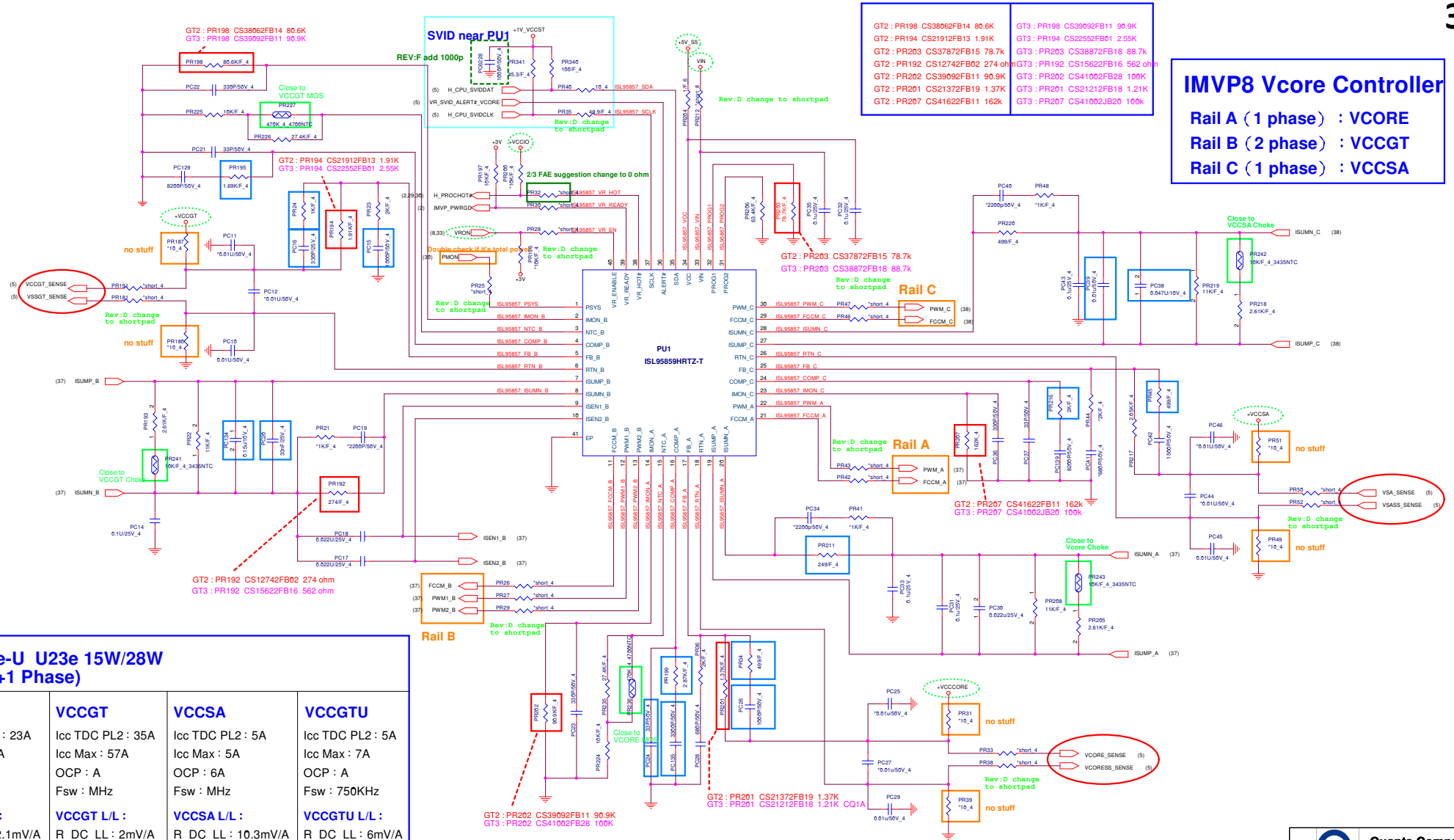
A

A

		Quanta Computer Inc.
		PROJECT : ZRW
Size	Document Number	Rev
	+VCCEOPIO (NB681GD-Z)	2A
Date: Thursday, June 25, 2015		Sheet 34 of 48

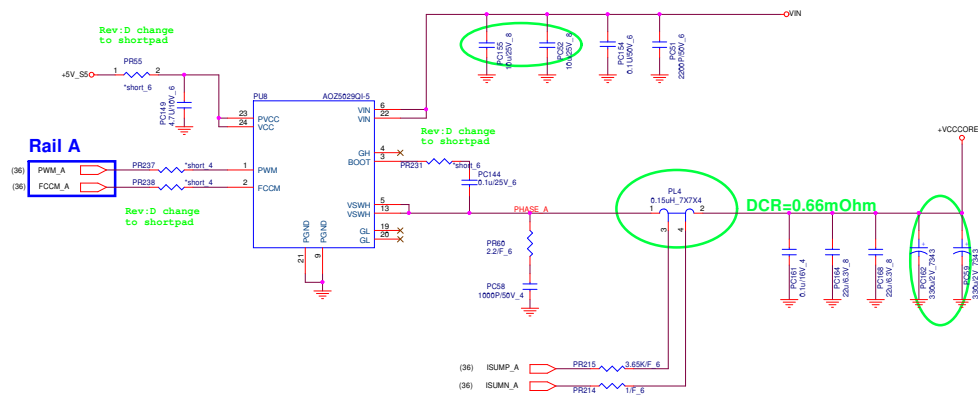


Rail A (1 phase)	: VCORE
Rail B (2 phase)	: VCCGT
Rail C (1 phase)	: VCCSA

Skylake-U U23e 15W/28W
(1+2+1+1 Phase)

VCCORE	VCCGT	VCCSA	VCCGTU
lcc TDC PL2 : 23A	lcc TDC PL2 : 35A	lcc TDC PL2 : 5A	lcc TDC PL2 : 5A
lcc Max : 29A	lcc Max : 57A	lcc Max : 5A	lcc Max : 7A
OCp : 35A	OCp : A	OCp : 6A	OCp : A
Fsw : MHz	Fsw : MHz	Fsw : MHz	Fsw : 750KHz
VCCORE L/L :	VCCGT L/L :	VCCSA L/L :	VCCGTU L/L :
R_DC_LL : 2.1mV/A	R_DC_LL : 2mV/A	R_DC_LL : 10.3mV/A	R_DC_LL : 6mV/A
R_AC_LL : 2.1mV/A	R_AC_LL : 2mV/A	R_AC_LL : 10.3mV/A	R_AC_LL : 6mV/A

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VCORE

lcc TDC PL2: 23A

lcc Max : 29A

OCP : 35A

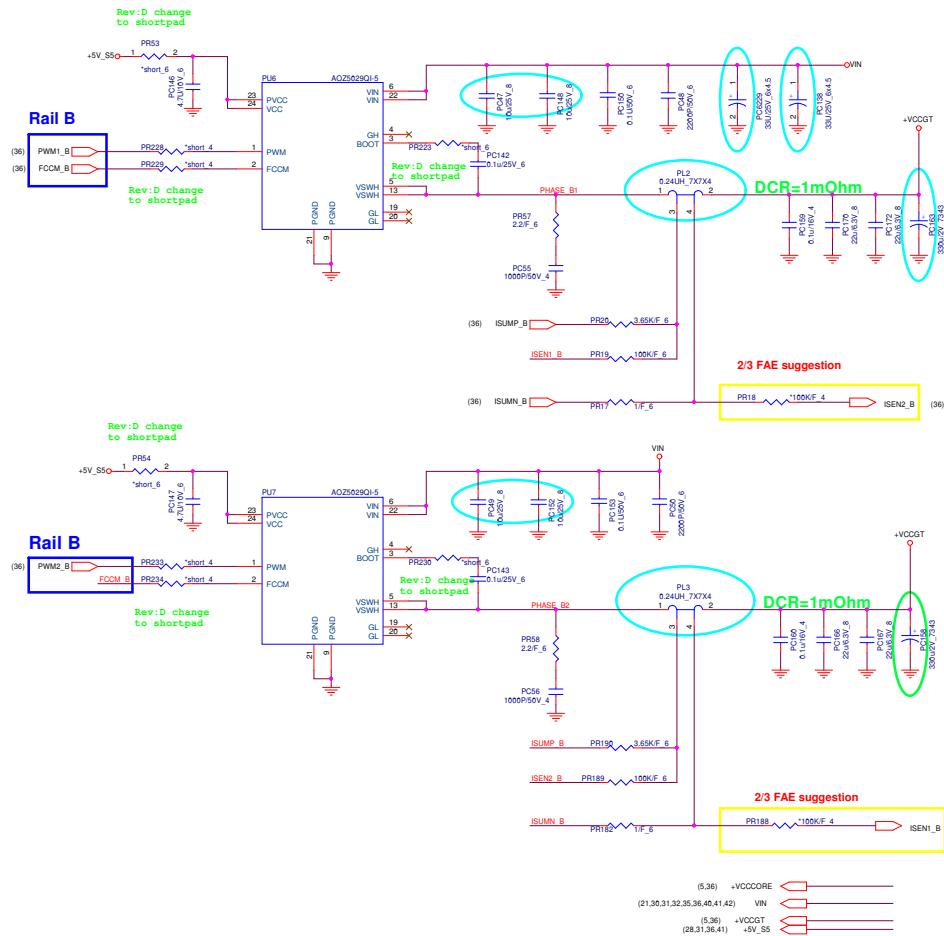
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

lcc TDC PL2 : 35A

lcc Max : 57A

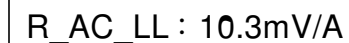
OCP : A

Fsw : MHz

VCCGT L/L :


R_DC_LL : 2mV/A

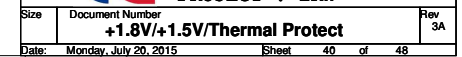
R_AC_LL : 2mV/A

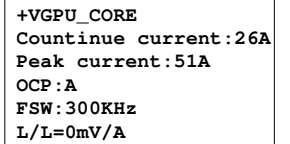


D
C
B
A

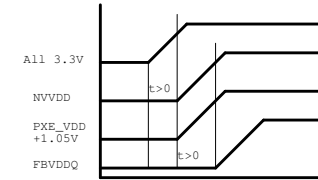
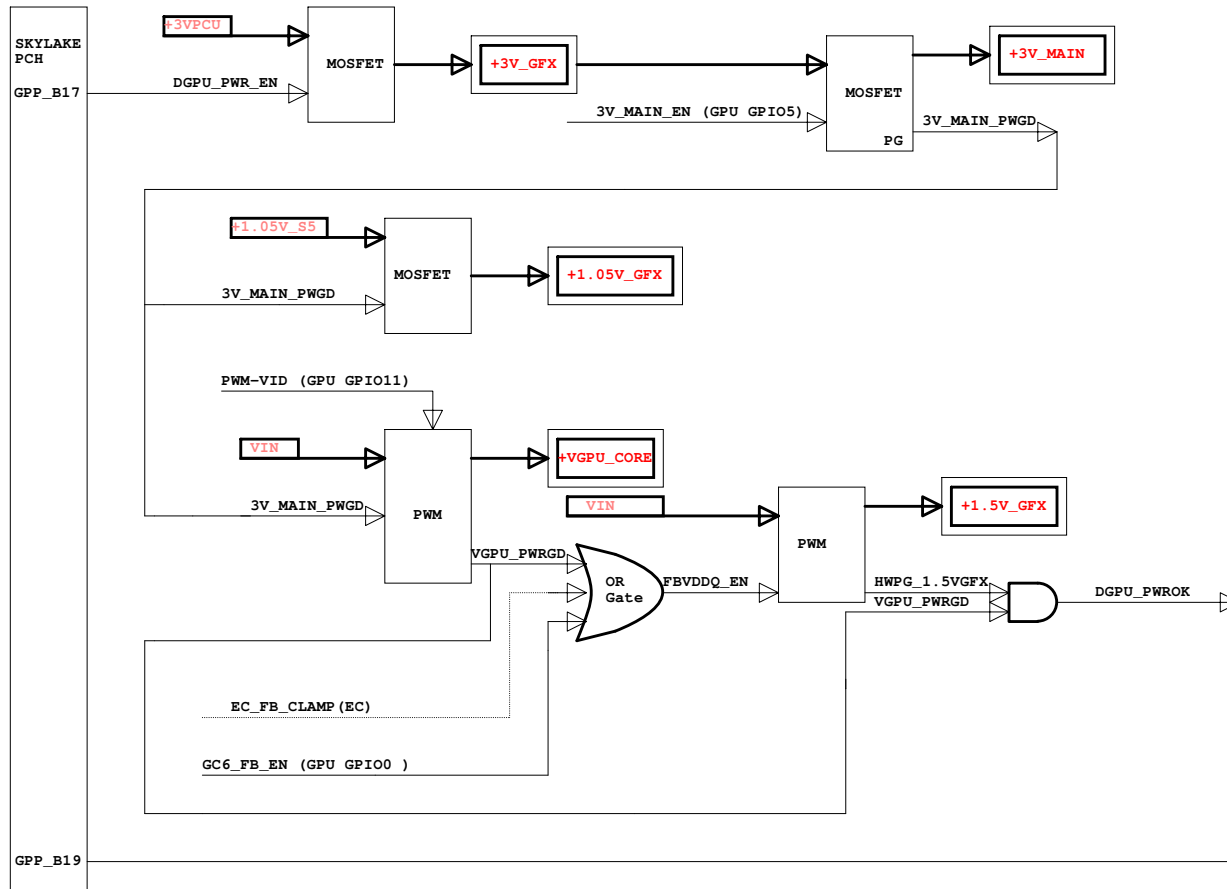
D
C
B
A

		Quanta Computer Inc.	
		PROJECT : ZRW	
Size	Document Number		Rev
	+VCCGTx (ISL95853HRZ-T)		2A
Date:	Thursday, June 25, 2015		Sheet 39 of 48



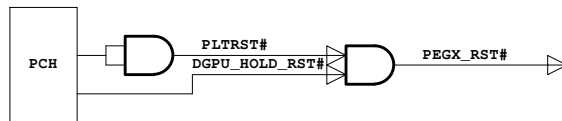


VGA power up sequence

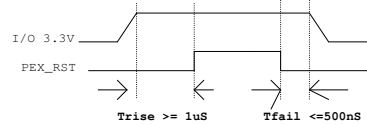


N15x Power on sequence
 Notes: -All 3.3V includes all rails powered at 3.3V
 -PEX_VDD 1.05V includes all rails that are bared

VGA Reset

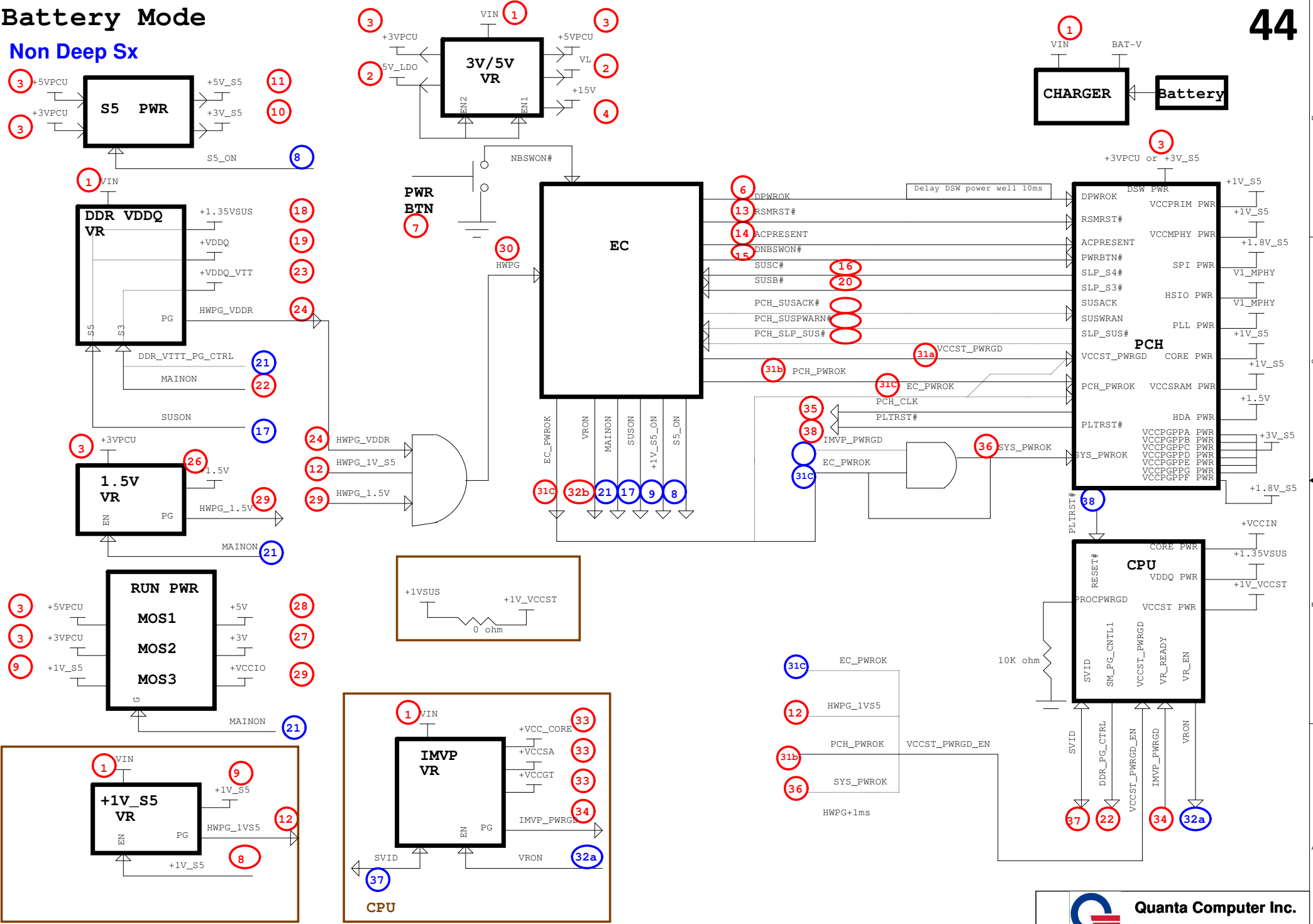


PEX_RST timing

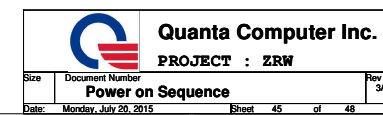


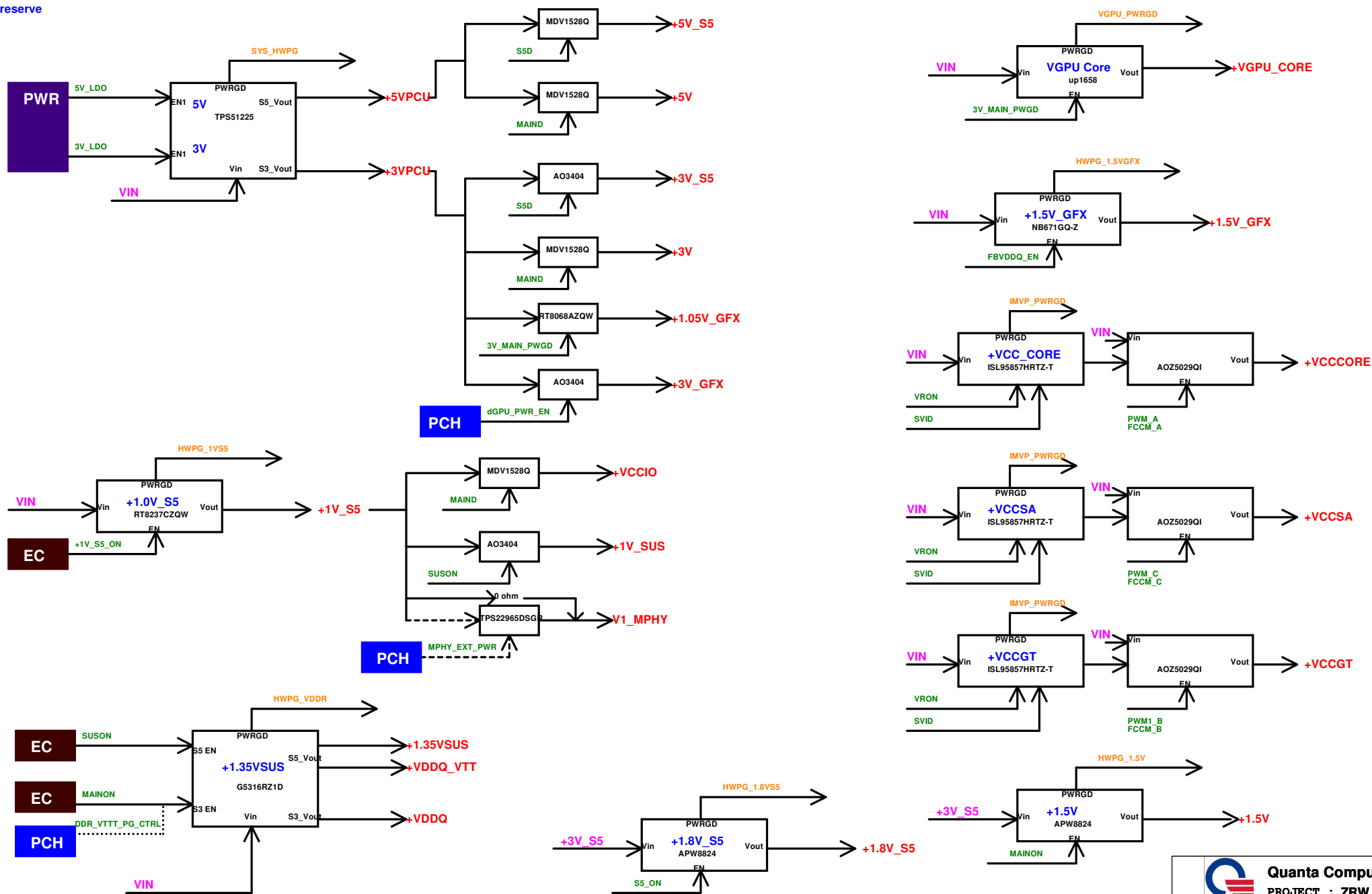
Battery Mode

Non Deep Sx

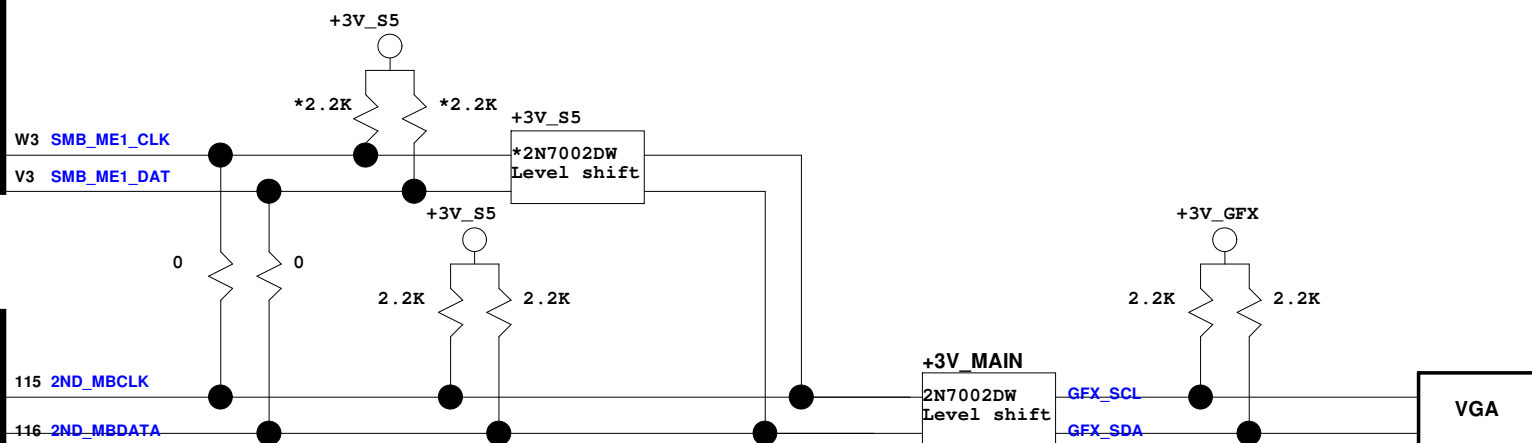
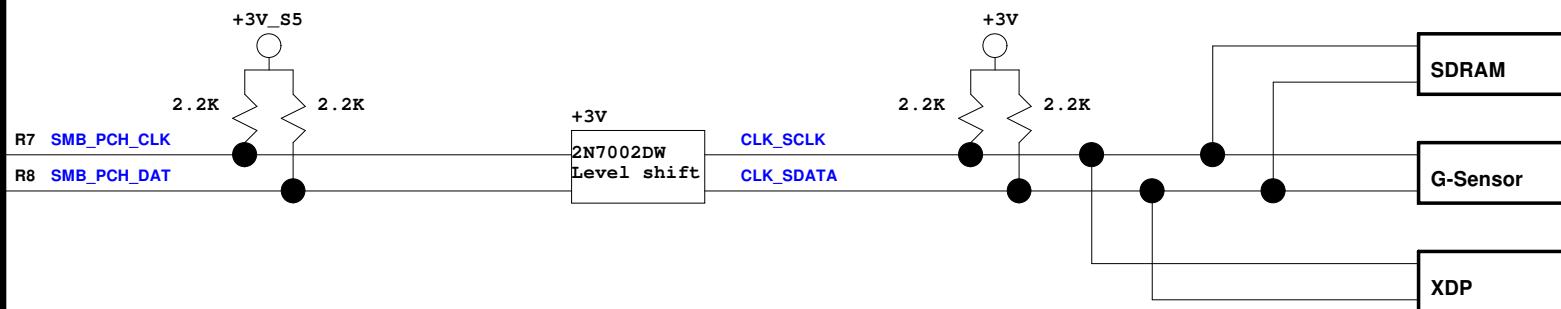
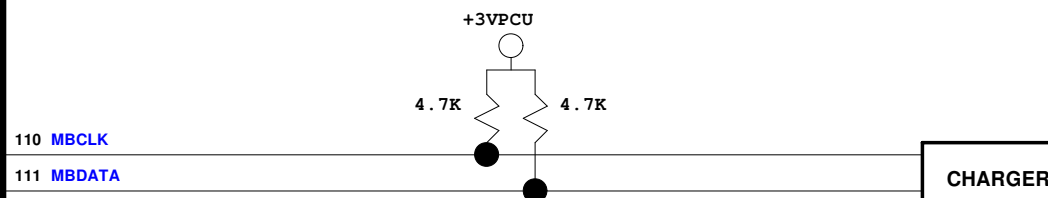


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Skylake U

EC
IT8987CX

Model	Date	CHANGE LIST
ZRW REV:A	1/20	1. FIRST RELEASED
ZRW REV:B	2/4	1. PU3#3 enable pin from VGPU_EN change to 3V_MAINPWGD control , add PR343 0ohm. (page 41) 2. U35#U11 #U12 connect to +1.8V_S5 for support Canonlake-U PCH. (page 10) 3. U46#3 from net USB_OC1# change connect to USB_O2# PCH. (page 28) 4. Add R776 33 0hm and C805 180 pf in NBSWON#. (pge 27) 5. Change LAN_WAKE# pin from CPU_LAN_WAKE# to WAKE#(ball BB15) to support CPPM(PCIE LTR&OBFF&L1 off) (page 08) 6. add PR344 between PU14#12 & JP13. for GT3 CPU (page 33) 7. add PR345 between PU13#12 & JP12 for GT3 CPU (page 34)
	2/12	1. net ACCEL_INTA from U35#AD1 change to U35#AB1 [UART0_RX] net TP_INT_PCH from U35#AD2 change to U35#AB3 [UART0_CTS#] (page 04) 2. CN3 all pin from UART1 change connect to UART2 (page 04) 3. R587 from 0 ohm change to 1k pull down for USB2ID (page 06) 4. add C806 for EMI request R748 0 ohm no stuff from EC site move at CPU site (page 07) 5. R293 stuff 4.7k , R294 from 4.99k change to 5.48 (page22) 6. XDP_TCK0,XDP_TCK1,XDP_TMS,XDP_TDI don't need pullup or pull down NO Stuff R515 , R558, R514, R537 (page 02)
	2/12	1. p.40 PR153 from 22 ohm change to 220 ohm for S334/S5 bo bo sound issue.
	3/4	1. p.15 & p.16 L1 & L2 footprint from 0603 changed 0402 2. p.6 Delete UART1 4 pcs TP 3. p.25 EMI request add C807 33p for CLKRUN# 4. p.31 +3vpcu & +5vpcu from MPS NB679 change to TB51225 5. p.24 R420 & R422 vendor suggest from 56 ohm chage to 62 ohm [CS06202JB15]
ZRW REV:C1	4/30	1. p.2 Stuff 10k ohm_4 of R780 & R781. [KBSMI# & EC_SCI#] Pull up to +3V. 2. P.29 U45 EC pin 70 connect to p.30 PU5#8 IDCHG at 3. P.29 U45 EC pin 95 connect to net IOAC_LANPWR# 4. P.06 Add PQ6059 & PQ6060 for EC_RTCRST control set RTC_SRTC_RST# & RTC_RST#
	5/7	1. p.09 removed MPHY_EXT_PWR control power function[Removed U11, R195, R197,C208,C253] 2. p.07 R576 & R572 from value 4.7k change to 2.2k
ZRW REV:C2	5/8	1. p.36 & p37 change new PU6,PU7,PU8,PU9 footprint AOZ5029Q1-5 & partnumber AL005029001 2. p.28 Delete L8,L9,L10,L14,L15,17 EMI Choke footprint
	5/25	1. p.09 R762 [LPM_ZVM_N] & R763 [MSM#] No Stuff dr GT3 2. p.09 add R789 0 ohm for VCCHDA p.24 R365 stuff 0 ohm connect to +3V , R363 0 bm no stuff connect to +1.5v 3. p.34 delete +VCCEOPIO circuit 4. p.05 delete R141 , R133 , R547 for SVID data,Ald#,clk 5. p.39 delete VCCGT_X circuit 6. p.37 delete PR77 & PR88 for VCCGT connect to VCGTX
	5/28	1. p.03 Delete R656 & R189. DDR0_ALERT# & DDR1_ALE# connect to GND 2. p.09 Delete R763 0 ohm for net MSM#.
ZRW REV:C3	6/18	1. p.05 Add C814 1000p/50v_4 connect +1V_VCCST and near R138 SVID. 2. p.36 Add PC6228 1000p/50v_4 connect +1V_VCCST ad near RR341 SVID. 3. p.02 Add R795 , R796 , R797 0ohm for DCI_USB_3 test fixture 4. p.11 delete XDP function connector U27 , U30 CN1 5. p.09 Remove short Jumper for all +1V_S5. 1. R163 , R159 ,R581, R146 ,R149 ,R157 R173 , R151 , R170 , R136 2. R545 , R144 , R150 , R147 , R551 , R557R584 [VCCCLK1~6] 3. R168 [+1_S5 -> V1_MPHY] 6. p.36 remove PR37 Shortpad for SVID_ALERT# 7. p.07 Delete Q33 , R579 ,R583 for SMBus(EC)
	6/23	1. p.02 Delete TP82 and Net [SKTOCC#] 2. p.05 reserve 5 pcs 1000 pF capacitor in +1V_VCCST [C815,C816,C817,C818,C819] , no stuff by default 3. p.09 Reserve test point TP95 for CPU AK13 ball 4. p.32 add PC6230 22u/6.3v_6 in connect to PQ23.1 [+1V_SUS]

 Quanta Computer Inc.		DOC NO.	PROJECT MODEL :	ZWA	APPROVED BY:		DATE:
<div>FileDocument NumberRev 3A</div> <div>Change list</div>			PART NUMBER:		DRAWING BY:		REVISION: