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Analog Circuit for Sound Localization Applications

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Abstract -- We describe an analog CMOS circuit that computes the time (phase) delay between two10 kHz sinusoids. This circuit can be used in sound localization applications. We realize a locking range of 10 - 170 degrees in less than 1 ms that is robust over process variations. Two receivers placed at a distance from one another intercept a sinusoidal waveform emanating from a sound source. The phase difference between the two signals is detected by the circuit, which gives an estimation of the distance of the source from the receivers. This solution is simpler and more elegant than current digital techniques that require specialized DSP hardware to be implemented in real time.

INTRODUCTION

Accurate sound localization of distant sound sources is important for teleconferencing, voice control systems, and robotic navigation. In real acoustic environments, however, background noise and reverberation, can degrade the performance of these systems. Previous works have been reported using microphone arrays and various algorithms to handle these issues [1-3]. Although most phase detection schemes have been implemented using DSP, some methods use analog VLSI technology, providing a more elegant solution for computing time delays between continuous-time signals. The analog circuits proposed by Pu and Harris [4] are all operated in the subthreshold region using CMOS transistors. This offers a wide range of phase detection with a phase locking speed of 10 milliseconds, but biasing the transistors correctly under process variations proves to be very difficult.

This paper proposes a CMOS-based analog circuit that is fairly robust to process variations with a phase detection range of 10^o – 170^o, accurate resolution within 2^o, and a phase locking speed under a millisecond. To obtain these specifications, the circuit must be tuned for a specific input frequency. Although typical speakers are capable of generating sound between 20 Hz and 20 kHz, most average grade microphones cannot pickup frequencies above 10kHz. Based on this acoustic limitation and other circuit limitations that will be discussed later in this paper, the phase detector designed in this paper was tuned for a 10 kHz input.

CONCEPT AND METHODS

The most basic configuration for the localization of a sound source contains a pair of microphones or other

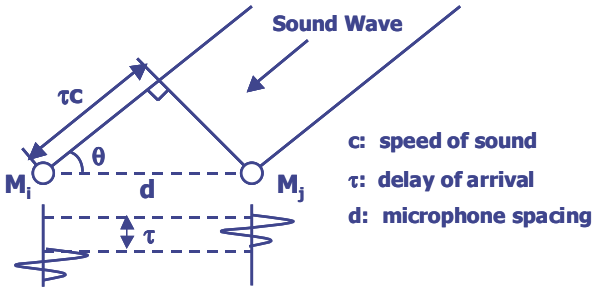

Figure 1: *Sound localization diagram for an incident sound wave on two detectors or microphones.*

detectors. As shown in Figure 1, an acoustic wave emanating from the sound source will be intercepted by the microphones at different times, resulting in a phase difference between the two transduced signals. Given this phase difference and the microphone spacing, the incident angle of the acoustic wave can be calculated:

$$\theta = \cos^{-1}\left(\frac{\tau \cdot c}{d}\right) \qquad (1)$$

where d is the spacing between microphones, τ is the delay of arrival, and c is the sound propagation speed. Arrays of detectors are typically used to obtain more accurate information about the distance and direction of a sound source. Due to the periodicity of the cosine function, the distance between the receivers (d) should be less half the wavelength of the input sinusoid.

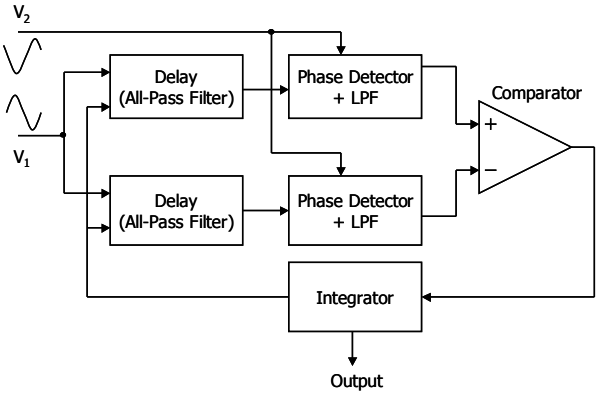

Figure 2: *Block diagram of the phase detector.*

The block diagram of the phase detector is shown in Figure 2. This system includes two delay elements, two multiplier circuits, a comparator, and a capacitor used to store the tuning voltage of the delay elements. Most of the elements of the circuit contain CMOS transistors operating in the saturation region, with the exception of a few transistors operating in the linear

region as resistors. Two input signals, V_1 and V_2, are fed into the system with the assumption that both signals have the same frequency and amplitude, but different phases. The input signal V_1 is sent through two delay elements (Figure 2), each element delaying the signal by two different time lengths. The main goal of the circuit is to adaptively control the two delayed versions of V_1 to make their phases approach the phase of the other input signal V_2. For measuring the phase difference between V_2 and a delayed version of V_1, the two signals are correlated using a multiplier and low pass filter. The multiplication of these two sinusoids having the same frequency ω but different phases ϕ_1 and ϕ_2, results in two components. The first one is a sinusoid with frequency 2ω and phase ($\phi_1 + \phi_2$) and the second one is a DC signal proportional ($\phi_1 - \phi_2$):

$$A\sin(\omega t+\phi_1)\times A\sin(\omega t+\phi_2)= \frac{A^2}{2}[\cos(\phi_1-\phi_2)-\cos(2\omega t+\phi_1+\phi_2)] \quad (2)$$

Passing the resulting sinusoid through a low pass filter with cutoff frequency $f_C << 2\omega$ gives out the DC component, which is a constant proportional to the phase difference of the two signals. The correlated outputs corresponding to the two different delayed versions of V_1 are compared by the Comparator and the result is stored by a capacitor which in turn is used to adjust the tuning voltage of the delay elements.

HARDWARE IMPLEMENTATION

Delay circuit

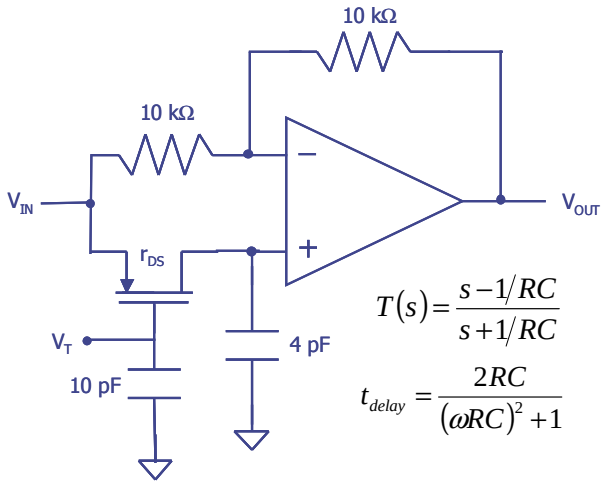

Figure 3: *Circuit schematic of delay block.*

The delay circuit, shown in Figure 2, is implemented with an all-pass filter with a frequency response shown in Figure 3. In order to have a total locking range in excess of 160°, the delay circuit has to have that much tuning range. The main design issues for the delay block are: (1) tuning range (RC_{max}/RC_{min}) of ~100 (two decades) to get phase delays from near zero to 180 degrees, (2) implementation of large resistance or capacitance using minimal die area to realize these phase delays at low frequencies, and (3) robustness against process variations.

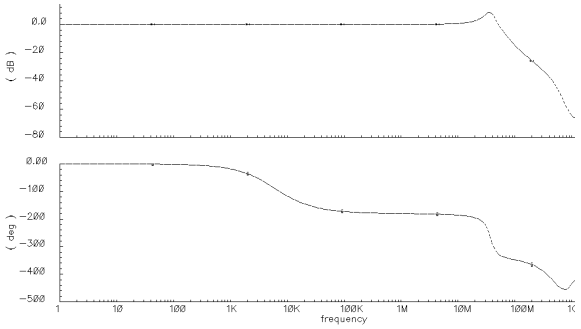

Figure 4: *Frequency response of the all-pass filter.*

These stringent requirements in modern MOS fabrication technology were realized using a 4pF capacitance and a variable resistor implemented through a transistor operating in the triode region. This solution proves to be a better alternative than using varactors or switched capacitors. In the linear region, the MOS drain source resistance is expressed as

$$r_{ds}=\frac{1}{k_n'\left(\frac{W}{L}\right)(v_{gs}-V_{TH})}. \quad (3)$$

In the sub-threshold region this changes to

$$r_{ds}=\frac{v_{ds}}{I_0\left(\frac{W}{L}\right)e^{\frac{qV_{GB}}{kT}}\left(e^{-\frac{qV_{SB}}{kT}}-e^{-\frac{qV_{DB}}{kT}}\right)}, \quad (4)$$

an exponential relationship with v_{GB}. We take advantage of this relationship to achieve large tuning ranges of around 100. This large variation in MOS resistance helps realize phase delays from 10 to 170 degrees for the 10kHz input signal, as shown in Figure 5.

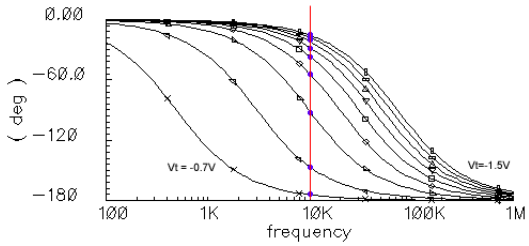

Figure 5: Phase response of delay circuit for several tuning voltages in 0.1 V increments.

Phase Detector

The phase detector circuit was implemented using a four-quadrant Gilbert cell multiplier and low-pass filter. Since we use the DC component of the Gilbert cell output to decide whether the phase delays introduced by the delay blocks to the first input are sufficient or not, a low pass filter (LPF) is needed to attenuate the sinusoidal component at 20kHz. The LPF has been implemented using a first-order RC topology. Design of the low pass filter posed a problem similar to the one faced in design of the delay block. The value of resistance and capacitance required for implementing the LPF were far too large to be economically realizable in modern fabrication processes. We, therefore, used transistors in the linear region to achieve a high resistance value, on the order of 10MΩ. Using a reasonably sized capacitance yielded a LPF with 1.2 kHz cutoff frequency.

Comparator & Integrator

The outputs of the two Gilbert cells after passing through the LPF are fed into the comparator (Figure 2). Since the inputs to the delay blocks have to vary from –1.5 to –0.7 Volts, the output of the comparator was constrained to be in this region. The output of the comparator is fed back to the variable resistance of the all pass delay circuit through an integrator, which is implemented using a capacitor. To prevent large oscillations in the feedback circuit (ping pong effect), a damping element in the form of a resistor is introduced before the capacitor. This resistor is again implemented using a linear region NMOS. Since the gate of this MOS transistor is tied to ground, the voltage at the integrator can't rise above the threshold voltage, $-V_{tN}$, of the transistor. Very importantly, the voltage to be fed to the transistor in the delay block should be in the same range. This overall arrangement insures that the circuit does not go outside its locking range. The initial state too is near the locking state which minimizes the locking period.

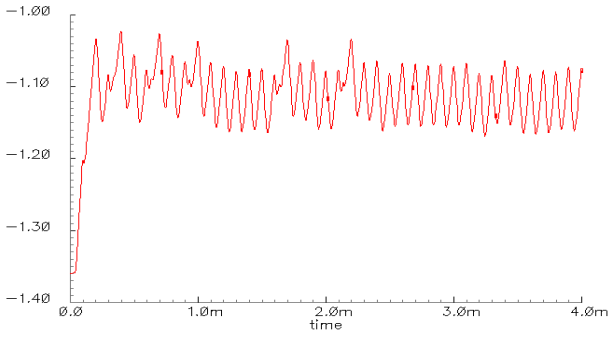

Figure 6*: Output of complete circuit given a two 10 kHz input signals 45^o out of phase. Acquisition time to a stable tuning voltaae is less than 1 millisecond.*

SYSTEM SIMULATION

Putting all the blocks together, we went ahead with simulating the complete circuit. Different phase delays were given the two input sinusoids (200mV peak to peak). The output voltage was measured from the integrator. A simulation output for a phase difference of 45 degrees between the input signals is shown Figure 6. As can be observed, the output does not settle to a DC value, but rather is a sinusoid at the same frequency as the input signals with a constant DC offset. Low pass filtering of this signal is required to get the average DC output voltage.

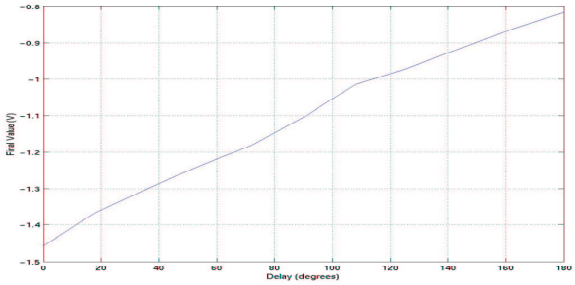

Figure 7: Plot of DC output voltage vs. input phase difference of two 10 kHz sinusoidal inputs. The output characteristic is almost a straight line between phase and output voltage.

The acquisition time for the circuit is around 1ms, which is a significant improvement from 10ms, previously reported [5]. A plot of the DC output voltage with respect to the phase difference between the two input sinusoids is shown in Figure 7.

The total noise created by the circuit devices at the input of the comparator was 42.4mV. Before entering into the comparator the signal passes through a low pass filter, so the high frequency components of the noise are already filtered out and we get a smaller noise voltage after the LPF than the one before it. This low noise floor ensures proper operation of the circuit even when considering circuit noise.

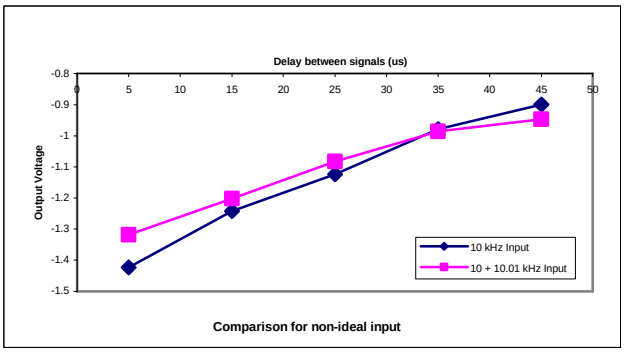

Figure 8*:* Output voltage vs time delay for a pair of 10 kHz and 10.01 kHz sinusoidal inputs. The output voltage swing degrades for the non-ideal input case. However, the **v**oltage-phase difference characteristics follow the same straight-line characteristics as for the ideal case.

Corner Simulations

The performance of the circuit with respect to some of the process corner variations is shown in the figures below. In all these figures, the red line is for the case when the corner variable is at its low value, the blue for the nominal one and magenta for the high corner case.

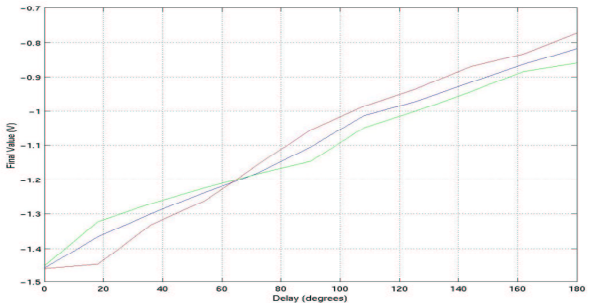

Figure 9*: Phase delay vs. output voltage for varying temperatures for 0, 25 and 70 degree centigrade.*

The deviations in curves in figure 9 could be explained using the temperature dependence of the MOS transistor currents in the linear and sub-threshold region.

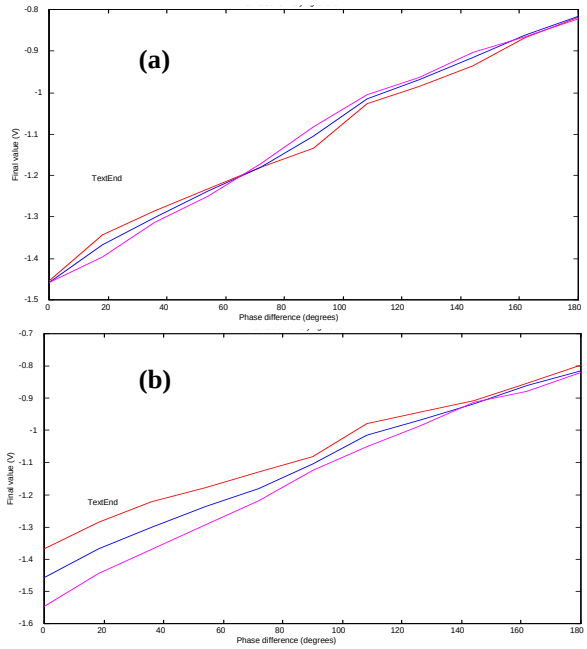

Figure 10*: Circuit output vs. phase delay for varying (a) oxide thickness for nominal and +/- 10% change; (b)Vtp for 0.6, 0.7 and 0.8 Volts*

Though there are variations in output voltage with variations in some process parameters, the effect can be offset by adding a constant delay to the signal moving in one branch of the circuit. Thus, we would still continue to get the same output voltage versus phase difference curves after tuning the circuit when the design is used in industrial production.

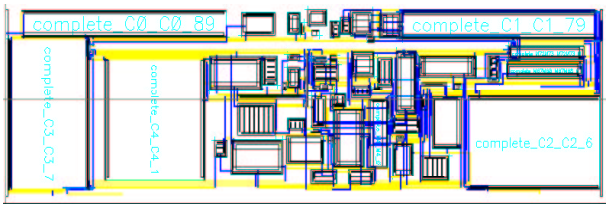

Figure 11*: Layout of the circuit.*

CONCLUSION

In this paper, the design of a phase locking circuit was accomplished for sound localization applications. The problem of large passive devices was tackled by implementing large resistances through transistors operating in linear region. The circuit is fairly robust to process corners and has a linear output voltage characteristics with respect to phase differences in the input signal. The locking time achieved was less than 1 millisecond. The circuit can be implemented in the "ears" of a robot so that the robot may detect the direct and distance of the source of sound that is calling it. Similar implementations at different operating frequencies can find applications in SONAR and other acoustic devices.

REFERENCES

[1] Nishiura et al., "Localization of Multiple Sound Sources Based on a CSP Analysis with a Microphone Array," IEEE 2000.

[2] Grech et al, "Low Voltage SC TDM Correlator For the Extraction Of Time Delay," IEEE 2000.

[3] Pu and Harris, "A Continuous Time Analog Circuit for Computing Time Delays Between Signals," IEEE International Symposium on Circuits and Systems, 1996.

[4] Sakamoto, et al, "DSP Implementation of a 3D Sound Localization Algorithm for Monaural Sound Source, " IEEE 2001.

[5] Mead, "Analog VLSI and Neural Systems" Addison-Wesley, 1989.