CMOS Logic ICs
Usage Considerations

Outline:

This document explains notes on using CMOS logic ICs, methods of prevent latch-up, load-capacitance effects, unstable outputs (hazards and meta-stable outputs), and decreasing various noise effects (switching noise, reflected noise, and crosstalk noise) by pattern design.

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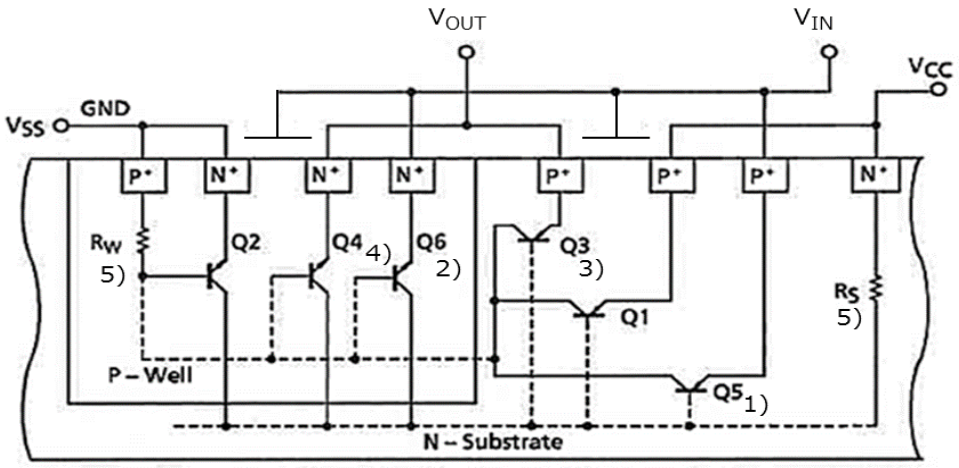
1. Latch-up

A latch-up is a phenomenon specific to CMOS integrated circuits that originates from the formation of a silicon-controlled rectifier (SCR) during normal operation. A common cause of a latch-up is excessive noise, surge voltage, or surge current on an input or output pin of a CMOS IC. Another cause is a sharp change in the supply voltage. In such cases, even if the triggering signal is disconnected, an excessive current continues flowing between V_{CC} and GND, eventually leading to the destruction of the IC. Once a latch-up occurs, an excessive current persists until the V_{CC} supply is removed or decreased. Otherwise, a latch-up results in the burnout of internal bonding wires or the destruction of a component.

1.1. Causes of a latch-up

Figure 1.1. shows an equivalent circuit of a CMOS circuit, including its parasitic structure. An NPN transistor (Q2) is formed in the P-well on the n-channel MOS side and a PNP transistor (Q1) is formed in the N-substrate on the p-channel MOS side. Parasitic resistance also exists between IC pins. Look at the current paths through the parasitic elements shown in this figure. The parasitic structure is equivalent to a thyristor. For example, if current flows into the N-substrate because of an external cause, a voltage drop occurs across resistor R_s in the N-substrate. As a result, Q1 turns on, causing current to flow from V_{CC} to GND via resistor R_w in the P-well. The current flowing through R_w produces a voltage difference across R_w, which turns on Q2, causing supply current to flow via R_s. Since this further increases the voltage difference across R_s, Q1 and Q2 remain on. Consequently, the supply current continues increasing. As described above, CMOS ICs suffer from a latch-up problem when voltage differences occur across R_w in the P-well and R_s in the N-substrate. The causes of a latch-up are as follows.



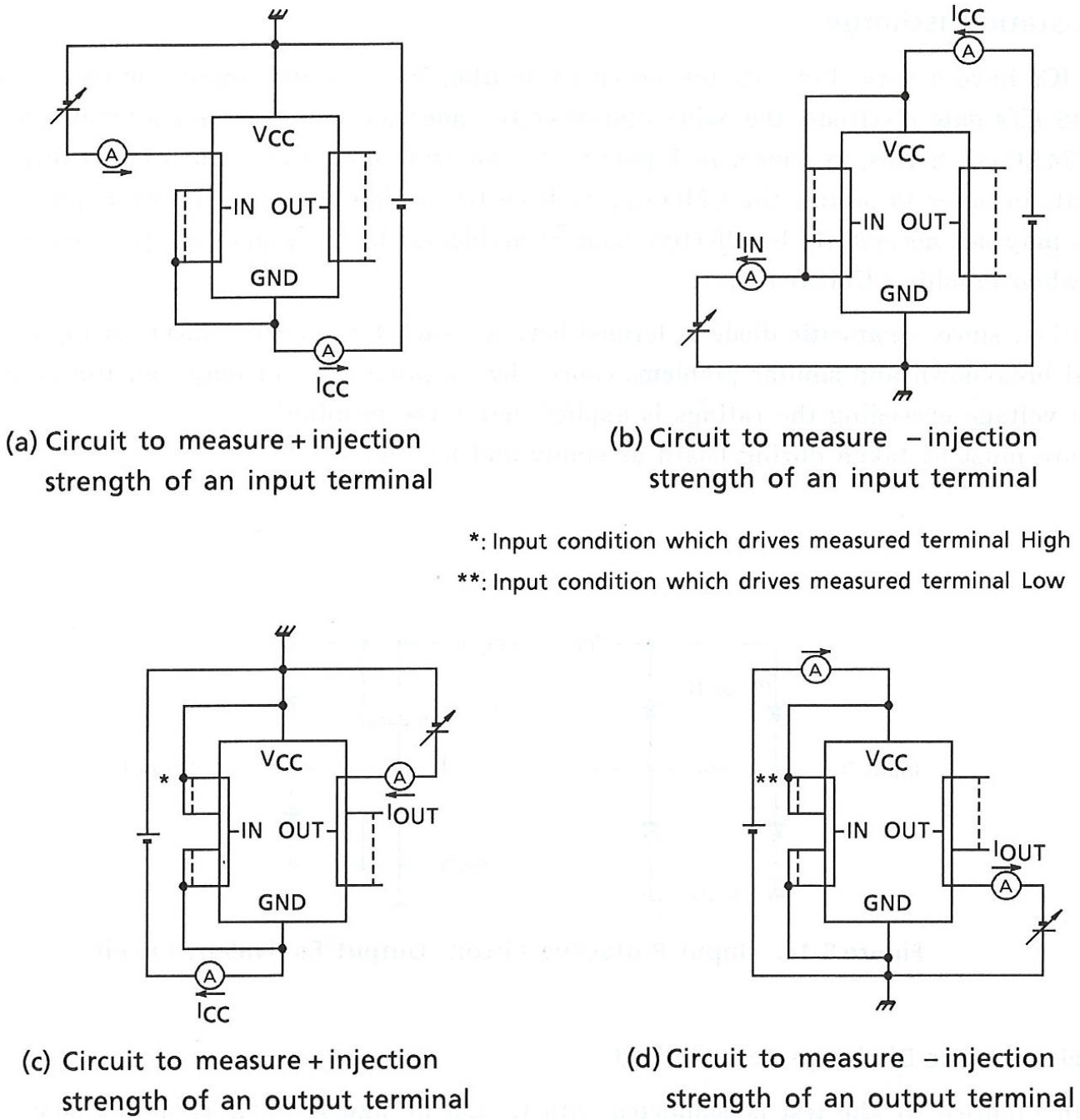
1) Input voltage (V_{IN}) higher than (V_{CC} + V_F): Q5 turns on.
2) Input voltage lower than (V_{SS} – V_F): Q6 turns on.
3) Output voltage (V_{OUT}) higher than (V_{CC} + V_F): Q3 turns on.
4) Output voltage lower than (V_{SS} – V_F): Q4 turns on.
5) Supply voltage exceeding the V_{CC} rating, leading to a breakdown of an internal junction (Current directly flows to either R_w or R_s.)
(V_F is the forward base-emitter voltage of parasitic bipolar transistors Q3 to Q6.)

Figure 1.1 Equivalent circuit of a CMOS IC and a latch-up operation

1.2. Measuring latch-up immunity

Figure 1.2 shows several test circuits for latch-up immunity.

A latch-up immunity test provides positive or negative current injection via an input or an output to trigger a latch-up and measures the current (I_{IN} or I_{OUT}) when a latch-up occurs.



(a) Circuit to measure + injection strength of an input terminal

(b) Circuit to measure − injection strength of an input terminal

*: Input condition which drives measured terminal High

**: Input condition which drives measured terminal Low

(c) Circuit to measure + injection strength of an output terminal

(d) Circuit to measure − injection strength of an output terminal

Figure 1.2 Latch-up immunity measurement through current injection

1.3. Latch-up prevention

Since Toshiba's standard CMOS logic ICs provide sufficient margins for latch-up, you can use them in the same environment as for bipolar ICs (74LS series) that are intrinsically free from latch-up. Toshiba's CMOS logic ICs are immune to latch-up under the rated conditions, but it is recommended to add a protection circuit to the IC interface as shown in Figure 1.3 if an excessive surge might be applied to the IC.

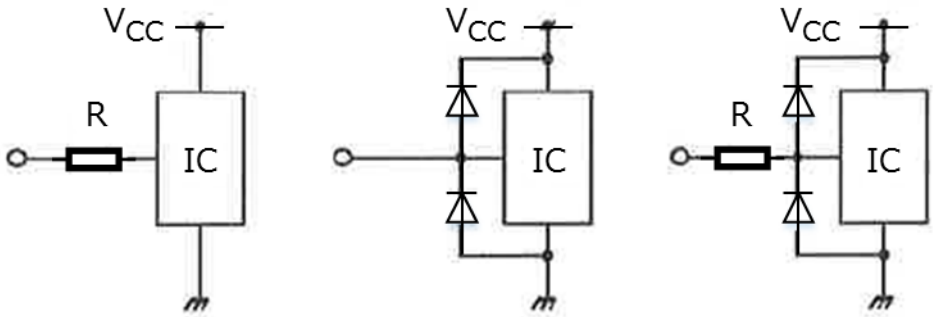


Figure 1.3 Examples of measures to prevent latch-up

2. Load capacitance (capacitors connected to a signal line and either V_{CC} or GND)

When an output pin of a CMOS IC is connected to a large load capacitance, its propagation delay increases. In addition, the increased charge/discharge current into or out of the capacitor might cause noise or a bonding wire burnout. Since current flows to the output parasitic diode at power-down, a CMOS IC should not be connected directly to a large load capacitance.

If it is necessary to connect a capacitor directly to the output of a CMOS IC in order to increase its delay time or filter out noise, its capacitance should be 500 pF or less. When a larger capacitor is required, a current-limiting resistor (R) should be connected between the IC output and a capacitor as shown in Figure 2.1.
CMOS ICs with an output-tolerant function do not need a current-limiting resistor (R) for power-down. However, a current-limiting resistor (R) might be necessary to limit the flow of charge current into the capacitor.

When a capacitor is discharged as a result of power-down, current flows to an internal protection diode and is returned to V_{CC} via the input pin. Therefore, a large load capacitance should not also be connected directly to an input pin. A capacitor of up to 500 pF may be connected directly to the input of a CMOS IC, but when a larger capacitor is required, a current-limiting resistor (R_S) should be connected between the IC input and a capacitor as shown in Figure 2.1.
CMOS ICs with an input-tolerant function do not need a current-limiting resistor (R_S).

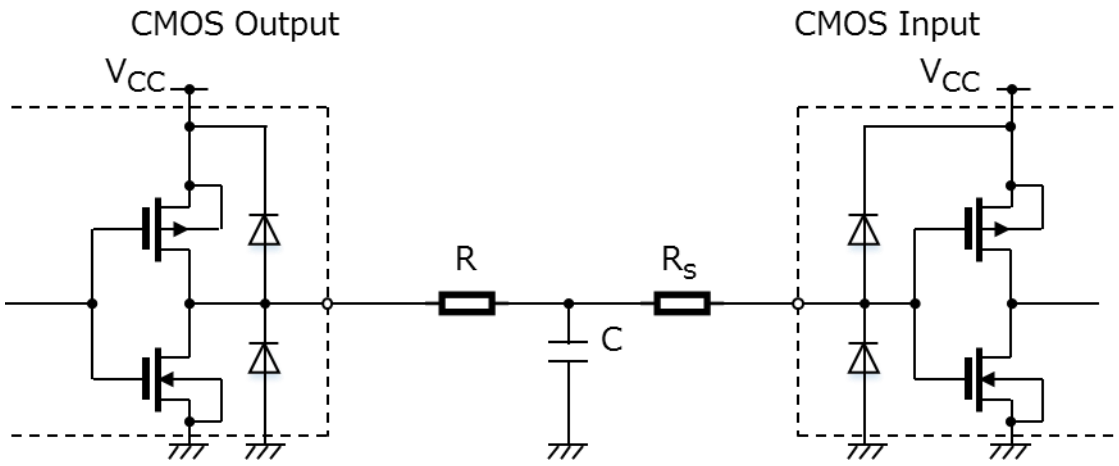


Figure 2.1 Connecting a large load capacitance

3. Inputs with large rise and fall times (slowly changing inputs)

The V_{CC} and GND lines of a CMOS IC are susceptible to ripple during switching transitions because of shoot-through and output currents. If a slowly changing signal is applied to the input, a CMOS IC might malfunction because of the effect of ripples. To prevent malfunction, the input rise and fall times must be kept within the recommended operating conditions. Use ICs with a Schmitt-trigger input for a slowly changing input.

4. Types of noise to be noted: a) switching noise, b) signal reflection, and c) crosstalk noise

Care should be exercised as to switching noise when using CMOS logic ICs.
Major types of noise include:
(a) Switching noise (overshoot, undershoot, ground bounces)
(b) Signal reflection
(c) Crosstalk noise
See Figure 4.1. Each type of noise is detailed in the following subsections. These types of noise are caused by the output slew rate (di/dt or dv/dt) and the output trace.
Care should also be taken as to electromagnetic interference (EMI) noise generated under multiple combined conditions and electromagnetic susceptibility (EMS) noise emitted by nearby electronic devices.

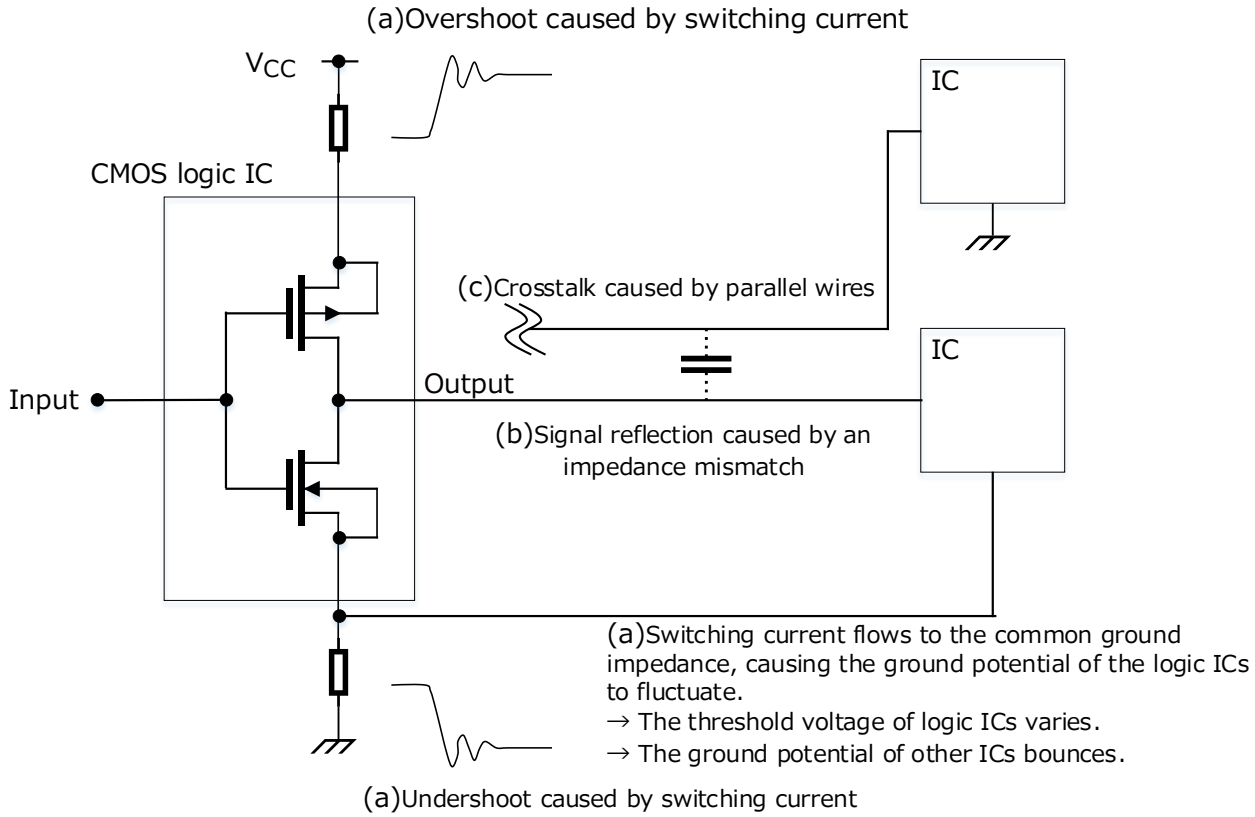


Figure 4.1 Types of noise

4.1. Switching noise

The MOSFETs in a CMOS logic IC make switching transitions while charging and discharging internal and external load capacitances. The trace impedance during switching can be regarded as an LCR circuit. Since the switching current (i) flows through inductance (L), a spike voltage (=L(di/dt)) appears on the V_{CC} and GND lines of the CMOS logic IC. This noise is called switching noise.

Multiple simultaneously switching outputs draw a large charge/discharge current and therefore cause a large switching noise (called simultaneous switching noise). The following lists the measures for the reduction of switching noise.

Measures to reduce switching noise:

- Increase the width and reduce the length of V_{CC} and GND lines to reduce their inductance.
- Place a bypass capacitor between and as close as possible to the V_{CC} and GND pins of the CMOS logic IC (Figure 4.2).
- Exercise care as to clock and reset signals. Unused inputs of gates such as drivers should be connected to either V_{CC} or GND. Connect a low-pass filter to the output of used gates to remove noise.
- Select low-noise ICs.
- Add a damping resistor to the output of used gates (Figure 4.3). It is necessary to adjust the value of the damping resistor by checking the output waveform. (* Toshiba provides CMOS ICs with an internal damping resistor (Figure 4.4), which help reduce not only switching noise but also parts count.)

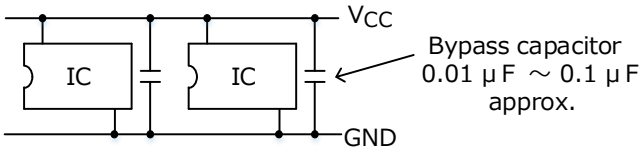


Figure 4.2 Bypass capacitor

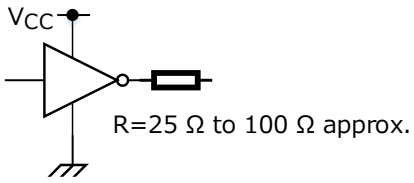


Figure 4.3 Damping resistor

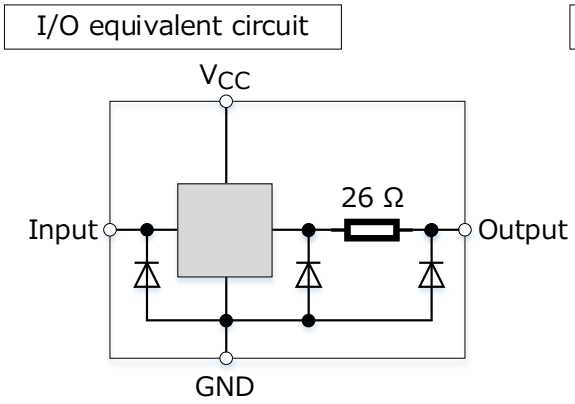


Figure 4.4 CMOS ICs with an internal damping resistor

4.2. Signal reflection

In the case of high-speed CMOS logic ICs, reflections cause an increase in the signal delay, ringing, overshoot, and undershoot.

Reflections in transmission lines:

Typical traces have a characteristic impedance(*1) of 50 to 150 Ω. However, the I/O impedance of high-speed CMOS logic ICs differs from the typical characteristic impedance of traces. This impedance mismatch causes part of the transmitted signal to be reflected to both the transmitting and receiving ends of a transmission line. Signal reflection does not affect a slowly rising output because its rise period overlaps that of the reflected signal. Signal reflection causes a problem when the reflected signal returns to the output after it rises, i.e., when the following equation is true:

$t_r < 2T$

t_r: Rise time of the output signal

T: Propagation delay time from the transmitting end to the receiving end of a transmission line

Suppose that the output rise time is 3 ns and that the propagation delay time along a transmission line is 5 ns/m. Then, signal reflection has a significant impact when the transmission line is 60 cm or longer. The following lists the measures for signal reflection.

Measures for signal reflection:

- Increase the board assembly density and reduce the length of board traces to reduce their inductance and capacitance. In this case, however, care is required as to crosstalk between adjacent traces. (See Section 4.3 for crosstalk.)
- Do not use ICs with an output current higher than necessary.
- Provide electrical termination so that the I/O impedance of a CMOS logic IC matches the characteristic impedance of the transmission line (Figure 4.5).
- When the output of a CMOS logic IC drives multiple CMOS logic ICs, the output trace should be fanned out close to the driven ICs. (Figure 4.6).

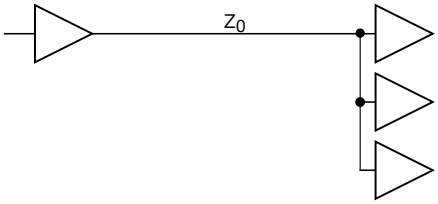


Figure 4.6 Impedance of trace

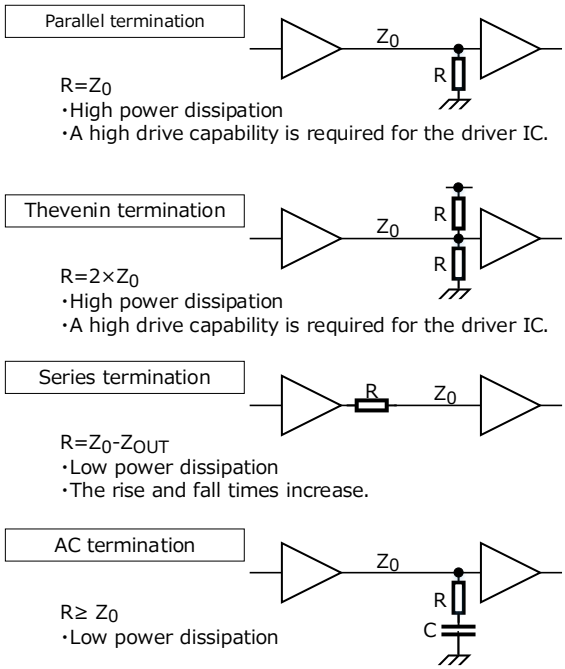


Figure 4.5 Examples of electrical termination

*1 Characteristic impedance

The characteristic impedance is one of the characteristics of a transmission line (e.g., board trace, coaxial cable).

The general expression of the characteristic impedance of a transmission line is $Z_0 = \sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. The unit of characteristic impedance is ohm (Ω).

When a termination resistor of 50 Ω is connected to the end of a transmission line with a characteristic impedance of 50 Ω, signal reflection does not occur at the connection point. However, if the characteristic impedance does not match the resistor value, signal reflection occurs at the connection point.

4.3. Crosstalk noise

Crosstalk noise is induced by capacitive or inductive coupling between two adjacent transmission lines that run in parallel. Regarding crosstalk, care should be exercised as to rapidly rising or falling signals.

When such a signal travels through a transmission line, crosstalk noise is induced in an adjacent line (victim) and propagates in both directions: in the same direction as for the aggressor signal and in the direction opposite to it.

Since the speed of crosstalk propagation is equal to that of the aggressor signal, the crosstalk noise that travels in the same direction as the aggressor signal (called far-end crosstalk) appears as pulse-like noise. On the other hand, the crosstalk noise that travels in the opposite direction (called near-end crosstalk) maintains a constant level while the aggressor signal propagates along the line.

Crosstalk noise also propagates along the aggressor line and then returns to the victim line.

Generally, you can prevent crosstalk as follows.

Measures for the prevention of crosstalk:

- Add earth traces between parallel traces.
- Reduce the length of traces that run in parallel.
- In the case of a multi-layer board, run traces on alternate layers orthogonally to each other (Figure 4.7).
- Increase the spacing between traces.

Figure 4.8 shows a typical level of crosstalk noise traveling along 30-cm traces.

This example shows near-end crosstalk. When the near end of the victim trace is the receiving end, it is susceptible to the effect of crosstalk.

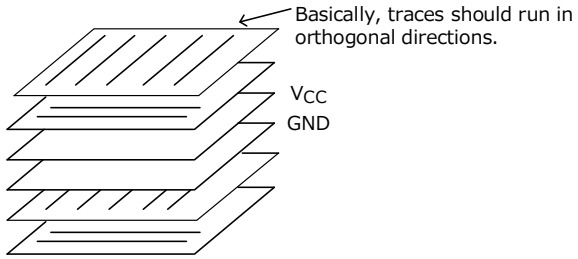
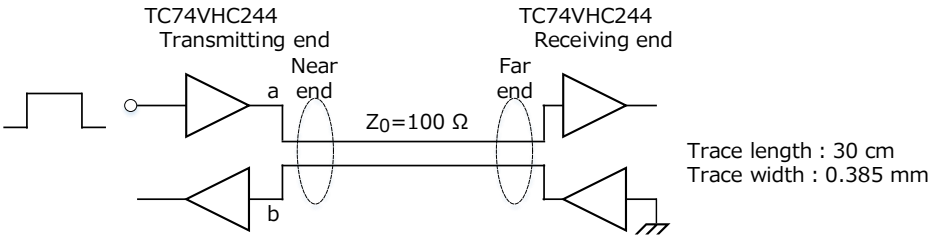


Figure 4.7 Multi-layer board



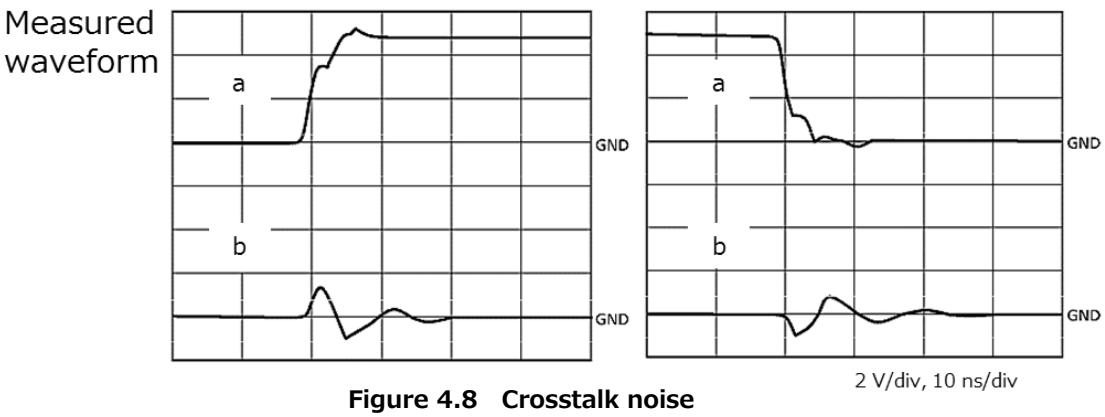


Figure 4.8 Crosstalk noise

5. Phenomena that cause an output to become unstable

Hazards and metastability momentarily cause a wrong change in the output of a CMOS logic IC, resulting in a circuit malfunction.

A hazard occurs in logic circuits with multiple inputs and a metastability occurs in sequential circuits such as flip-flops.

Section 5.1 describes hazards and Section 5.2 discusses metastability.

5.1. Hazards

In the case of multiple-input combinational logic consisting of OR, AND and other gates, a slight difference in the timing of input signal changes causes a brief whisker-like pulse called a hazard.

Using the circuit shown in Figure 5.1, let's see how a hazard occurs because of a difference in signal delays. Suppose that a rising signal transition occurs simultaneously at A and B. The signal applied to B reaches the AND gate via an inverter. Since the signal that enters the AND gate from B is delayed by an inverter, the AND gate receives input signals A and C at different timings, potentially producing a High pulse at the Y output.

To prevent hazards, combinational logic should not be designed to produce a desired output value from simultaneous changes in its inputs. Using a flip-flop to adjust the output timing also helps eliminate a hazard.

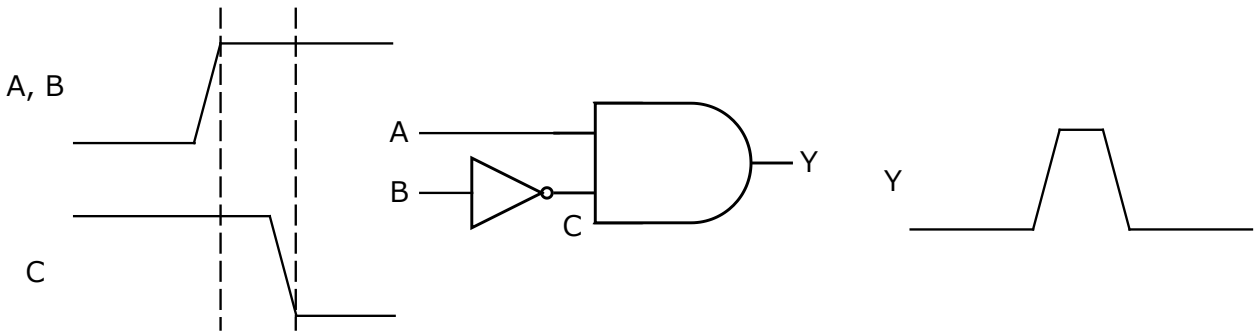


Figure 5.1 Example of a hazard caused by multiple logic gates

In addition to a signal timing difference, a slowly changing input can be a cause of a hazard. Hazards due to a slowly changing input can be prevented by using a logic gate with a Schmitt-trigger input.

5.2. Metastability

The output of a synchronous sequential circuit can potentially persist in an unstable equilibrium called a metastable state, depending on the timing of a data signal to be latched relative to the clock signal.

A sequential circuit enters a metastable state when its input setup and hold time (t_s and t_h) requirements shown in the datasheet are not satisfied.

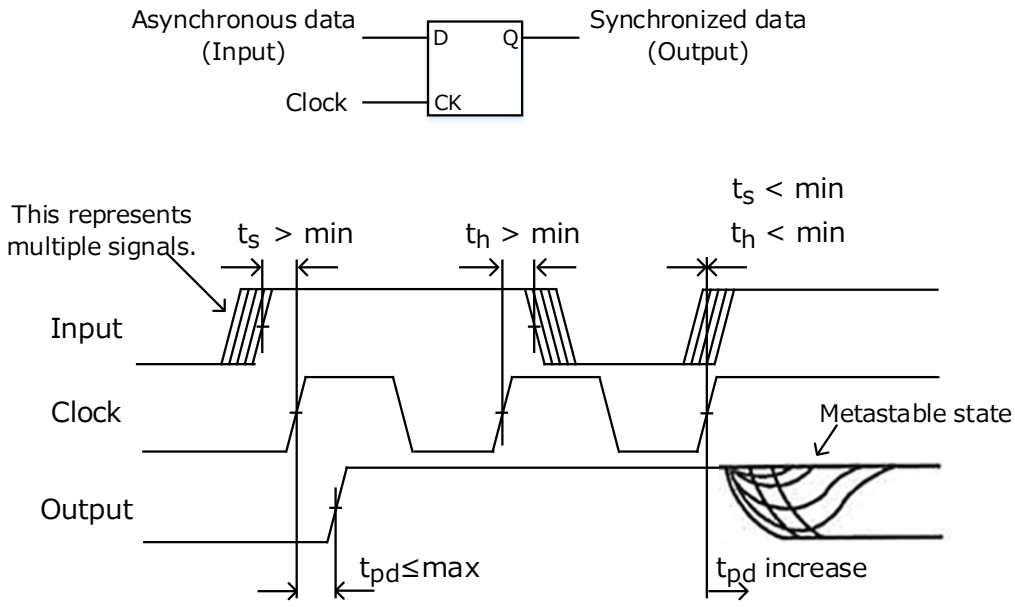


Figure 5.2 Metastable state

Figure 5.2 illustrates metastability, which causes t_{pd} to become longer than expected or causes the output to toggle back to the initial logic value.

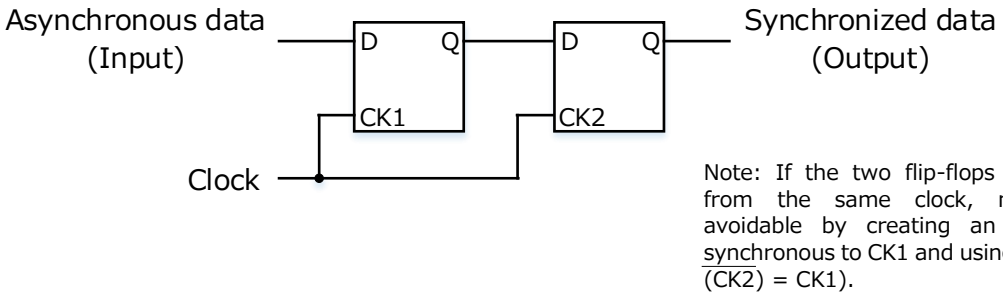
Metastability potentially occurs when an active input (e.g., a clock signal) and a passive input (e.g., a data signal) are asynchronous to each other.

To prevent sequential circuits from entering a metastable state, the recommended timing conditions shown in the datasheet must be satisfied.

For example, when the CK and D inputs are asynchronous, they can be synchronized as shown below. In this case, however, care should be exercised as to the cycle period and propagation delay of CK. If they are close, the data signal might not propagate to the second flip-flop.

The synchronizer shown in Figure 5.3 consists of two flip-flops. The first flip-flop prevents an increase in t_{pd} and a hazard from being transferred to the output of the second flip-flop.

Even in this case, care is needed when the phase difference between CK1 and CK2 is close to the CK-to-Q delay (t_{pd}) of the first flip-flop.



Note: If the two flip-flops cannot operate from the same clock, metastability is avoidable by creating an inverted clock synchronous to CK1 and using it as CK2 (e.g., $\overline{CK2}$ = CK1).

Figure 5.3 Synchronizer to prevent metastability

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