MULTIMEDIA UNIVERSITY

SECOND TRIMESTER, **SESSION 2022/2023**

ASSIGNMENT

EEN6223 – ELECTRONICS 2

(All sections / Groups)

INSTRUCTIONS TO STUDENTS

1. This is a group assignment (2 students per group, from the same majoring).
2. Complete ALL questions.
3. Submission is due by 5pm on 24th May 2024 (Friday).
4. Write your **name, student ID,** and **major** clearly on this cover page of your submission. Incomplete information might result in mark deduction.
5. Plagiarism is a very serious offense. ZERO mark will be given if any acts of plagiarism detected.

No.	Name	ID	Major
1.			TE / RE
2.			TE / RE

Objectives:
- To gain an understanding of electronic circuit design procedures.
- To develop a working knowledge of CAD tools and device models.
- To compare theoretical performance with simulated results.
- To design electronic circuit to meet specific application requirements.

Instructions to students:

1. This assignment consists of **TWO (2)** questions. Answer **ALL** questions. Marks allocation for each part of the questions is indicated in the questions. The total marks of this assignment will be scaled to 10% for the assignment.

2. Students are required to work in group of **TWO (2), from the same majoring (Both TE/Both RE)**. Each group shall submit 1 report only. Submit both the **PSPICE/LT-SPICE etc. design files** (softcopy), **Short Video Clip** recording the students works (5 minutes, <20MB size) and **softcopy report, all in a zipped file**.

3. All schematic diagrams and simulated graphs/waveforms must be printed using **PSPICE/LTSPICE or whatever simulation software you think it is deeming fit.** Before printing the schematic diagram, remember to enter the **student names** in the title box (at the bottom corner of the schematic entry window). Untidy works and submission might result in mark deduction.

4. Any form of plagiarism identified will render the student to obtain **ZERO** marks.

Problem 1: **[10 marks]**

Design a Junction Field Effect Transistor (JFET) amplifier that meets the required specifications. Heavy emphasis is placed on the theory and comparison with simulation results.

Required Specifications:
Voltage Gain: > 10
Input Resistance: >100 kΩ
Load Resistance: 100 kΩ
Supply Voltage: 30 V
Output Voltage Swing: > 10 V peak-to-peak
Operating Frequency: 1 kHz

Design Procedure:

1. Select a suitable JFET.
2. Design the amplifier by hand. Using the datasheet values,
   (i) Choose a value for I_D(max) for the case of $I_{DSS(max)}$ and $V_{P(max)}$
   (ii) For the case of $I_{DSS(min)}$ and $V_{P(min)}$, choose I_D(min) to be 80% - 90% of I_D(max)
   (iii) Perform hand-analysis to find the required biasing resistors and coupling/ bypass capacitors
   (iv) Analyse the voltage gain and output voltage swing for the two extreme cases ($I_{DSS(max)}$ - $V_{P(max)}$, and $I_{DSS(min)}$ - $V_{P(min)}$). If the required specifications cannot be met, go back to step (i), choose a new value for I_D(max) and repeat the design process.
3. Using PSPICE software, simulate the amplifier performance. Make computer printout of the schematic diagram, with DC voltages and currents at every node indicated. Also produce a plot of input and output voltage waveforms at 1 kHz, with the amplitude of the sinewave signal source set to a value that gives maximum voltage swing at the load resistor without noticeable distortion.
4. Compare the hand analysis and the simulated results. The PSPICE transistor model uses fixed values of I_{DSS} and V_P. The simulation results will not match the hand analysis but they should fall in between the two extreme cases.
5. Write a hand-written report, documenting your design decisions, hand analysis and simulated results. Include schematic diagram and plot of simulated result.

Note:

- ✓ DC voltage and current values can be obtained by enabling bias voltage display and bias current display in the schematic window.
- ✓ By checking "Detailed Bias Point." option in the transient analysis setup, g_m can be viewed in the simulation output file (*.OUT).
- ✓ A_V can be obtained by dividing output voltage at R_L by its corresponding input voltage V_i.

Problem 2: **[10 marks]**

Design a BJT amplifier that meets the following specifications.

Specifications:
Voltage gains: $A_{v\,mid} = V_o/V_i \approx -73$, $A_{vs\,mid} = V_o/V_s \approx -55$
Input resistance: $Z_i = 2455\ \Omega$
Load resistance: 3.3 kΩ
Input signal: 1 mV peak
Lower cutoff frequencies: $f_{LS} \approx 103$ Hz, $f_{LC} \approx 38$ Hz and $f_{LE} \approx 750$ Hz
Higher cutoff frequencies: $f_{Hi} \approx 278$ kHz and $f_{Ho} \approx 2.73$ MHz

Design Procedure:

1. Perform hand-analysis to find the required biasing resistors and coupling/ bypass capacitors
2. Using **PSPICE/LTSPICE or whatever simulation software you think it is deeming fit**, simulate the amplifier performance. Make computer printout of the schematic diagram, with DC voltages and currents at every node indicated. Also produce plots of V_o/V_s and $|A_v/A_{v\,mid}|$ (dB).
3. Compare the hand analysis and the simulated results.
4. Write a hand-written report, documenting your design decisions, hand analysis and simulated results. Include schematic diagram and plot of simulated result.

(Note: Please refer to Chapter 11 of R. L. Boylestad and L. Nashelsky "*Electronic Devices and Circuit Theory*", Prentice-Hall, for examples on simulation using PSpice software)

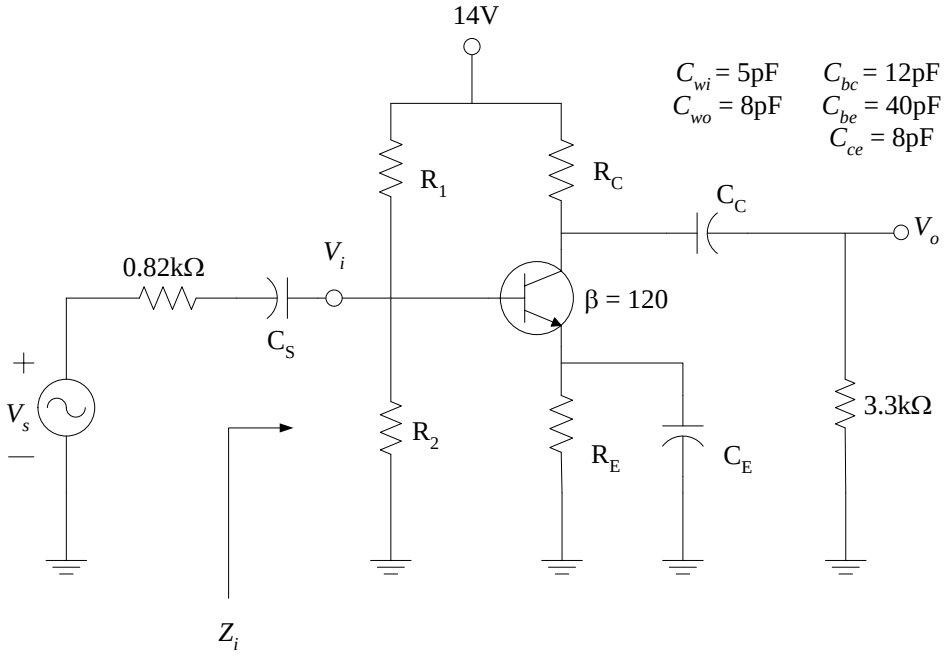

Fig. 2