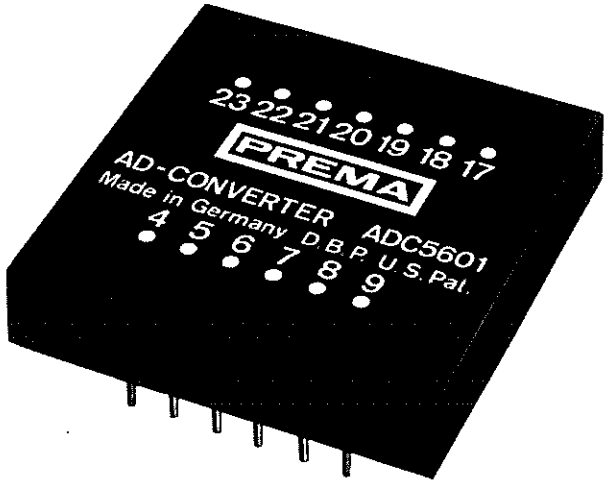
INSTRUMENTS

PREMA




# ADC 5601

## 25-BIT ANALOG-TO-DIGITAL CONVERTER

- 25 BIT RESOLUTION
- NON-LINEARITY 0.0001 %
- OPTIMUM MATCHING TO MICROPROCESSOR
- RESOLUTION AND CONVERSION SPEED CONTROLLED BY MICROPROCESSOR
- FOR APPLICATIONS REQUIRING HIGH RELIABILITY AND COMPACT CONFIGURATION

DESCRIPTION

The ADC 5601 is a high-performance analog to digital converter with up to 25 bit resolution. This converter operates according to the integrating PREMA multiple ramp procedure (U.S. Pat, Germ. Pat). The converter is suitable for numerous applications because it permits optimum hardware and software matching to a microprocessor.
The microprocessor software determines the conversion time, the resolution and the error correction. The residual non-linearity is less than 0.0001 % and the typical temperature coefficient is 0.5 ppm/°C, making the ADC 5601 a top performance device. It has been designed for negative polarity input voltages and positive polarity reference voltages.

The ADC 5601 is designed for unipolar or bipolar applications programable only by external connections. REF IN is the reference voltage input for a high stability reference of approx. 7 V. $Vx_1$ is a negative input voltage in the range of 0 to −5 V (unipolar) or from −2.5 V to +2.5 V (bipolar). For bipolar applications a negative high stability reference of −2.5 V is required at the $Vx_2$ input. For offset adjustment a series resistor $R_V$ may be connected to this input.

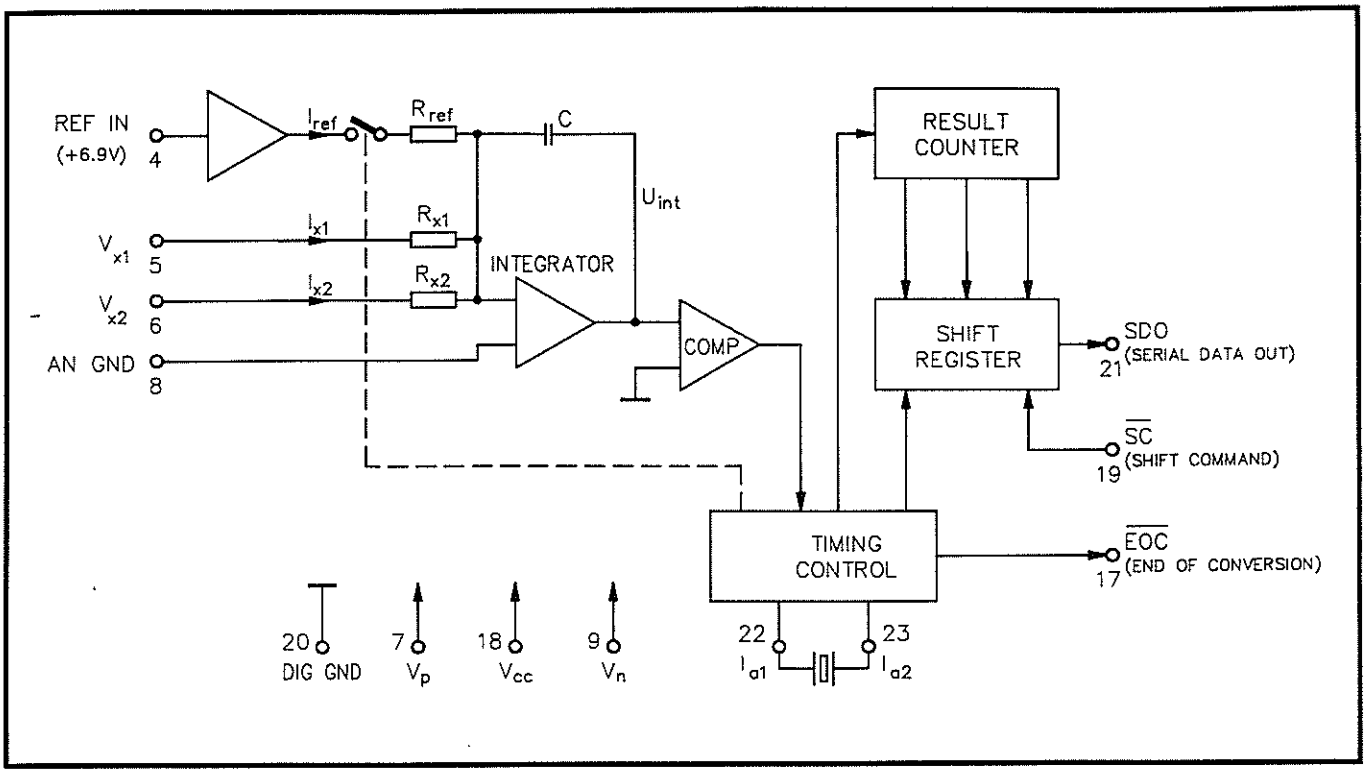



FIG. 1: SIMPLIFIED BLOCK DIAGRAM

## MEASURING PRINCIPLE

The PREMA multiple ramp method for analog to digital conversion (German patent No. 2114141, U.S.Pat. No. 3765012) is used in the ADC 5601. It is the basis for a reliable high resolution AD-converter with outstanding linearity and long-term accuracy, with continuous integration of the measured signal to cancel any interference, without falsifying breaks.

An amplifier which operates as integrator with the capacitor C (fig. 1) continuously integrates a current $I_e$ which is proportional to the input voltage $Vx_1$ being measured. This procedure has inherent high linearity, because it does not require periodic switch off of the input voltage. Errors dependent on the input voltage level, as they are usually generated by switching capacitances, do not occur in this case.

The capacitor is periodically discharged (fig. 2) by a current $I_{ref}$ from a reference voltage source $U_{ref}$ (discharge times $T_1$ to $T_n$), which has opposite polarity with respect to the signal voltage being measured. The end of a down integration is defined by coincidence of comparator response and a pulse flank of the clock oscillator. The total change of charge on the capacitor during one measuring cycle is zero.
This means that the sum of the discharge times $T_1 \ldots T_n$ is proportional to the mean value of the input voltage. This sum can be determined by the µP and can be further processed for filter, display, or other recalculations.

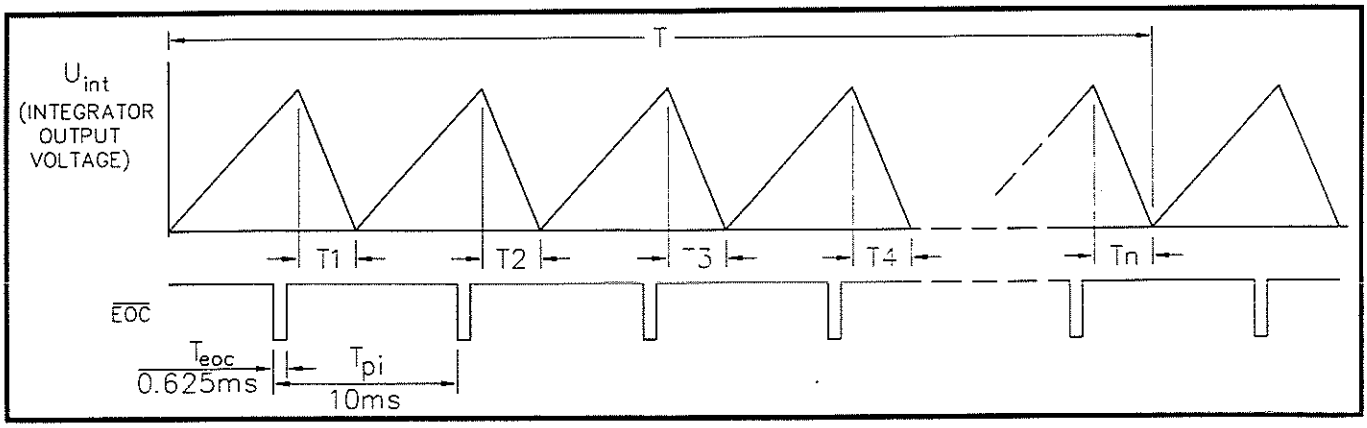



FIG. 2: INTEGRATOR OUTPUT VOLTAGE VERSUS TIME
(A detailed pulse diagram for one partial integration time tpi see fig. 3)

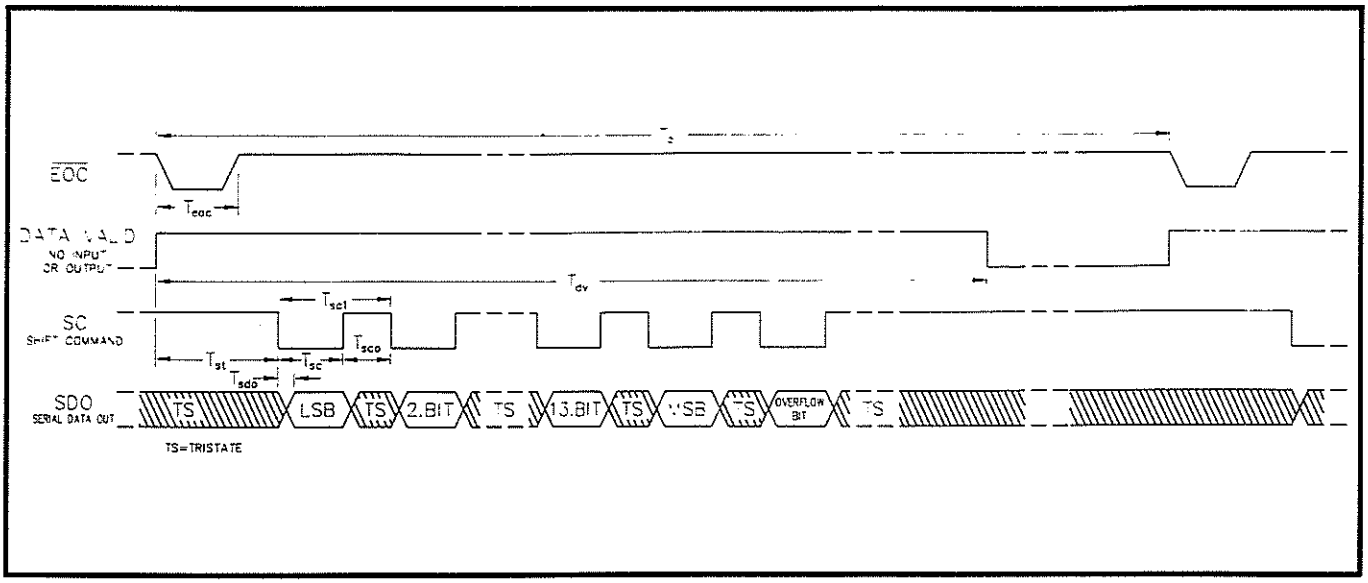



FIG. 3: DETAILED PULSE DIAGRAM FOR ONE PARTIAL INTEGRATION TIME

## DATA EXCHANGE BETWEEN THE ADC 5601 AND THE MICROPROCESSOR

The analog to digital converter ADC 5601 delivers its digital conversion result in serial form via the output SDO. Prior to this, the ADC 5601 reports the end of a 10 ms duration partial integration via the "end of conversion" output (see fig. 3). The microprocessor then has 8.5 ms time to read out the 15 bit conversion result of the last partial integration, using the shift clock pulse sequence which it must apply to the SC-input of the converter. In the resting state the microprocessor places logic level HIGH on the SC line which switches the serial data output (SDO) to high impedance. The LSB of the conversion result appears at SDO on the first negative going flank of SC. The 15th transmitted bit is the overflow bit.

Under normal conditions the microprocessor calculates the conversion result for the total measuring time T as the sum of the individual partial integrations from the times $T_1$ to $T_n$. The total measuring time is $n \cdot 10$ ms. The value of n ($n = 1, 2, 3 \ldots$) is defined by the user in the microprocessor software. The number n is determined by the desired minimum or maximum measuring time or by the desired resolution. The maximum resolution for a single partial integration time of 10 ms is 13 thousand (see corresponding sections for offset and gain adjustment).

## REFERENCE

The reference source lies outside the converter module, so that the user can make his own choice of low-price or high-stability reference for the ADC 5601, to suit the particular application. Reference voltages in the range +6 V to +8 V are acceptable. The gain and (approximately) the offset change are inversely proportional to the reference voltage. Reference ground should lie at the same potential as ANALOG GROUND, with a shortest possible connection.

## GAIN AND OFFSET ADJUSTMENTS

Gain and offset adjustments are normally made by the microprocessor which controls the analog to digital converter.

An analog adjustment may be of interest in particular for the offset because it can be used to shift the analog span of the signal input $Vx_1$ (Pin 5).

For this, a series resistance $R_v$ and a negative offset voltage $U_v$ are connected to $Vx_2$ according to fig. 5.

The counter result is calculated as

$$U_{ADC}\,(D/s) = Vx_1\,(V) \cdot C_1 + U_v\,(V) \cdot \frac{10\ k\Omega}{R_v\,(k\Omega) + 10\ k\Omega} \cdot C_2$$

The gain of the input signal $Vx_1$ is given by the first expression $Vx_1 \cdot C_1$. The adjustment of unipolar or bipolar operation is done by the second expression

$$U_v\,(V) \cdot \frac{10\ k\Omega}{R_v(k\Omega) + 10\ k\Omega} \cdot C_2$$

With $U_v = -2.5$ V und $R_v = 0$ the converter operates in bipolar mode. Temperaturecoefficient and long-term drift of the offset voltage $U_v$ (V) and the series resistance $R_v$ affect the counter result. Increasing offset values demand high stability and low temperature-coefficients of the offset voltage $U_v$ and the series resistance $R_v$. The resting digital offset is removed by the microprocessor.

The offset should be adjusted such that the digital conversion result for each partial integration is not less than 100 digits for the smallest magnitude of the input voltage $Vx_1$ at pin 5, i. e. with the $Vx_2$-input grounded, the smallest magnitude input voltage should not be less than 100 digits corresponding to about 50 mV.

If a gain modification is necessary too, this can be achieved with a metal film or wirewound resistor, less satisfactorily with a potentiometer, connected in series with the input $Vx_1$ (pin 5). A series resistance of $m \cdot 10$ kOhm reduces the gain by a factor of $1/(m + 1)$. When m is greater than 0.03, an unfavourable choice of series resistor will lead to deterioration of the temperature stability of the converter gain.

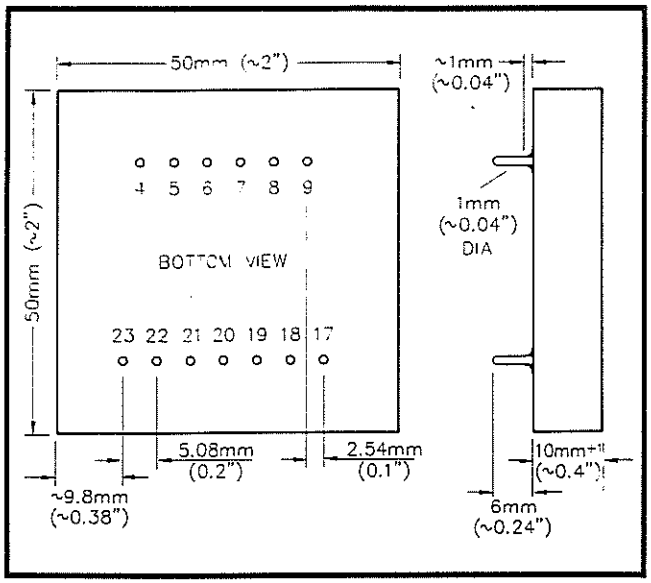



FIG. 4: OUTLINE DIMENSIONS

## LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC 5601 but should be connected together as close to the unit as possible. If these grounds must be run separately, use wide conductor pattern and a 0.1 µF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

## POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum type capacitors as shown in Figure 5 to obtain noise free operation. These capacitors should be located close to the ADC 5601.
Normally regulated power supplies with 0.1 % or less ripple are recommended for use with this ADC 5601. See Layout Precautions and Figures 5.

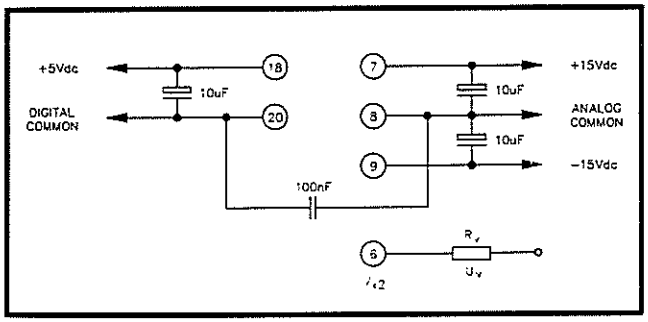



FIG. 5: RECOMMENDED POWER SUPPLY DECOUPLING

LIFE SUPPORT POLICY

PREMAs products are not authorized for use as critical components in life support devices or systems without the express written approval of the management of PREMA GmbH. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

The information in this publication has been carefully checked and is believed to be reliable; however no responsibility is assumed for possible inaccuracies or omissions. Manufactured under one or more of the following patents: U.S. Pats: 3765012; 4361831; Germ. Pats: 2114141; 2820601.

## ABSOLUTE MAXIMUM RATINGS [1)]

ADC 5601

Reference Input Voltage Range, $V_{ref}$ ..... –0,3 to Vp
Supply Voltage, Vp ..... –0,3 V to 17 V
Supply Voltage, Vn ..... +0,3 V to –17 V
Supply Voltage, Vcc ..... –0,3 V to 6 V
Digital Input ..... –0,3 V to Vcc + 0,3 V
All Analog Inputs, Vn ..... –0,3 V to Vcc + 0,3 V

Digital Outputs Current Range,
Source and Sink ..... 16 mA
Continuous Total Dissipation
at or Below +55 °C ..... 600 mW
Operating Free Air Temperature Range ..... 10 °C to 50 °C
Storage Temperature Range ..... –20 °C to 80 °C
Lead Temperature 1/16 Inch (1,6 mm)
from Case for 10 Sec. ..... +260 °C

## ELECTRICAL CHARACTERISTICS (Part 1) [1)]

| PARAMETER | SYMBOL | TEST CONDITIONS unless otherwise noted: Vcc = 5 V, Vp = 15 V, Vn = –15 V, $V_{ref}$ = 6.9 V, fq = 3,6864 MHz, AN GND = 0 V, Ta = 23 °C | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| RESOLUTION | | Integration time 20 s | | | 26,000,000<br>25 | Bit |
| | | 2 s | | | 2,600,000<br>21 | Bit |
| | | 200 ms | | | 260,000<br>18 | Bit |
| | | 20 ms | | | 26,000<br>15 | Bit |
| ACCURACY [4) 5)] | | | | | | |
| Error All Sources (24 h, ±1 °C) | | contains all following particularized errors | | 2 + 1 | | (read+fs.) ppm |
| Error All Sources (1 year, ±5 °C) | | | | 10 + 1 | | (read+fs.) ppm |
| Linearity Error | | | | | +/– 0.0001 | % FS |
| Inherent Quantization Error | | | | +/– 1/2 | +/– 3/4 | LSB |
| Differential Linearity Error | | | | +/– 1/2 | | LSB |
| Gain Error | | | | | +/– 0.05 | % |
| Offset | | | | 0.5 | | % FS |
| DRIFT | | | | | | |
| Gain | | | | 0.5 | 0.8 | ppm/°C |
| Offset | | | | 0.3 | 0.6 | ±µV/°C |
| Temperature Range | Ta | | 10 | | 50 | °C |
| Warm-Up Time | | | 5 | | | min |
| GAIN | | | | | | |
| Input $Vx_1$ | $C_1$ | $Vx_2$ at ANALOG GND | –2,60 | –2,67 | –2,74 | $10^5$ D/Vs |
| Input $Vx_2$ | $C_2$ | $Vx_1$ at ANALOG GND | –2,60 | –2,67 | –2,74 | $10^5$ D/Vs |
| ANALOG INPUTS | | | | | | |
| Input Voltage Range (Bipolar) | $Vx_1$ | $Vx_2$ fixed at –2.5 V | +2.5 | | –2.5 | V |
| Input Voltage Range (Unipolar) | $Vx_1$ | $Vx_2$ fixed at –50 mV | 0 | | –5 | V |
| $V_{ref}$-Input Voltage Range | $V_{ref}$ | | 6 | | 8 | V |
| Input ANALOG GND | | | –30 | 0 | 30 | mV |
| Impedance ($Vx_1$-Input) | $Rx_1$ | | 9.99 | 10 | 10.01 | kOhm |
| Impedance REF IN | $R_{ref}$ | | | 100 | | MOhm |
| Impedance (Voff-Input) | $Rx_2$ | | 9.99 | 10 | 10.01 | kOhm |

## ELECTRICAL CHARACTERISTICS (Part 2) [1)] — ADC 5601

| PARAMETER | SYMBOL | TEST CONDITIONS unless, otherwise noted: Vcc = 5 V, Vp = 15 V, Vn = −15 V, $V_{ref}$ = 6.9 V, fq = 3,6864 MHz, AN GND = 0 V, Ta = 23 °C | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| DIGITAL- AND TIMING DATA | | | | | | |
| Serial Data Code | | 15 bits binary each partial integration, starting with LSB | | | | |
| Serial Data Out Drive | SDO | | 6 | | | TTL Loads |
| End of Conversion Drive | EOC | | 6 | | | TTL Loads |
| Shift Command Input | SC | | | | | |
| Min. Hi Voltage | | | | | 2.0 | V |
| Hi Current | | | | 3 | 40 | µA |
| Max. Lo Voltage | | | 0.8 | | | V |
| Lo Current, negative | | | | | −1 | µA |
| Shift Command Time | Tsc | | 300 | | | ns |
| Shift Command Time | Tsco | | 12 | | | µs |
| Shift Command Time | Tsc 1 | | 25 | | | µs |
| Shift Command Start Time | Tst | | 0 | | | ns |
| SDO Delay Time | Tsdo | | | 100 | 150 | ns |
| Data Valid Time | Tdv | | 8.5 | | | ms |
| EOC Time | Teoc | | | 625 | | µs [3)] |
| Partial Integration Time | Tpi | | | 10 | | ms [3)] |
| Total Integration Time [2)] | T | | | n · 10 | | ms [3)] |
| Frequency of external Crystal | fq | | 3.0 | 3.6864 | 3.7 | MHz |
| SUPPLY | | | | | | |
| Power Consumption | | | | 450 | 600 | mW |
| Supply Current (Vp) | Ip | | | 10.5 | 14 | mA |
| Supply Current (Vn) | In | | | 7.5 | 10 | mA |
| Supply Current (Vcc) | Icc | | | 36 | 50 | mA |
| Supply Voltage | Vp | | 14.5 | 15 | 15.5 | V |
| Supply Voltage | Vn | | −14.5 | −15 | −15,5 | V |
| Supply Voltage | Vcc | | 4.75 | 5 | 5.25 | V |
| POWER SUPPLY SENSIVITY | | | | | | |
| +/− 15 V | Vp, Vn | | | 0.0001 | | %FS/%Vp, n |
| 5 V | V | | | 0.0001 | | %FS/%Vcc |

1) All voltage values are with respect to ground terminal DIG GND unless otherwise noted.
2) n = number of partial integrations selected by µP-Software.
3) This time is derived from (e.g. inversely proportional to) the crystal frequency fq.
4) Analog voltages are with respect to ground terminal AN GND.
5) Add errors through drift of the external reference voltage.

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