52B33/52B33H

64K Electrically Erasable PROM

October 1987

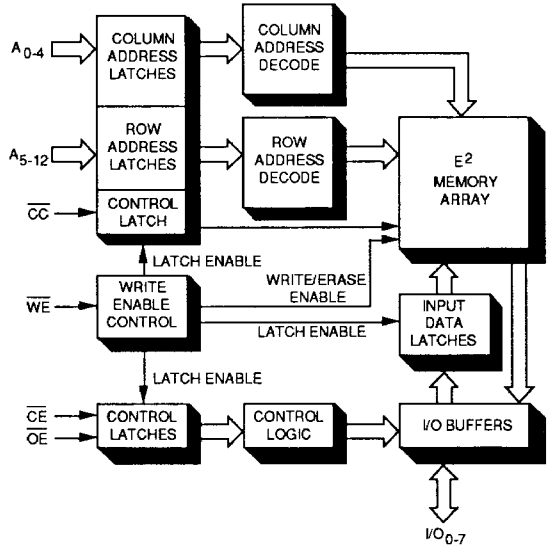
Features

- **High Write Endurance Over Temperature Range**
  - **52B33/52B33H; 10,000 cycles/byte minimum**
- **Input Latches**
- **Fast TTL Byte Write Time**
  - **1 ms for 52B33H**
  - **9 ms for 52B33**
- **5 V± 10% Vcc**
- **Power Up/Down Protection**
- **200 ns Read Access Time**
- **DiTrace®**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Military And Extended Temperature Range Available**

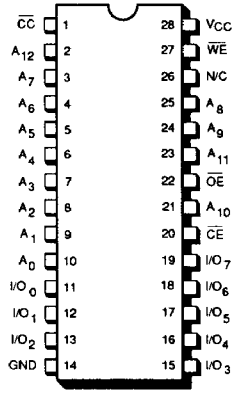
Description

SEEQ's 52B33 is a 8192 x 8 bit, 5 volt electrically erasable programmable read only memory (EEPROM) which is specified over a 0°C to 70°C temperature range. Data retention is specified to be greater than 10 years. The device has input latches on all addresses, data and control (chip and output) lines. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times. For applications requiring a faster byte write or erase time, a 52B33H is available at 1 ms, giving a 10 times speed increase.

Block Diagram



Pin Configuration



Pin Names

A_0-A_4	ADDRESSES – COLUMN (LOWER ORDER BITS)
A_5 -A_{12}	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

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The pin configuration is to the JEDEC approved byte wide memory pinout. EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by EEPROMs. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into these systems is simplified because of the fast access time and input latches. The specified 200 ns access time eliminates or reduces the number of microprocessor wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B33 has six modes of operation (see Table 1) and requires only TTL inputs to operate these modes. The "H" members of the family operate in the same manner as the other devices except that a faster write enable pulse width of 1 ms is specified during byte erase or write.

Read

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The write enable ($\overline{WE}$) pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Write

To write in to a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs and I/O lines. All inputs can be released after the write enable hold time (t_H) and the next input conditions can be established while the byte is being erased. During this operation, the write enable must be held at a TTL low for 9 ms (t_{WP}). A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the 52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

DiTrace

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

NOTE:
1. Characterized. Not tested.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... −65°C to +100°C
Under Bias ..... −10°C to +80°C
D.C. Voltage applied to all Inputs or Outputs with respect to ground ..... +6.0 V to −0.5 V
Undershoot/Overshoot pulse of less then 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... (undershoot) −1.0 V (overshoot) + 7.0 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B33, 52B33H
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

Power Up/Down Considerations

SEEQ's "52B" E² family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Erase/Write

(Over the operating V_{CC} and temperature range)

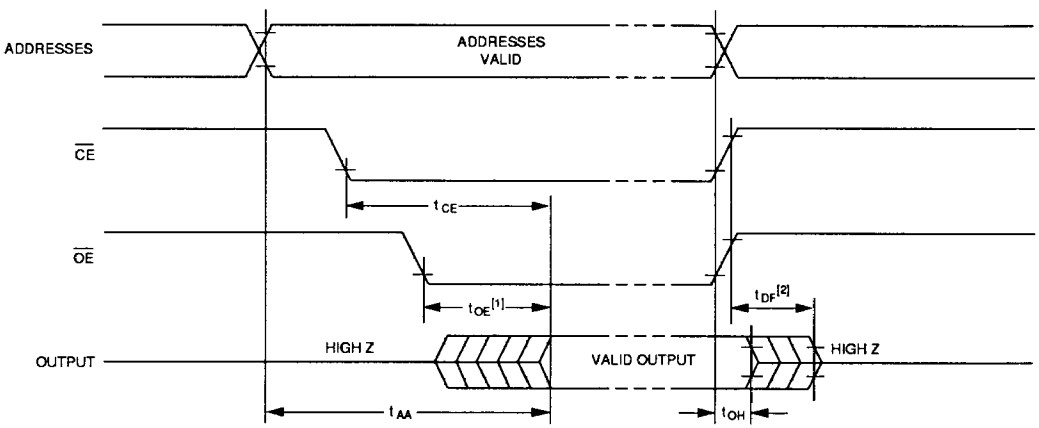
Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage			10	µA	$\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		18	40	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		60	110	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

NOTE:
1. Nominal values are for T_A = 25°C and V_{CC} = 5.0 V.

A.C. Operating Characteristics During Read (Over the operating V_{cc} and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H Min.	Max.	Units	Test Conditions
t_{AA}	Address Access Time	-200		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{CE}	Chip Enable to Data Valid	-200		200	ns	$\overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{OE}[1]	Output Enable to Data Valid	-200		80	ns	$\overline{CE} = V_{IL}$
		-250		90	ns	
		-350		100	ns	
t_{DF}[2]	Output Enable to High Impedance	-200	0	60	ns	$\overline{CE} = V_{IL}$
		-250	0	70	ns	
		-350	0	80	ns	
t_{OH}	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[3]	Input and Output Capacitance	All		10	pF	V_{IN} =0 V for C_{IN}, V_{OUT} = 0 V for C_{OUT}, T_A = 25°C

Read Cycle Timing



NOTES:

1. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
4. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
5. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

A.C. Test Conditions

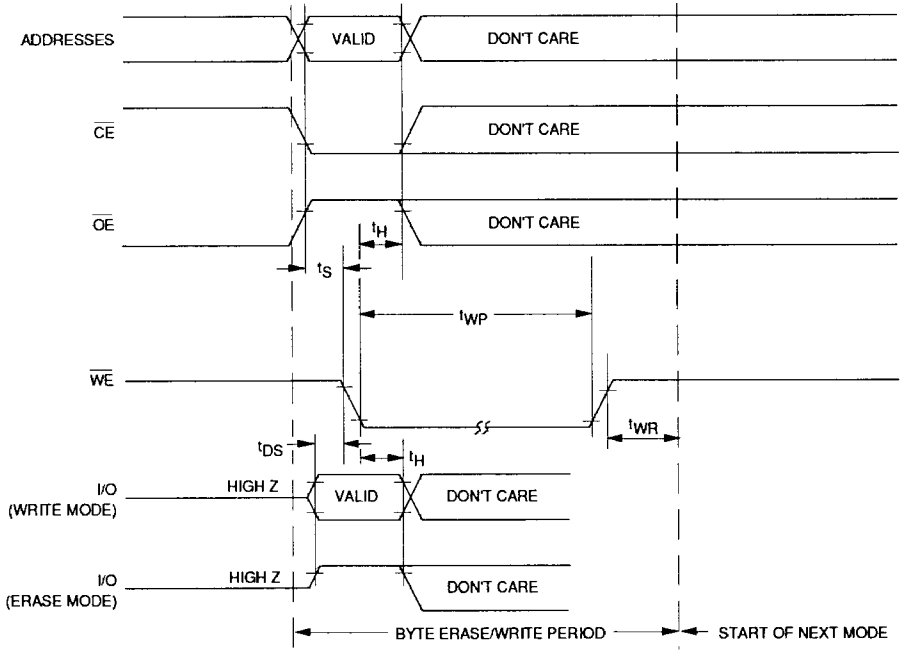
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

A.C. Operating Characteristics During Write/Erase

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	15		ns
t_H [4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Byte Modes — 52B33	9		ms
	Byte Modes — 52B33H	1		
t_{WR} [5]	$\overline{WE}$ to Mode Change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle	1		µs

Byte Erase or Byte Write Cycle Timing



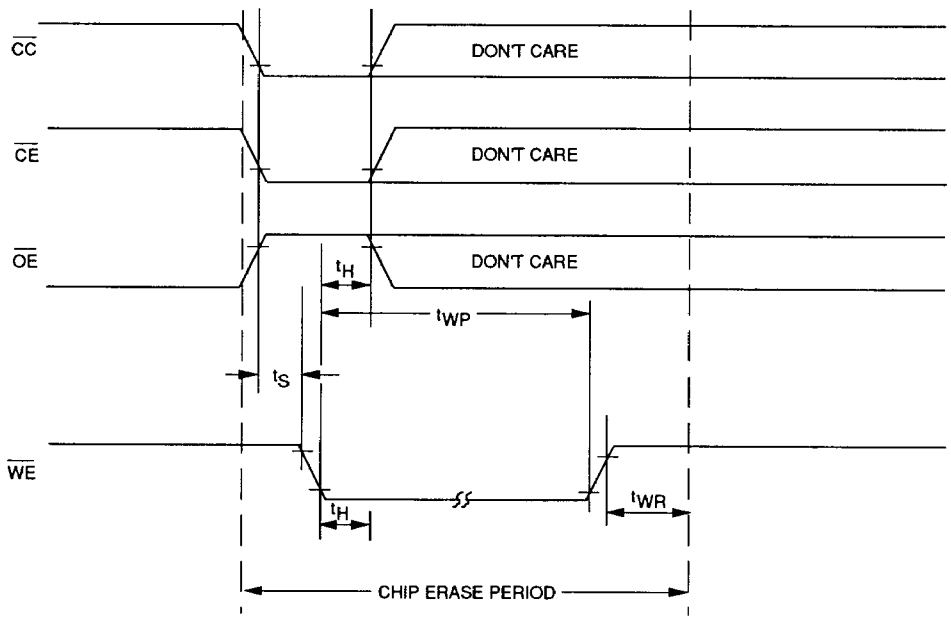
(Notes 4 and 5 are on previous page)

A.C. Operating Characteristics During Chip Erase.

(Over the operating V_{CC} and temperature range)

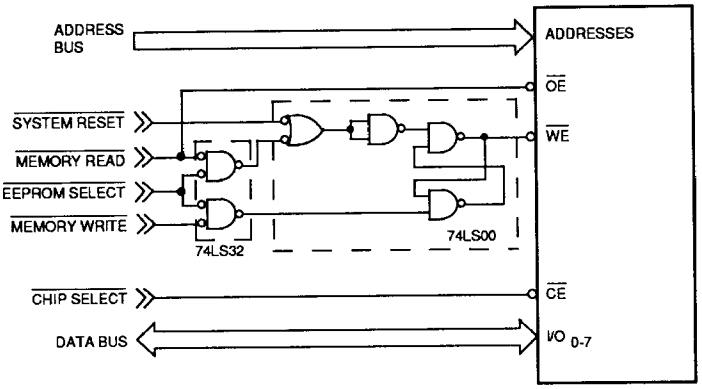
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CC}$, $\overline{CE}$, $\overline{OE}$ Setup to $\overline{WE}$	50		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$ change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Chip Erase — 52B33 Chip Erase — 52B33H	10		ms
t_{WR}[5]	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle		1	µs

TTL Chip Erase Timing



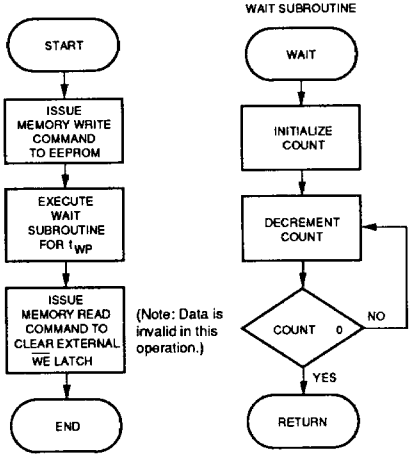
NOTE: Address, Data are don't care during Chip Erase.

Microprocessor Interface Circuit Example for Byte Write/Erase



NOTE:
ALL SIGNALS MUST SATISFY THE RELATIONSHIPS INDICATED BY THE TIMING DIAGRAMS SHOWN ON PAGES 4 AND 5. $\overline{\text{EEPROM SELECT}}$ IS DERIVED FROM THE $\overline{\text{CHIP SELECT}}$ SIGNALS OF ALL DEVICES FOR WHICH THIS CIRCUIT GATES $\overline{\text{WE}}$. THIS MAY ENTAIL A SIMPLE OR FUNCTION. IN CASE OF A SINGLE EEPROM, THE TWO SIGNALS WOULD BE COMMON.

Typical EEPROM Write/Erase Routine



Ordering Information