5494/7494 4-Bit shift Register (Parallel-In, Parallel-Out)

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.																SN5494	J ①			W①					
																SN7494	J ①	N ①							
FAIRCHILD																FM5494/FM9394	D ①								
																FC7494/FC9394	D ①	P ①							
MOTOROLA																MC5494	L ①								
																MC7494		P ①							
N. S. C.																									
PHILIPS																									
																N7494		①							
SIGNETICS																S5494	F ①	B ①		W①					
																N7494	F ①	B ①							
SIEMENS																									
																FLJ231		①							
FUJITSU																									
HITACHI																									
																HD2533	①	P ①							
MITSUBISHI																									
NEC																									
TOSHIBA																									

Electrical Characteristics SN5494, SN7494

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54'	−55°C to 125°C
Input voltage	5.5V		SN74'	0°C to 70°C
		Storage temperature range		−65°C to 150°C

recommended operating conditions

		SN5494			SN7494			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, $t_{w(clock)}$		35			35			ns
Width of clear pulse, $t_{w(clear)}$		30			30			ns
Width of preset pulse, $t_{w(preset)}$		30			30			ns
Setup time, t_{setup}	High-level data	35			35			ns
	Low-level data	25			25			
Hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

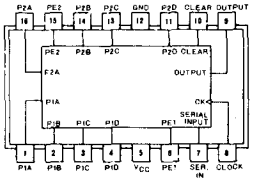
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS †		MIN	TYP ‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA		2.4	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 2.4V				160	μA
		Other inputs					40	
I_{IL}	Low-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 0.4V				6.4	mA
		Other inputs					−1.6	
I_{OS}	Short-circuit output current ◆		V_{CC} = MAX	SN54'	−20		−57	mA
				SN74'	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 1	SN54'		35	50	mA
				SN74'		35	58	
f_{max}	Maximum clock frequency				10			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock		V_{CC} = 5V, C_L = 15pF, T_A = 25°C, R_L = 400Ω			25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock					25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset						35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear						40	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5V, T_A = 25°C.
◆ Not more than one output should be shorted at a time.

Pin Assignment (Top View)

①



positive logic: see function tables

Function Table

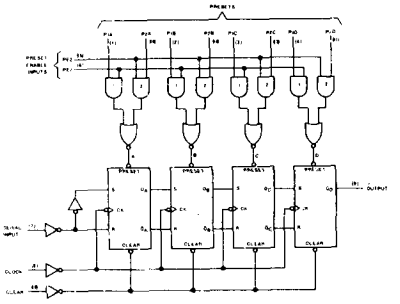
'94 PRESET (see Note 2)
BIT A, TYPICAL OF ALL

PRESET INPUTS				INTERNAL
PE1	P1A	PE2	P2A	PRESET A
L	X	L	X	H (inactive)
L	X	X	L	H (inactive)
X	L	L	X	H (inactive)
X	L	X	L	H (inactive)
H	H	X	X	L (active)
X	X	H	H	L (active)

'94 REGISTER (see Note 2)

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

Functional Block Diagram



◆ ··· dynamic input activated by transition from a high level to a low level

'94 4-BIT SHIFT REGISTER

NOTES: 1. I_{CC} is measured with the outputs open, clear grounded following momentary application of 4.5 V, both preset-enable inputs grounded, and all other inputs at 4.5 V.

2. H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.