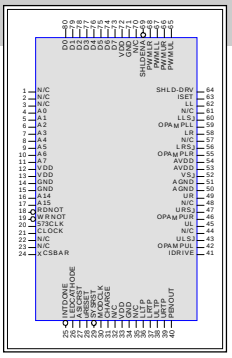

Excalibur Chip Set Controller

Developer's Guide

Features

- Support for Capacitive and/or 5-wire Resistive Touchscreens
- Lower System Cost
- Small Form Factor
- MicroTouch Proprietary *Excalibur* ASIC (80 pin PQFP)
- Simple System Power Requirements (5V @ 35 mA typical)
- Serial UART or PS/2 Interface

Description

The Excalibur chip set consists of an optimized controller circuit that can be used with MicroTouch *capacitive* or 5-wire *resistive* touchscreens. The chip set is designed for maximum flexibility and ease of implementation.

At the core of the chip set is the MicroTouch Excalibur proprietary custom ASIC and the microcontroller firmware. The ASIC contains the latest technology used in MicroTouch touchscreen controllers. The ASIC, together with an 80C32 microcontroller, a 64K OTP EPROM, a 2K-bit serial EEPROM, and a few discrete components, form a powerful and versatile touchscreen controller.

Multi-mode is an implementation method that lets you switch the controller's behavior from capacitive to resistive simply by changing a few shorting-plugs. You can also select serial or PS/2 communication protocol via shorting-plugs.

With multi-mode, you can switch touchscreen technologies and communication modes at will without having to design multiple circuits and manage the different SKUs.

This document includes full technical detail for the Excalibur ASIC. It also provides implementation schematics and a complete bill of materials for capacitive, resistive, and multi-mode touchscreen controllers.

MicroTouch

Excalibur Chip Set Controller Developer's Guide
Part Number: 19-221, Version 2.0

Excalibur ASIC Chip Specifications

Table 1, Table 2, and Table 3 list the specifications for the Excalibur ASIC.

Table 1. Excalibur Absolute Maximum Ratings

Parameter	Rating
Storage temperature range	-65 to 150 °C
Operating free-air temperature	0 to 65 °C
Supply voltage, VDD, AVDD*	6.5V
Input voltage range*	-0.5 to +6.5V
Output current, I_O	5 mA
Input current, I_I	5 mA
Continuous total power dissipation	$T_A \leq 25°C$ Power Rating: 1 W De-Rating Factor Above T_A=25°C: 12 mW/°C T_A=65°C Power Rating: 520 mW
Case temperature for 40 seconds	225 °C

** All voltages are with respect to GND and AGND.*

Table 2. Excalibur Recommended Operating Conditions (TA = 0 to 65°C)

Parameter	Rating
Supply voltage, VDD, AVDD	4.5 to 5.5V
Input rise or fall times (logic inputs)	500 ns maximum
Clock frequency	11.0592 MHz (MicroTouch recommends using this frequency such that nominal baud-rate frequencies are generated by the microcontroller.)

Table 3. Excalibur Electrical Characteristics (TA=25°C)

Parameter	Rating
Minimum high level input voltage, V_{IH} (logic inputs) VDD & AVDD = 4.5V to 5.5V	3.5V
Maximum low level input voltage, V_{IL} (logic inputs) VDD & AVDD = 4.5V to 5.5V	0.8V
Maximum input Leakage high, I_{INH} VDD & AVDD = 5.5V	±1 μA
Maximum input Leakage low, I_{INL} VDD & AVDD = 5.5V	±1 μA
Maximum input Leakage low, I_{INL} (logic inputs w/ pull-ups) VDD & AVDD = 5.5V	5 to 35 μA
Typical total supply current, I_{CC} VDD & AVDD = 5.5V	5 mA
Maximum total supply current, I_{CC} VDD & AVDD = 5.5V	8 mA

System Power Requirements for Complete Chip Set

Table 4. System Power Requirements for Complete Chip Set

Parameter	Rating
Vcc	5V ± 10%, ripple and noise < 50 mVpp (peak-to-peak)
Icc	35 mA typical, 60 mA maximum

Excalibur Pin Definitions

Figure 1 shows the layout of the pins on the Excalibur ASIC. Table 5 lists the name, type, and description of each pin.

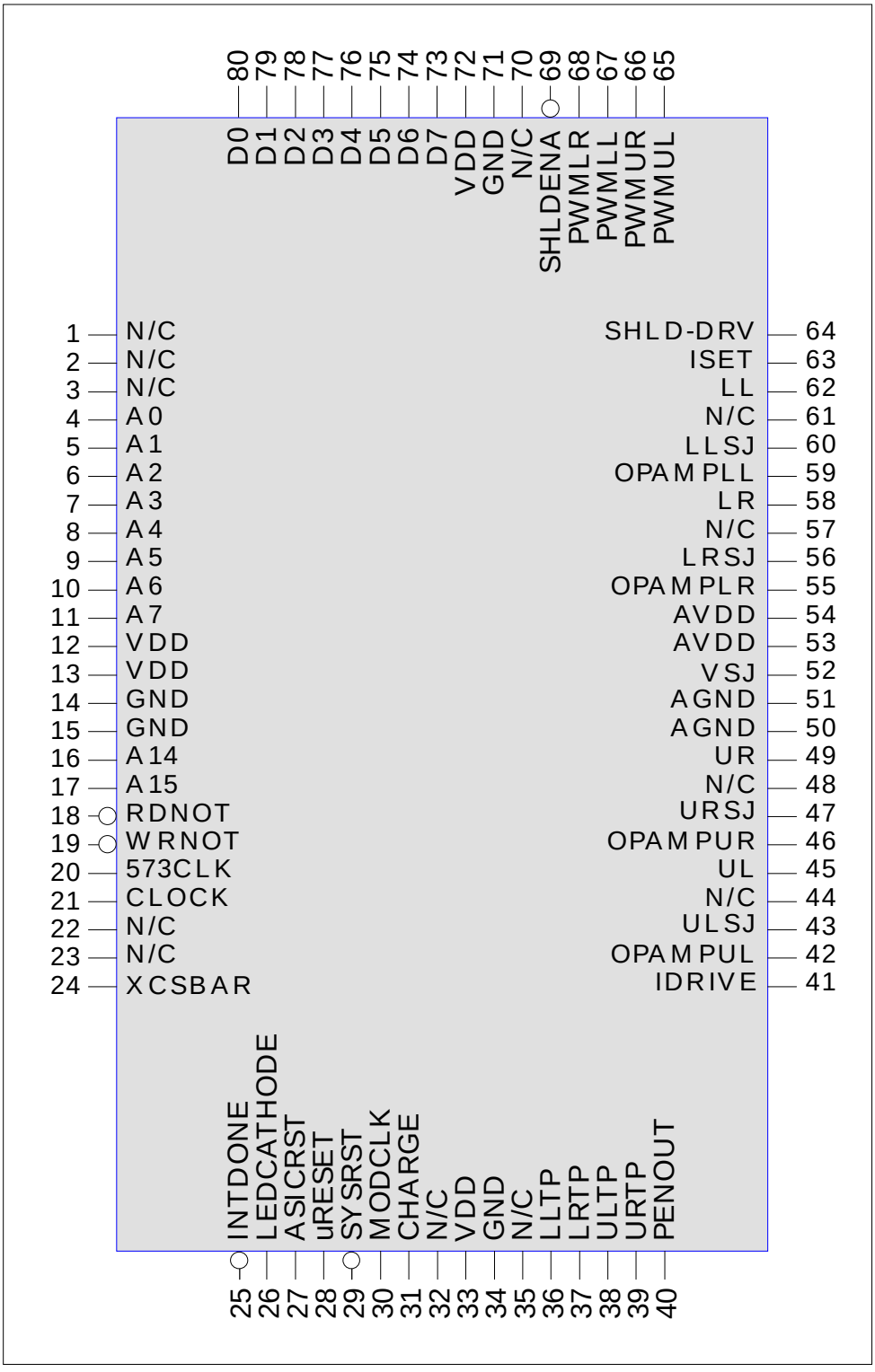

Figure 1. Excalibur Pinout

Table 5. Excalibur Pin Definitions

Pin	Name	Type	Description
1	N/C	N/C	No connection
2	N/C	N/C	No connection
3	N/C	N/C	No connection
4	A0	Output	EPROM lower order address bit A0
5	A1	Output	EPROM lower order address bit A1
6	A2	Output	EPROM lower order address bit A2
7	A3	Output	EPROM lower order address bit A3
8	A4	Output	EPROM lower order address bit A4
9	A5	Output	EPROM lower order address bit A5
10	A6	Output	EPROM lower order address bit A6
11	A7	Output	EPROM lower order address bit A7
12	VDD	Power	Digital power
13	VDD	Power	Digital power
14	GND	Gnd	Digital ground
15	GND	Gnd	Digital ground
16	A14	Input	Address bit A14
17	A15	Input	Address bit A15
18	RDNOT	Input	Registers Read control (active low)
19	WRNOT	Input	Registers Write control (active low)
20	573CLK	Input	Lower order address-byte latch control
21	CLOCK	Input	Master clock (11.0592 MHz)
22	N/C	N/C	No connection
23	N/C	N/C	No connection
24	XCSBAR	Output	No connection
25	INTDONE	Output	A/D integration status (active low)
26	LEDCATHODE	Output	LED drive output
27	ASICRST	Input	Resets ASIC registers and FFs (active high)
28	uRESET	Output	Output of the ASIC's internal Power on Reset (POR) circuit OR'd with SYSRST (active high)
29	SYSRST	Input (Schmitt)	Chip set Master Reset (active low)
30	MODCLK	Output	No connection
31	CHARGE	Output	Sensor operating frequency
32	N/C	N/C	No connection
33	VDD	Power	Digital power
34	GND	Gnd	Digital ground
35	N/C	N/C	No connection
36	LLTP	Output	No connection
37	LRTP	Output	No connection
38	ULTP	Output	No connection
39	URTP	Output	No connection
40	PENOUT	Output	No connection

Pin	Name	Type	Description
41	IDRIVE	Output	Resistive screen drive output
42	OPAMPUL	Output	Upper-left amplifier output
43	ULSJ	Input	Upper-left amplifier input
44	N/C	N/C	No connection
45	UL	Output	Upper-left sensor drive
46	OPAMPUR	Output	Upper-right amplifier output
47	URSJ	Input	Upper-right amplifier input
48	N/C	N/C	No connection
49	UR	Output	Upper-right sensor drive
50	AGND	Agnd	Analog ground
51	AGND	Agnd	Analog ground
52	VSJ	Output	Voltage reference output
53	AVDD	Power	Analog power
54	AVDD	Power	Analog power
55	OPAMPLR	Output	Lower-right amplifier output
56	LRSJ	Input	Lower-right amplifier input
57	N/C	N/C	No connection
58	LR	Output	Lower-right sensor drive
59	OPAMPLL	Output	Lower-left amplifier output
60	LLSJ	Input	Lower-left amplifier input
61	N/C	N/C	No connection
62	LL	Output	Lower-left sensor drive
63	ISET	Input	Bias reference input, sets transfer f(x) gain
64	SHLD-DRV	Output	Shield amplifier output
65	PWMUL	Output	No connection
66	PWMUR	Output	No connection
67	PWMLL	Output	No connection
68	PWMLR	Output	No connection
69	SHLDENA	Input	No connection
70	N/C	N/C	No connection
71	GND	Gnd	Digital ground
72	VDD	Power	Digital power
73	D7	Bidir	Data bus signal D7
74	D6	Bidir	Data bus signal D6
75	D5	Bidir	Data bus signal D5
76	D4	Bidir	Data bus signal D4
77	D3	Bidir	Data bus signal D3
78	D2	Bidir	Data bus signal D2
79	D1	Bidir	Data bus signal D1
80	D0	Bidir	Data bus signal D0

Mechanical Specifications for Excalibur 80 Pin PQFP

The package style for the Excalibur ASIC is an 80 pin PQFP (plastic quad flat pack).

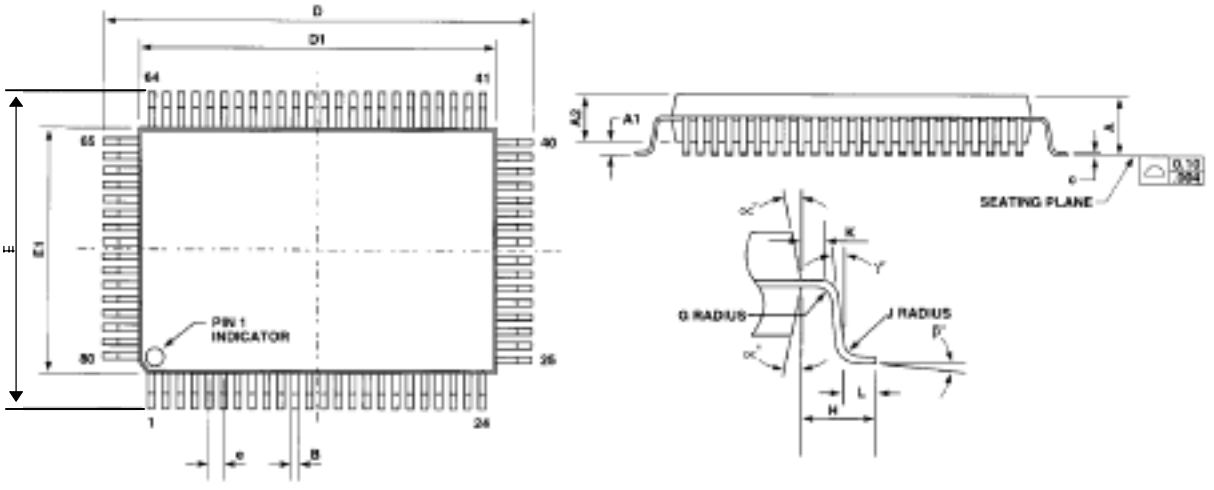

Table 6. Dimensions of the Excalibur 80 Pin PQFP

Symbol	Tolerance (mm)	Dimension (mm)
A		3.40 maximum
A1		0.25 minimum
A2	±0.10	2.70
D	± 0.25	23.20
D1	± 0.10	20.00
E	± 0.25	17.20
E1	± 0.10	14.00
L	+.15/-0.10	0.88 (*L is measured at gage plane at 0.25 above the seating plane.)*
B	± 0.05	0.35
c		0.17 maximum
G		0.20 radius minimum
e		0.80 nominal
J		0.30 radius minimum
β°		0° – 7°

Resistive Versus Capacitive Sensor Operation

The Excalibur ASIC is designed to operate analog capacitive or 5-wire resistive touchscreens with a minimum of difference in the overall chip set design. The main difference is the firmware used to program U4, the program ROM. From a circuit implementation point of view, the only remaining difference is how the fifth wire of the sensor is driven.

MicroTouch determines touch position by measuring currents in the four corners of the touchscreen, regardless of sensor technology.

- For capacitive operation, a fifth connection is made to the back of the sensor (backshield), typically connected to ground to provide noise immunity from the display device.
- For resistive operation, a fifth connection is made to the conductive top sheet connecting it to a current source.

For sensors with cable NovRAM, the electrical difference of the capacitive/resistive fifth wire is incorporated within the sensor harness. Therefore, you only need to select the firmware to implement either resistive or capacitive mode of operation.

For sensors without cable NovRAM, you can easily implement the fifth wire electrical difference into the chip set circuit if multi-mode operation is desired.

Firmware Programming

MicroTouch provides the firmware as binary hexadecimal files contained on the Excalibur ASIC Controller Firmware diskette (Part Number: 9310000). This diskette provides four versions of firmware that vary based on the touchscreen technology (capacitive or resistive) and the communication mode. Refer to “Serial Versus PS/2 Communication Modes” later in this document for more details.

- You must program the appropriate file(s) into individual 64K x 8 pages of a ROM device. Table 7 lists the available firmware files. For multi-mode applications, shorting-plugs on the upper address lines of the ROM can select the appropriate firmware.
- The file is in Intel hexadecimal format.
- All unused ROM bytes must be filled with FFH.

Serial Versus PS/2 Communication Modes

The Excalibur chip set design supports either serial communication or PS/2 communication. You can enable the communication mode (as well as capacitive versus resistive operation) by selecting the appropriate firmware. Table 7 shows the four firmware files included on the Excalibur ASIC Controller Firmware diskette (Part Number: 9310000).

Table 7. Firmware Available for the Excalibur Chip Set

Touchscreen Technology	Communication Mode	Firmware Part Number
Capacitive	Serial communication	9208900
Capacitive	PS/2 communication	9208710
Resistive	Serial communication	9208940
Resistive	PS/2 communication	9209100

You must be sure to use the appropriate set of I/O communication pins for the communication mode selected.

- For serial communication, use DATA-IN and DATA-OUT.
- For PS/2 communication, use PS2-CLK and PS2-DATA.

For multi-mode applications, shorting-plugs could also be used to select the I/O communication pins.

Touchscreen Interface

- *For sensors with cable NovRAM*, the J1 connector, the ferrite beads (L1 – L4), the ESD protection diodes (D1 – D5, D7, D8), and the resistors (R4 – R6) provide the touchscreen interface to the Excalibur ASIC. Refer to Figure 3.
- *For sensors without cable NovRAM*, the J1 connector, the ferrite beads (L1 – L4), and the ESD protection diodes (D1 – D5) provide the touchscreen interface to the Excalibur ASIC. SP3, R2, and R3 provide CRT turn-on HV discharge for resistive mode and shield termination for capacitive mode. Refer to Figure 5.

The four ferrites attenuate any RF pickup from the touchscreen. The ESD diodes clamp excessive voltage generated by an ESD disturbance and direct the currents to low impedance nodes. Be sure the EVDD and EGND connection to these diodes is short and direct using good PCB layout techniques. (Refer to “PCB Layout Considerations” later in this document for more information).

Microcontroller and Program Memory

U2 and U4 are the 80C32 microcontroller and program ROM respectively.

The 80C32 microcontroller is a member of the standard Intel 8051 style 8-bit CMOS microcontroller family. The 80C32 contains 256 bytes of RAM and includes a full serial UART interface. (The address/data bus of the 80C32 is multiplexed and applications using this microcontroller typically require an address demultiplexer circuit that latches the lower 8 bits of the address bus during a program fetch. The function of the demultiplexer circuit is built into the Excalibur ASIC.)

The 80C32 requires an external ROM or OTP (one time programmable) EPROM. MicroTouch supplies the firmware for the ROM as part of the Excalibur chip set package. It is available as a binary hexadecimal file, which is compatible with most PROM programmers.

The MicroTouch firmware controls all aspects of the hardware operation and provides for stand-alone touchscreen functionality. Touch position is automatically detected, calculated, and output serially at user selected baud rates. The firmware command set is extensive. Refer to the MicroTouch *Touch Controllers Reference Guide* for information on each command.

Non-Volatile Storage

A number of controller parameters, such as baud rate and other settings, are stored in the chip set's non-volatile EEPROM U3 (NovRAM). This allows all operating defaults to be maintained even after power has been removed. This 93C46 device features a 3-wire serial interface to the microcontroller.

A similar NovRAM resides in MicroTouch sensor cables with NovRAM, which contains manufacturing information, calibration data, and identification of sensor type. The ESD protection diodes (D1 – D3) and the resistors (R4 – R6) provide the communications interface with the sensor cable NovRAM. Refer to Figure 3.

Chip Set System Reset

From the host system point of view, the touchscreen controller can be hardware reset using the active low signal denoted in the schematics as SYSTEMRESET.

When SYSTEMRESET is asserted active low, the touch controller is in *hard reset*. A hard reset means that the entire chip set (Excalibur and 80C32 microcontroller) is brought to an idle state with no clock, logic, or processor activity.

When SYSTEMRESET is de-asserted, Excalibur pin 28, uRESET, switches low which enables the 80C32 microcontroller to boot up (the 80C32 requires an active high RESET). During the boot-up sequence, the 80C32 performs several self diagnostics. If the self diagnostics pass, the 80C32 will set its pin 16 low, ASICRESET**,** in order to enable full Excalibur operation.

> **NOTE:** *Do not confuse this process with the action of the software "Reset" command. A software reset does not alter the hardware operation. Instead, a soft reset performs a logical update on the controller's local information about the touchscreen environment. (Refer to the* Touch Controllers Reference Guide *for a description of the Reset command.)*

Excalibur ASIC Function

The Excalibur ASIC contains the touchscreen sensor interface logic, A/D converter, LED drive, and microcontroller interface. Its main function is to digitize the four unknown currents from the touchscreen corner nodes. The microcontroller establishes ASIC operating behavior at boot-up by writing internal registers used to control analog function and digital timing. It also establishes the operating frequencies and interactively nulls analog errors.

Under command from the microcontroller, the ASIC will start to integrate the four currents and proceed to do so for a preset length of time. When finished, the ASIC will set INTDONE low, interrupting the microcontroller. The microcontroller will then read the four digitized corner currents from the ASIC and issue another integration start. This process continues indefinitely.

For capacitive operation, the ASIC actively operates the sensor in order to detect touch capacitance, which is digitized as a proportional current. For resistive, it passively waits for a touch to provide D.C. current to its digitizers.

Design Considerations

Although the chip set only requires one physical +5V supply, it is advantageous to use the three separate connections, VDD, AVDD, and EVDD, as shown on the schematics and Sample PCB Layout. This helps minimize digital noise from being coupled into the A/D converter within Excalibur, as well as any ESD currents.

Likewise, there are three separate ground connections: GND, AGND, and EGND. You should connect these three grounds directly to split ground planes.

The only external components necessary for proper operation of the Excalibur ASIC are as follows:

- Capacitors C7, C8, and C9 are decoupling capacitors for the digital supply voltage VDD.
- C3 and C17 are decouplers for the analog AVDD supply.
- C16 is a decoupling capacitor for the reference voltage VSJ. This capacitor is connected between the VSJ pin and AVDD.
- R1 sets the internal gain of the ASIC.
- Capacitors C12 – C15 are used for the internal A/D converter. These ceramic capacitors require a quality dielectric. MicroTouch recommends X7R.
- The optional LED provides a number of diagnostic functions such as power-on self-test results, touch indication, and any error conditions that occur. The LED is controlled by an internal current source providing 4 to 5 mA for LED drive.

PCB Layout Considerations

The layout of the Excalibur chip set is straightforward. The general layout suggestions listed below should insure maximum performance from the Excalibur chip set implementation. Refer to Figure 2 for a sample PCB layout.

1. Maintain separate power planes, VDD, AVDD, and EVDD, connecting them together at the source of the +5V (ideally at the power supply or connector where the voltage originates.) Maintain separate ground planes, GND, AGND, and EGND, connecting them together at the source of circuit ground (ideally at the power supply or connector where ground originates).
2. Place touchscreen connector J1 and all ESD components in zone E, over the EVDD and EGND planes.
3. Place the four ferrite beads, L1 – L4, such that they bridge zones E and A.
4. Place op-amps, U5 and U6, and associated capacitors, C10 – C15, in zone A. Maintain PCB trace separation of each op-amp's two unique nets from the others. For example, do not route U5A pins 1 and 2 nets near U5B pins 6 and 7 nets. Place C12 – C15 as close as possible to their respective op-amps minimizing PCB trace length. Place U5 and U6 as close as possible to U1, minimizing PCB trace length.
5. Place U1 (Excalibur ASIC) such that it bridges zones A and D as shown in Figure 2. This places the analog portion of Excalibur over the AGND and AVDD planes, and the digital portion over the GND and VDD planes.
6. Place digital circuits, U2, U3, U4, and their support discrete components in zone D.
7. Route touchscreen connections UL, UR, LL, and LR with a minimum spacing of 25 mil between these four nets and any other net on the board, as well as keeping etch lengths to a minimum. Route them from J1 to the ESD components, then to the ASIC. These steps will help insure that ESD pulses are clamped by the protection diodes and not coupled into other circuitry.
8. Locate all decoupling capacitors as close as possible to their respective power pins.

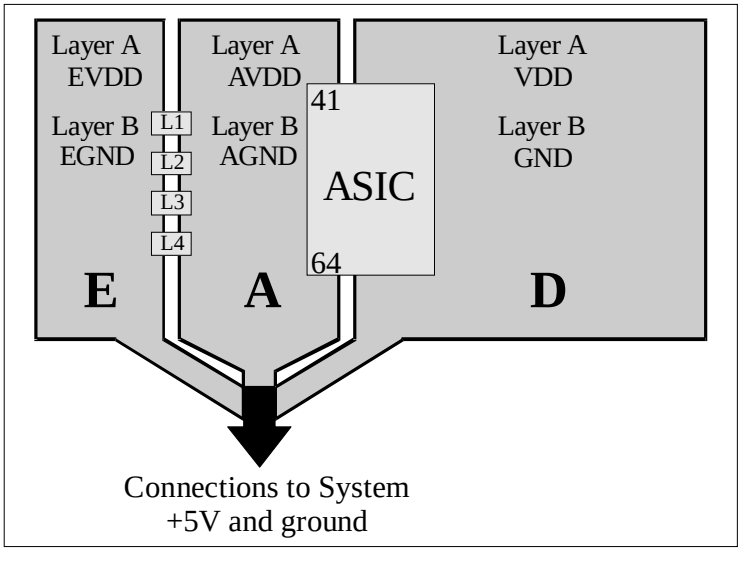

Figure 2. Sample PCB Layout

Testing Considerations

In most cases, the Excalibur chip set circuit is implemented as part of an overall embedded system or PCB assembly. Together with the fact that most applications are using custom software to communicate with the controller, testing the controller operation at either the manufacturing level or operational level is an issue that you should address before the controller PCB design is complete.

You should incorporate the following suggested list of test points into the PCB layout to provide easy access. Table 8 represents a set of test points that should be sufficient to validate correct operation of the Excalibur ASIC and firmware in general. These test points let you monitor internal signals that you can use for indicating normal operation during ATE or for debugging purposes. For many cases of in-circuit testing it will be advantageous for you to provide additional circuitry, where appropriate, for isolation of the different integrated circuits. The best manufacturing strategy is usually determined by the overall testing strategy used by the overall system PCB.

Table 8 *does not* include obvious signals such as supply voltages, crystal clocks, or communication signals as these are left up to you to incorporate if appropriate.

Table 8. Test Points

Pin Name and Number	Description	Normal Resistive Operation	Normal Capacitive Operation
UL Pin 45	Upper-left sensor drive	2.5V, ±0.2V	Square wave, 2.5 to 5V ~40kHz
UR Pin 49	Upper-right sensor drive	2.5V, ±0.2V	Square wave, 2.5 to 5V ~40kHz
LL Pin 62	Lower-left sensor drive	2.5V, ±0.2V	Square wave, 2.5 to 5V ~40kHz
LR Pin 58	Lower-right sensor drive	2.5V, ±0.2V	Square wave, 2.5 to 5V ~40kHz
CHARGE Pin 31	Sensor operating frequency	CMOS square wave ~40kHz	CMOS square wave ~40kHz
VSJ Pin 52	Voltage reference output	2.5V, ±0.2V	2.5V, ±0.2V
INTDONE Pin 25	A/D integration status	CMOS square wave ~200Hz, 80% duty cycle	CMOS square wave ~200Hz, ~80% duty cycle

NOTE: *You can use the test point labeled TP1 "PWRUP DEFAULTS" to restore factory defaults. An active low applied during the reset sequence will restore all factory defaults including communication parameters. Using the test point is useful if you cannot send the "Restore Defaults" (<CTRL>A RD) firmware command.*

Testing Considerations for Software

If the embedded system is not compatible with MicroTouch utility programs, such as Microcal (MS-DOS based), you must provide some generic ability to talk/listen to the chip set using a terminal program, via an external serial port.

For example, you can provide an external RS-232 interface at the DATA-IN and DATA-OUT signals of the chip set. If you do, you must also provide a way to disable your system's transmit pin in order to prevent signal contention on DATA-IN. This RS-232 interface will allow you to send diagnostic commands and observe the resulting reception of diagnostic feedback from the controller using a dumb terminal. Some diagnostic capabilities include touch calibration and verification functions.

Bill of Materials (BOMs) and Schematics

The schematics (refer to Figure 3 – Figure 6) show typical implementations of the chip set controller for capacitive and resistive touchscreen applications. You can modify the basic schematic to include RS-232 level translation for serial communication, or voltage pre-regulation as required by the available voltages in the host system.

Table 9 lists the bill of materials for the schematics shown in Figure 3 and Figure 4.

Table 9. Bill of Materials for Capacitive and Resistive Touchscreens with Cable NovRAM

Item	Quantity	Part Description	Reference Designators
1	2	22pF 10% COG 25V	C1 C2
2	1	6.8uF 10V Tantalum	C3
3	6	0.01uF X7R 25V	C12 C13 C14 C15 C16 C17
4	6	0.1uF X7R 25V	C4 C5 C6 C7 C8 C9 C10 C11
5	7	MMBD7000 dual diodes	D1 D2 D3 D4 D5 D7 D8
6	1	LED @5 mA (optional)	D6
7	1	Molex 10-88-1121 (2x6, .1C)	J1
8	4	Murata BLM21A102SPT Fair-Rite 2508051027	L1 L2 L3 L4
9	1	82.5K 1% 1/10W	R1 (R2 and R3 are not used.)
10	3	100 5% 1/10W	R4 R5 R6
11	2	Shorting-plugs (optional)	SP1 SP2 (Shorting-plugs, SP1 SP2, are required to implement multi-mode applications.)
12	1	93C46 EEPROM	U4
13	1	80C32 ROMLESS uP	U2
14	1	Excalibur* (MicroTouch P/N 19-550)	U1*
15	1	27C020 150 ns	U4 (MicroTouch supplies the firmware. For single and dual-mode applications, a 27C512 and 27C010 may be used, respectively.)
16	2	Motorola MC33072/MC34072	U5, U6
17	1	11.0592 MHz	Y1

** All components except the Excalibur ASIC are non-proprietary.*

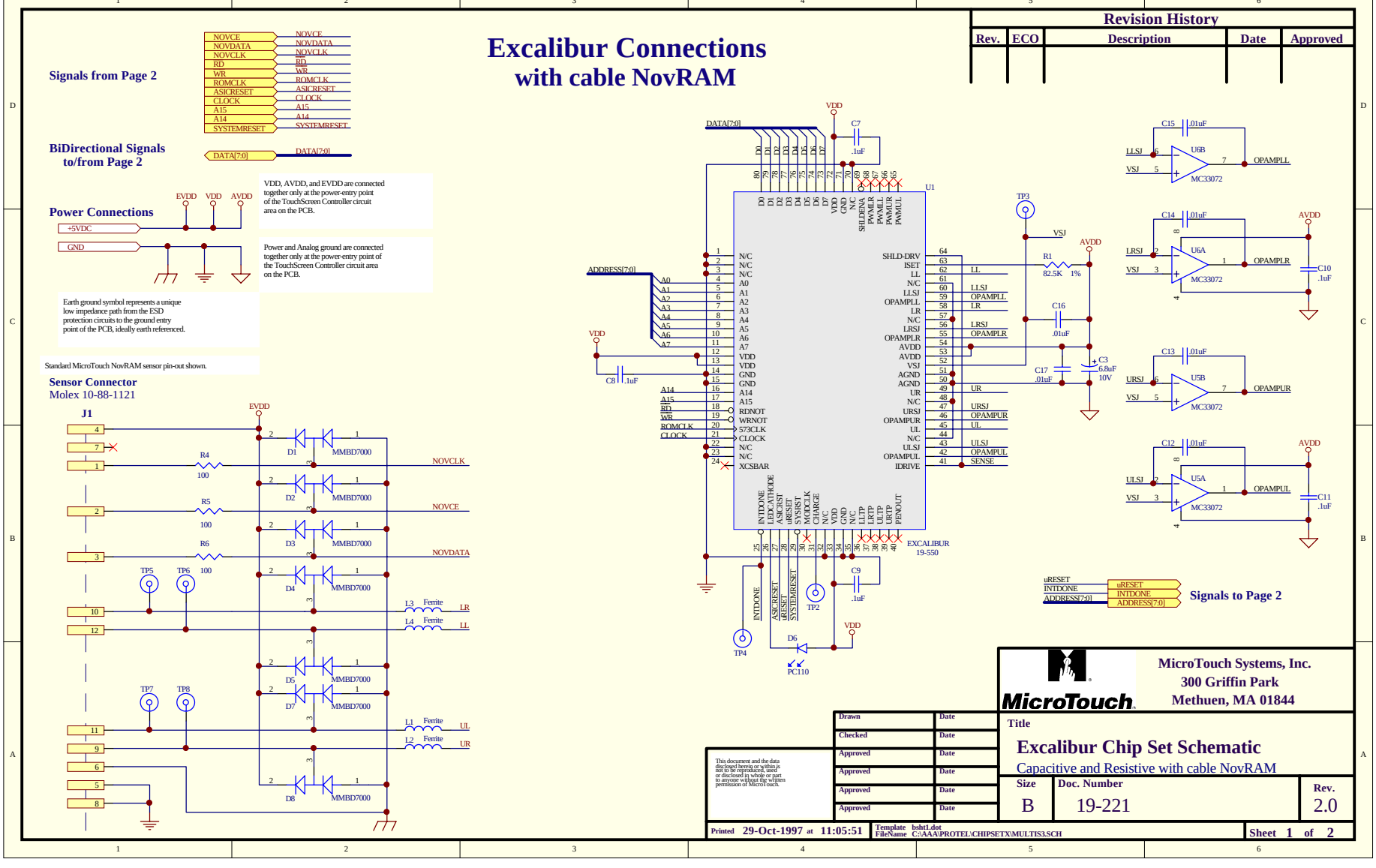

Figure 3. Excalibur Chip Set Schematic for Capacitive and Resistive Touchscreens with Cable NovRAM (Sheet 1 of 2)

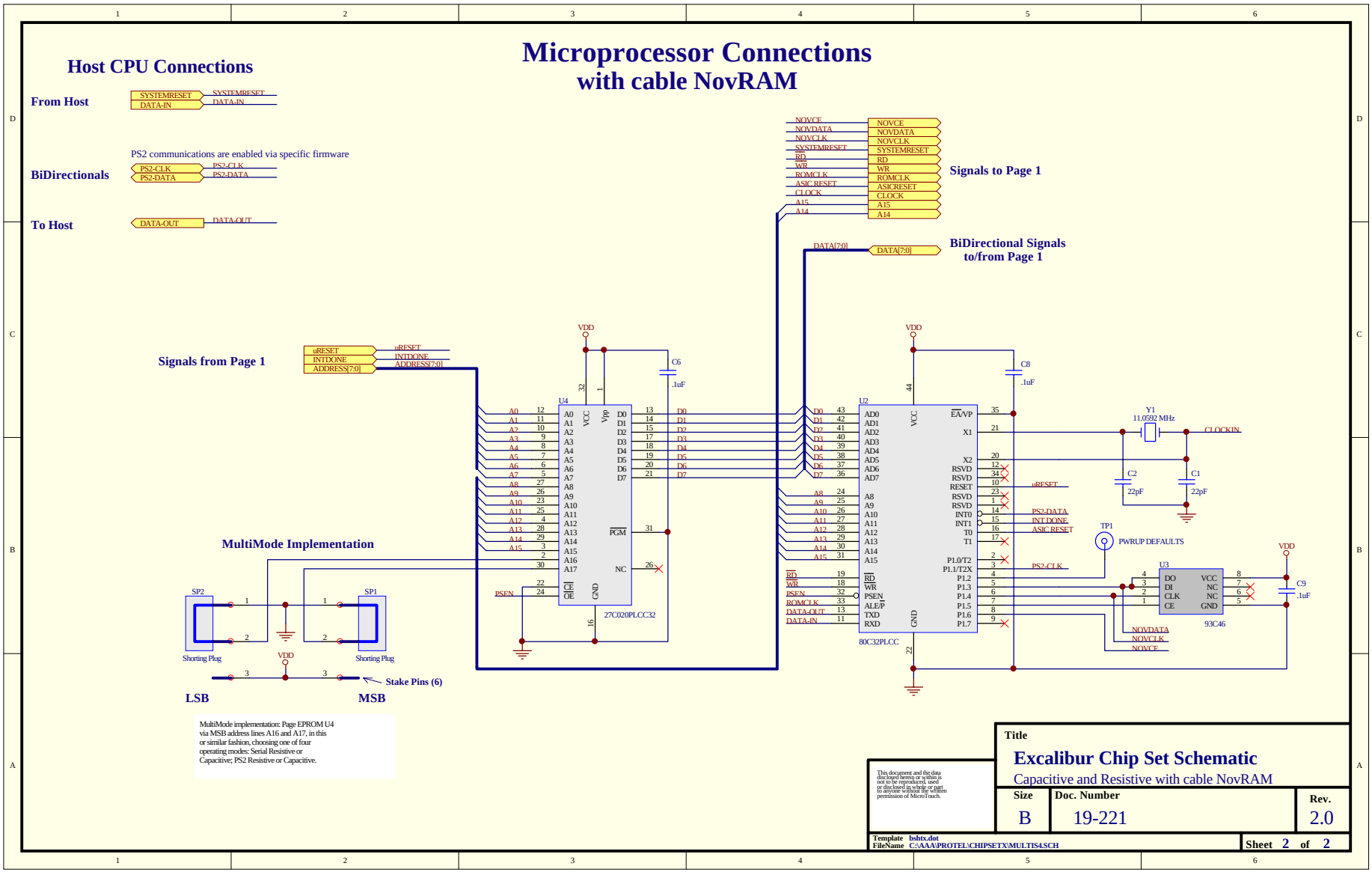

Figure 4. Excalibur Chip Set Schematic for Capacitive and Resistive Touchscreens with Cable NovRAM (Sheet 2 of 2)

Table 10 lists the bill of materials for the schematics shown in Figure 5 and Figure 6.

Table 10. Bill of Materials for Capacitive and Resistive Touchscreens without Cable NovRAM

Item	Quantity	Part Description	Reference Designators
1	2	22pF 10% COG 25V	C1 C2
2	1	6.8uF 10V Tantalum	C3
3	6	0.01uF X7R 25V	C12 C13 C14 C15 C16 C17
4	8	0.1uF X7R 25V	C4 C5 C6 C7 C8 C9 C10 C11
5	5	MMBD7000 dual diodes	D1 D2 D3 D4 D5
6	1	LED @5 mA (optional)	D6
7	1	5 pin connector (consult MicroTouch for specification)	J1
8	4	Murata BLM21A102SPT Fair-Rite 2508051027	L1 L2 L3 L4
9	1	82.5K 1% 1/10W	R1
10	2	1Meg 5% 1/10W	R2, R3 (R2 and R3 are required for resistive and multi-mode applications; not required for capacitive-only designs.)
11	3	Shorting-plugs (optional)	SP1 SP2 SP3 (Shorting-plugs, SP1 SP2 SP3, are required to implement multi-mode applications.)
12	1	93C46 EEPROM	U4
13	1	80C32 ROMLESS uP	U2
14	1	Excalibur* (MicroTouch P/N 19-550)	U1*
15	1	27C020 150 ns	U4 (MicroTouch supplies the firmware. For single and dual-mode applications, a 27C512 and 27C010 may be used, respectively.)
16	2	Motorola MC33072/MC34072	U5, U6
17	1	11.0592 MHz	Y1

** All components except the Excalibur ASIC are non-proprietary.*

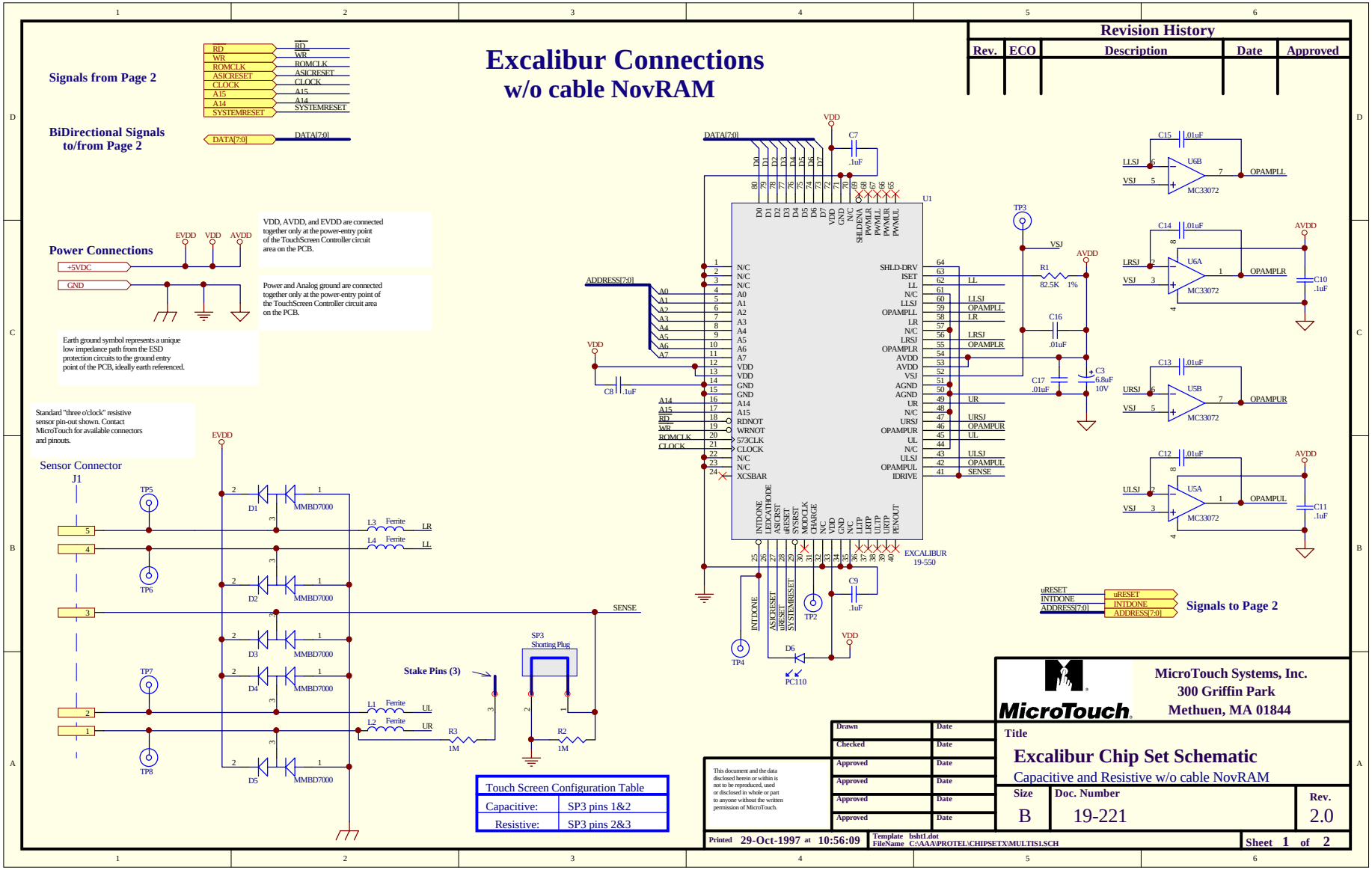

Figure 5. Excalibur Chip Set Schematic for Capacitive and Resistive Touchscreens without Cable NovRAM (Sheet 1 of 2)

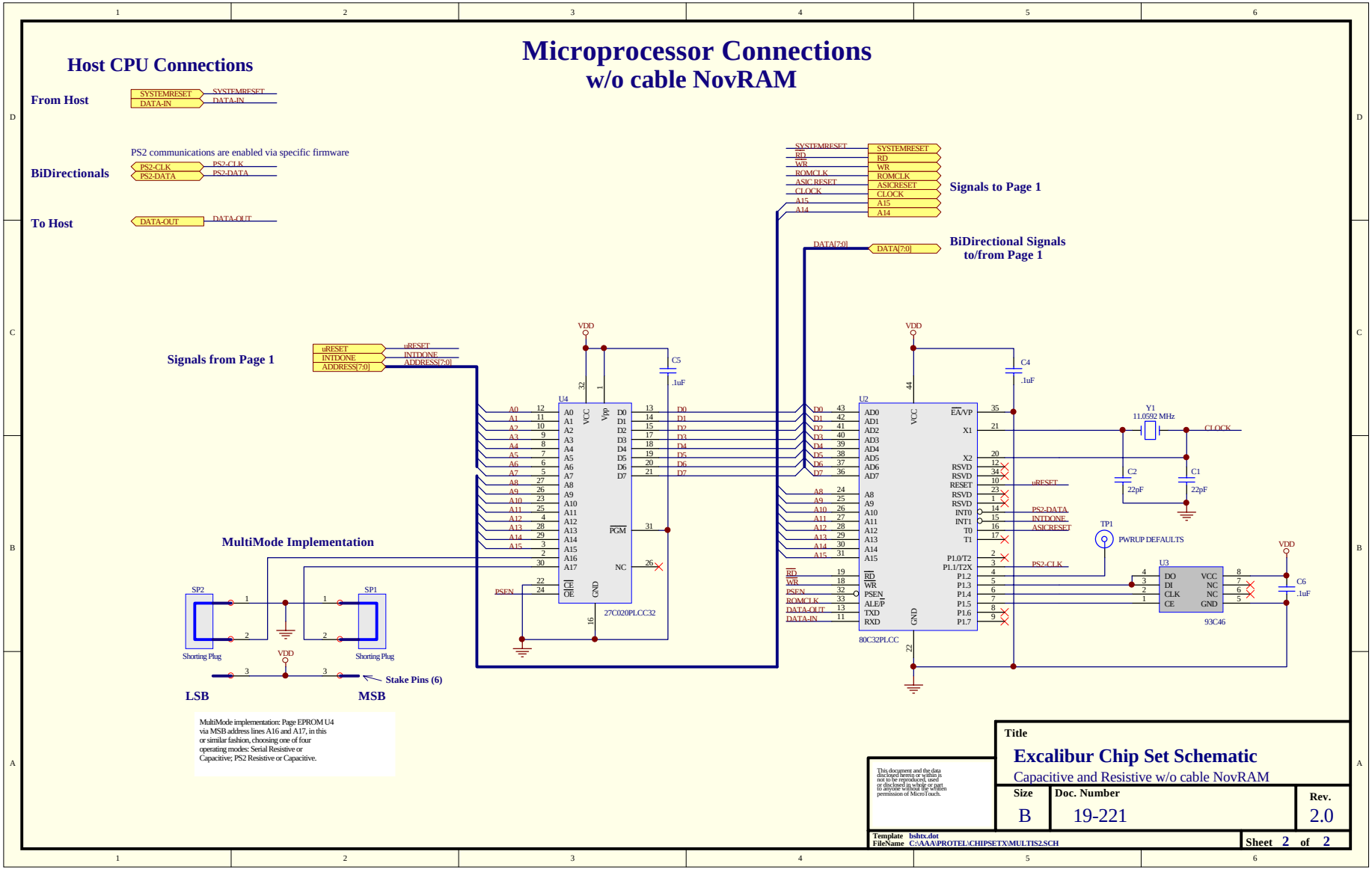

Figure 6. Excalibur Chip Set Schematic for Capacitive and Resistive Touchscreens without Cable NovRAM (Sheet 2 of 2)