

# FAN73611

## Single-Channel High-Side Gate Drive IC

### Features

- Floating Channel for Bootstrap Operation to +600V
- 250mA/500mA Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Canceling Circuit
- 3.3V and 5V Input Logic Compatible
- Output In Phase with Input Signal
- Under-Voltage Lockout for  $V_{DD}$  and  $V_{BS}$
- 8-Lead Small Outline Package (SOP)

### Applications

- High-Speed Gate Driver
- Plasma Display Panel
- Switching-Mode Power Supply (SMPS)
- Motor Drive Inverter

### Description

The FAN73611 is a monolithic high-side gate drive IC that can drive MOSFETs and IGBTs operating up to +600V. Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -9.8V$  (typical) for  $V_{BS} = 15V$ . The UVLO circuits prevents malfunction when  $V_{DD}$  or  $V_{BS}$  is lower than the specified threshold voltage. The output drivers typically source/sink 250mA/500mA; respectively, which is suitable for Plasma Display Panel (PDP) application, motor drive inverter, and switching mode power supply applications.

8-SOP



### Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN73611M <sup>(1)</sup>	8-Lead, Small-Outline Package (SOP)	-40°C ~ 125°C	Tube
FAN73611MX <sup>(1)</sup>			Tape & Reel

#### Note:

1. These devices passed wave soldering test by JESD22A-111.

## Typical Application Diagrams

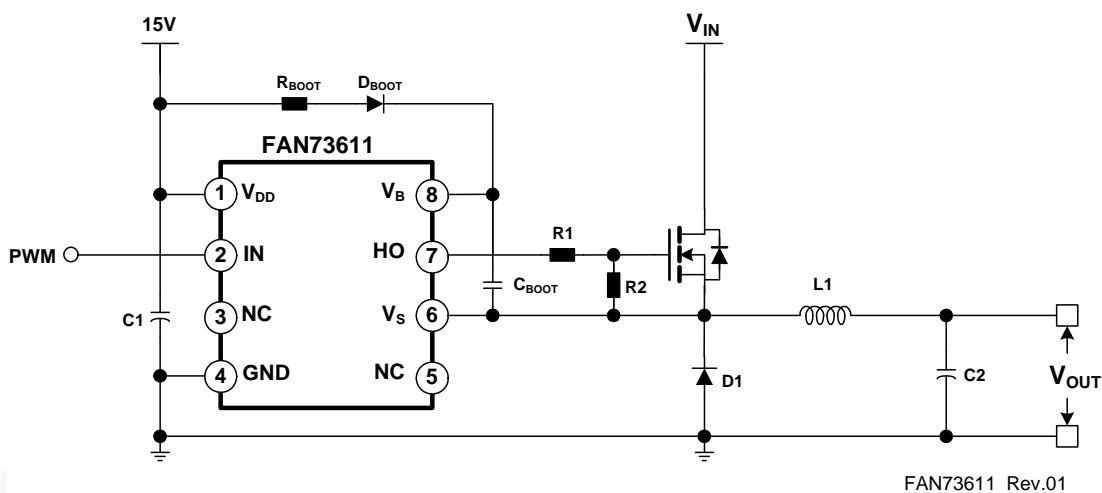


Figure 1. Step-Down (Buck) DC-DC Converter Application

## Internal Block Diagram

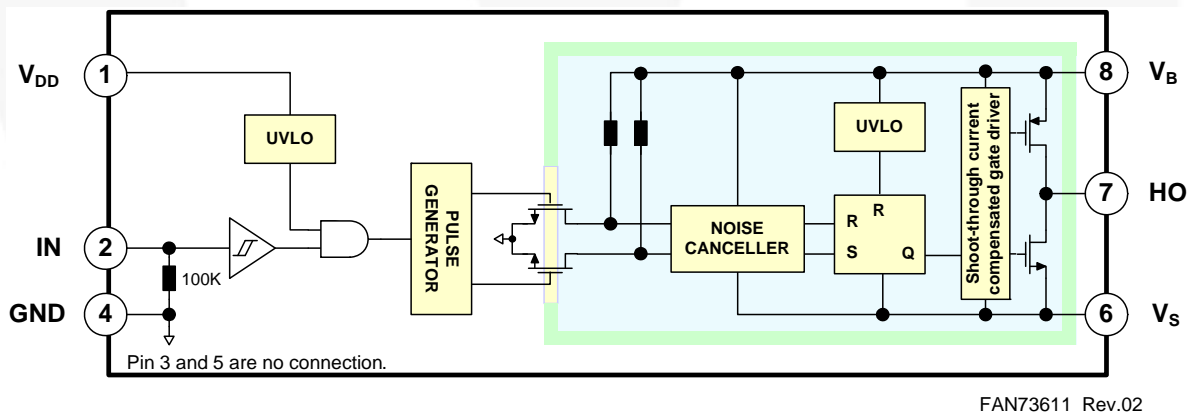


Figure 2. Functional Block Diagram

## Pin Configuration

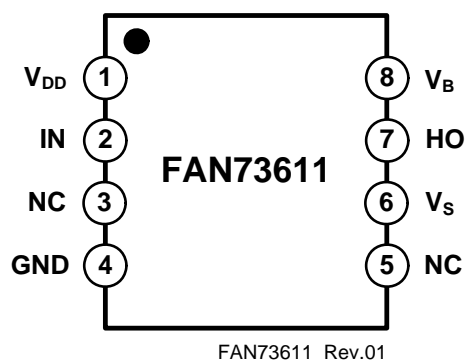


Figure 3. Pin Configuration (Top View)

## Pin Definitions

Pin #	Name	Description
1	$V_{DD}$	Supply Voltage
2	IN	Logic Input for High-Side Gate Driver Output
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	$V_S$	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	$V_B$	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}\text{C}$  unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
$V_S$	High-Side Floating Offset Voltage	$V_B-25$	$V_B+0.3$	V
$V_B$	High-Side Floating Supply Voltage	-0.3	625.0	V
$V_{HO}$	High-Side Floating Output Voltage	$V_S-0.3$	$V_B+0.3$	V
$V_{DD}$	Low-Side and Logic Supply Voltage	-0.3	25.0	V
$V_{IN}$	Logic Input Voltage	-0.3	$V_{DD}+0.3$	V
$dV_S/dt$	Allowable Offset Voltage Slew Rate		$\pm 50$	V/ns
$P_D$	Power Dissipation <sup>(2, 3, 4)</sup>		0.625	W
$\theta_{JA}$	Thermal Resistance		200	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction Temperature	-55	+150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature	-55	+150	$^{\circ}\text{C}$

### Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:  
*JESD51-2: Integrated circuits thermal test method environmental conditions, natural convection, and*  
*JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.*
- Do not exceed power dissipation ( $P_D$ ) under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S+10$	$V_S+20$	V
$V_S$	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
$V_{HO}$	High-Side Output Voltage	$V_S$	$V_B$	V
$V_{IN}$	Logic Input Voltage	GND	$V_{DD}$	V
$V_{DD}$	Supply Voltage	10	20	V
$T_A$	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$

## Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS}) = 15.0V$  and  $T_A = 25^\circ C$  unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND. The  $V_O$  and  $I_O$  parameters are relative to  $V_S$  and are applicable to the respective output HO.

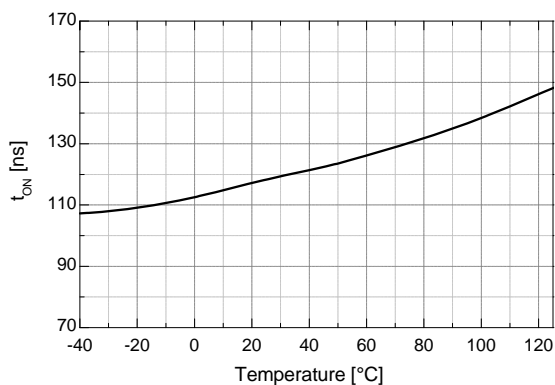
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<b>Power Supply Section</b>						
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN}=0V$ or $5V$ , $C_{LOAD}=1000pF$		80	140	$\mu A$
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$C_{LOAD}=1000pF$ , $f_{IN}=20KHz$ , RMS value		80	160	$\mu A$
$V_{DDUV+}$ $V_{BSUV+}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Positive Going Threshold Voltage	$V_{DD}=\text{Sweep}$ , $V_{BS}=\text{Sweep}$	7.8	8.8	9.8	V
$V_{DDUV-}$ $V_{BSUV-}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Negative Going Threshold Voltage	$V_{DD}=\text{Sweep}$ , $V_{BS}=\text{Sweep}$	7.3	8.3	9.3	V
$V_{DDHYS}$ $V_{BSHYS}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage	$V_{DD}=\text{Sweep}$ , $V_{BS}=\text{Sweep}$		0.5		V
$I_{LK}$	Offset Supply Leakage Current	$V_B=V_S=600V$			10	$\mu A$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN}=0V$ or $5V$ , $C_{LOAD}=1000pF$		60	100	$\mu A$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$C_{LOAD}=1000pF$ , $f_{IN}=20KHz$ , RMS Value		420	600	$\mu A$
<b>Input Logic Section</b>						
$V_{IH}$	Logic "1" Input Voltage		2.5			V
$V_{IL}$	Logic "0" Input Voltage				0.8	V
$I_{IN+}$	Logic Input High Bias Current	$V_{IN}=5V$		50	75	$\mu A$
$I_{IN-}$	Logic Input Low Bias Current	$V_{IN}=0V$			2	$\mu A$
$R_{IN}$	Input Pull-Down Resistance		60	100		$K\Omega$
<b>Gate Driver Output Section</b>						
$V_{OH}$	High Level Output Voltage ( $V_{BIAS} - V_O$ )	No Load			0.1	V
$V_{OL}$	Low Level Output Voltage	No Load			0.1	V
$I_{O+}$	Output High, Short-Circuit Pulsed Current	$V_{HO}=0V$ , $V_{IN}=5V$ , $PW \leq 10\mu s$	200	250		mA
$I_{O-}$	Output Low, Short-Circuit Pulsed Current	$V_{HO}=15V$ , $V_{IN}=0V$ , $PW \leq 10\mu s$	400	500		mA
$V_S$	Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO	$V_{BS}=15V$		-9.8	-7.0	V

## Dynamic Electrical Characteristics

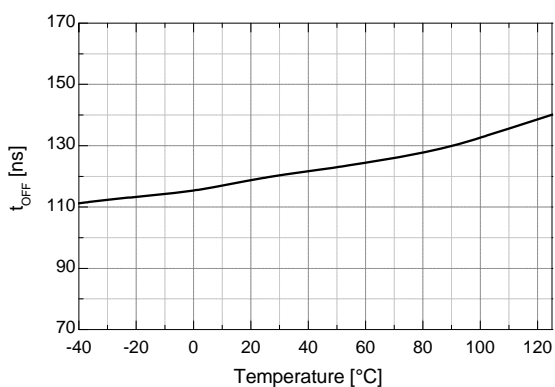
$V_{DD}=V_{BS}=15V$ ,  $C_{LOAD}=1000pF$ , and  $T_A=25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-On Propagation Delay Time	$V_S=0V$	70	120	170	ns
$t_{off}$	Turn-Off Propagation Delay Time	$V_S=0V$	70	120	170	ns
$t_r$	Turn-On Rise Time			70	140	ns
$t_f$	Turn-Off Fall Time			30	60	ns

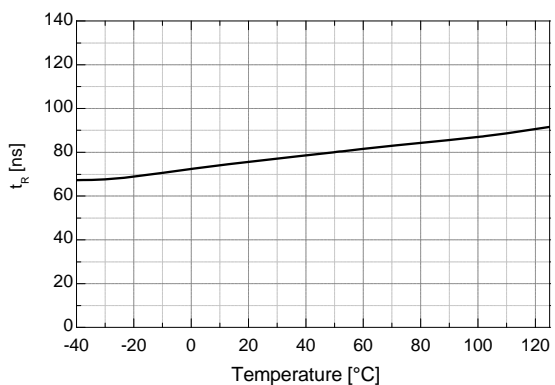
## Typical Characteristics



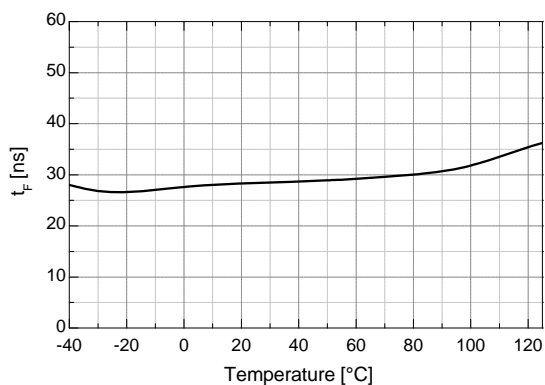
**Figure 5. Turn-On Propagation Delay vs. Temperature**



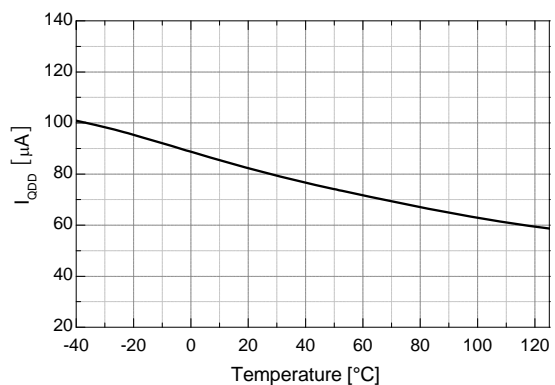
**Figure 6. Turn-Off Propagation Delay vs. Temperature**



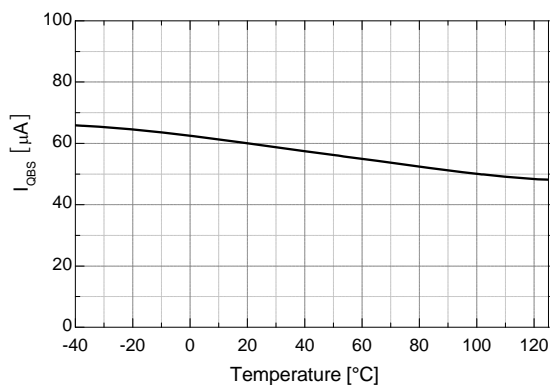
**Figure 7. Turn-On Rise Time vs. Temperature**



**Figure 8. Turn-Off Fall Time vs. Temperature**



**Figure 9. Quiescent  $V_{DD}$  Supply Current vs. Temperature**



**Figure 10. Quiescent  $V_{BS}$  Supply Current vs. Temperature**

# Typical Characteristics (Continued)

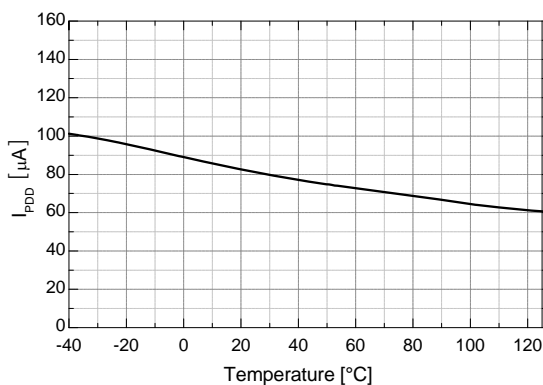


Figure 11. Operating  $V_{DD}$  Supply Current vs. Temperature

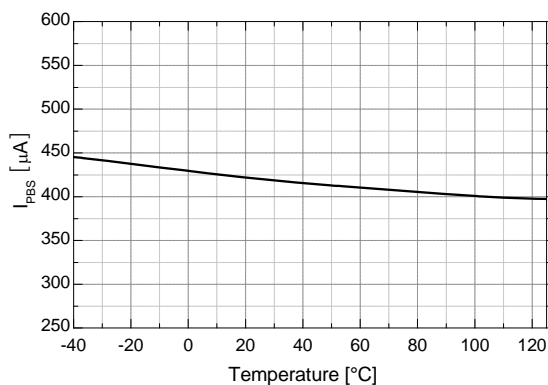


Figure 12. Operating  $V_{BS}$  Supply Current vs. Temperature

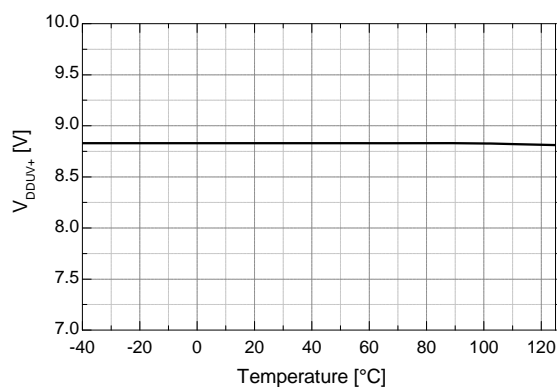


Figure 13.  $V_{DD}$  UVLO+ vs. Temperature

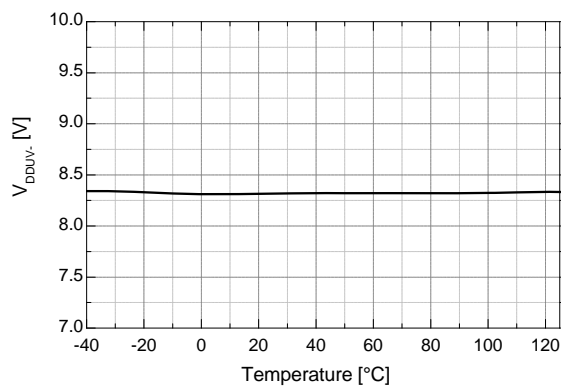


Figure 14.  $V_{DD}$  UVLO- vs. Temperature

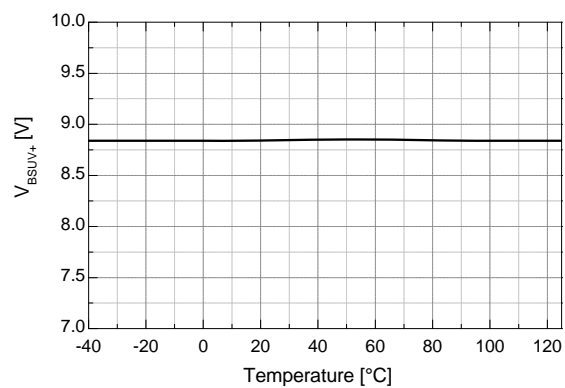


Figure 15.  $V_{BS}$  UVLO+ vs. Temperature

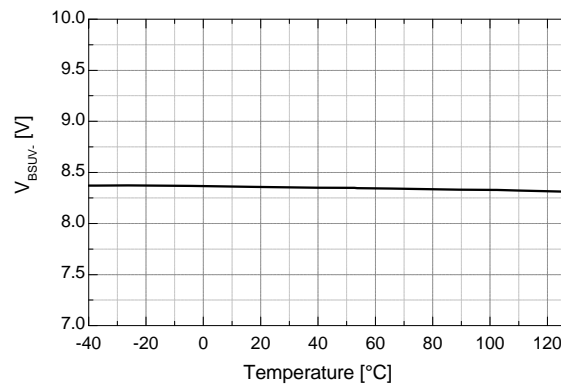
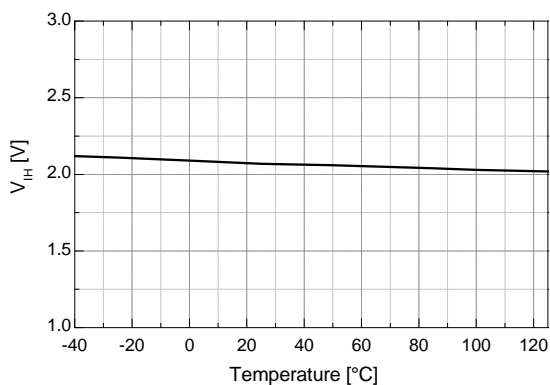
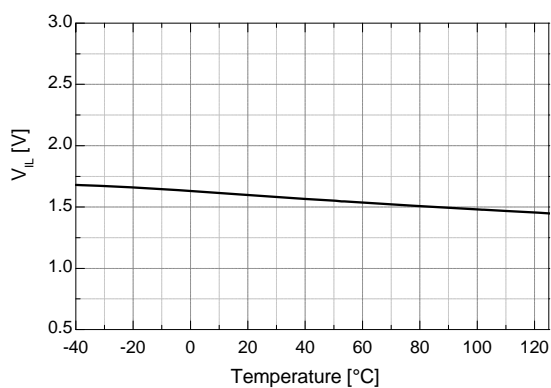


Figure 16.  $V_{BS}$  UVLO- vs. Temperature

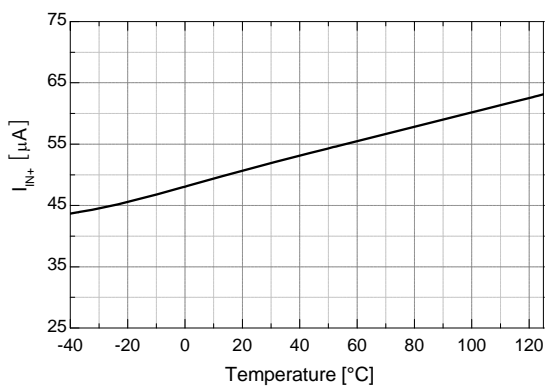
## Typical Characteristics (Continued)



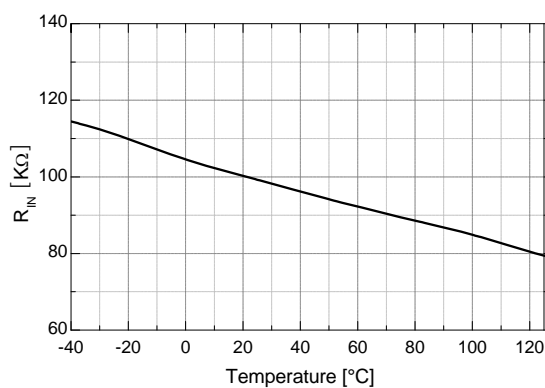
**Figure 17. Logic HIGH Input Voltage vs. Temperature**



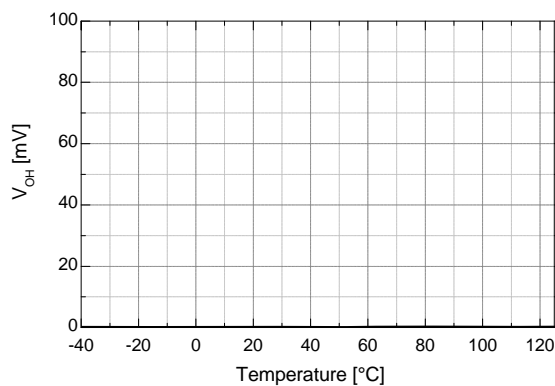
**Figure 18. Logic LOW Input Voltage vs. Temperature**



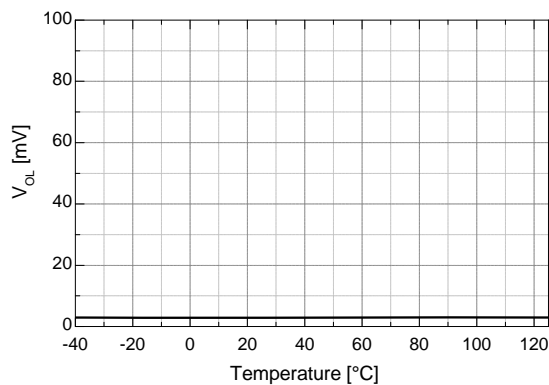
**Figure 19. Logic HIGH Input Bias Current vs. Temperature**



**Figure 20. Input Pull-Down Resistance vs. Temperature**



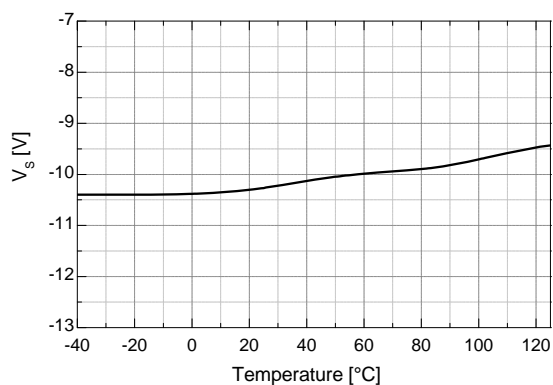
**Figure 21. High-Level Output Voltage vs. Temperature**



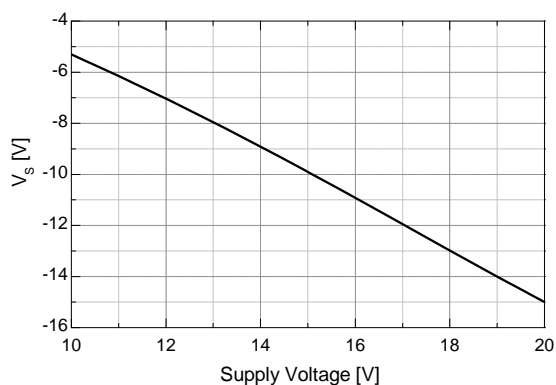
**Figure 22. Low-Level Output Voltage vs. Temperature**



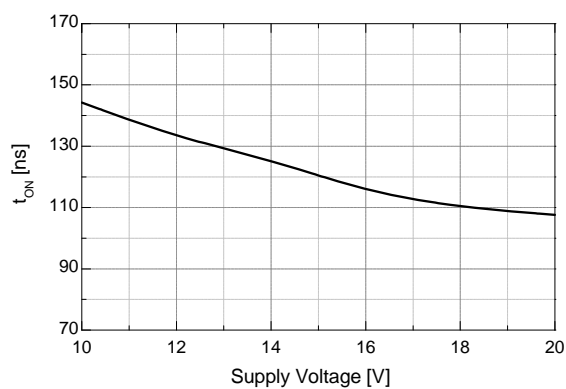
## Typical Characteristics (Continued)



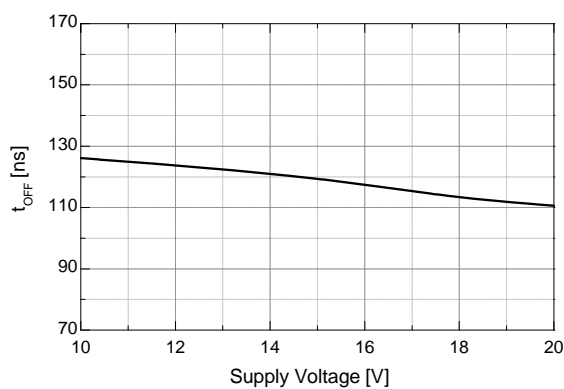
**Figure 23. Allowable Negative  $V_S$  Voltage vs. Temperature**



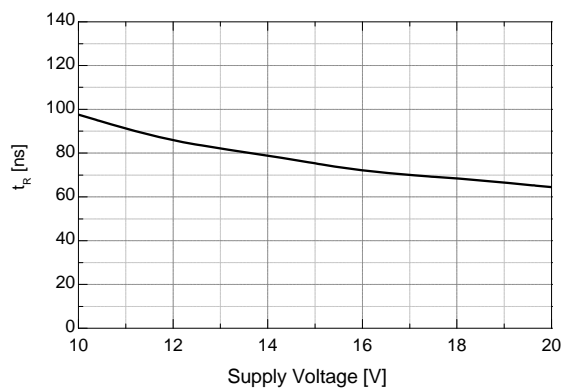
**Figure 24. Allowable Negative  $V_S$  Voltage vs. Supply Voltage**



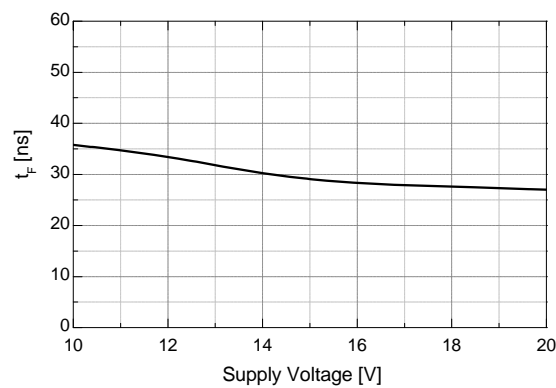
**Figure 25. Turn-On Propagation Delay vs. Supply Voltage**



**Figure 26. Turn-Off Propagation Delay vs. Supply Voltage**

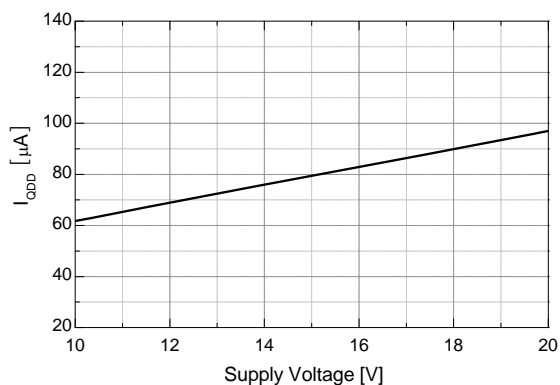


**Figure 27. Turn-On Rise Time vs. Supply Voltage**

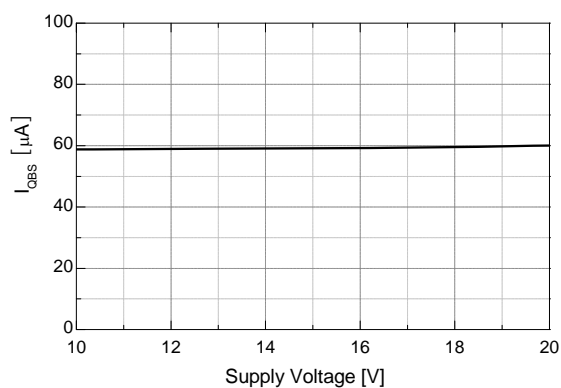


**Figure 28. Turn-Off Fall Time vs. Supply Voltage**

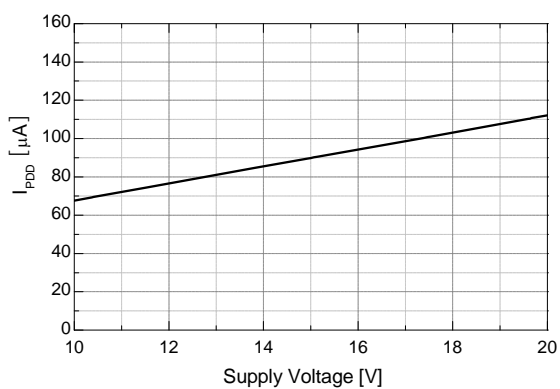
## Typical Characteristics (Continued)



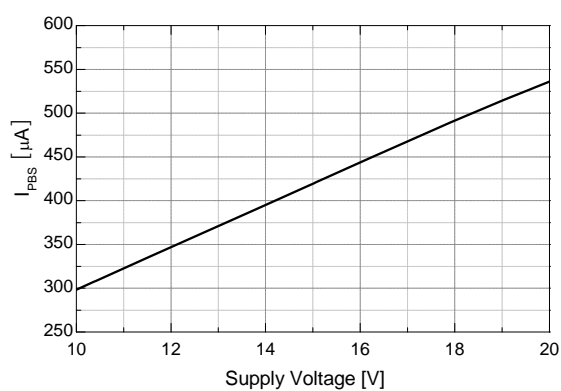
**Figure 29. Quiescent  $V_{DD}$  Supply Current vs. Supply Voltage**



**Figure 30. Quiescent  $V_{BS}$  Supply Current vs. Supply Voltage**



**Figure 31. Operating  $V_{DD}$  Supply Current vs. Supply Voltage**



**Figure 32. Operating  $V_{BS}$  Supply Current vs. Supply Voltage**

FAN73611 Rev.02

The schematic diagram illustrates the FAN73611 inverter circuit. The circuit is powered by a 15V supply. A UF4007 diode is connected between the 15V supply and the V<sub>DD</sub> pin of the FAN73611. A 10µF capacitor is connected between the 15V supply and ground. A 0.1µF capacitor is connected between the V<sub>B</sub> pin and ground. A 1000pF capacitor is connected between the V<sub>S</sub> pin and ground. The FAN73611 is connected with V<sub>DD</sub>, V<sub>B</sub>, V<sub>S</sub>, IN, and HO pins. A square wave input is applied to the IN pin. The output monitor is connected to the V<sub>S</sub> and HO pins. A graph shows the output voltage -V<sub>S</sub> over time.

FAN73611 Rev.03

## Physical Dimensions

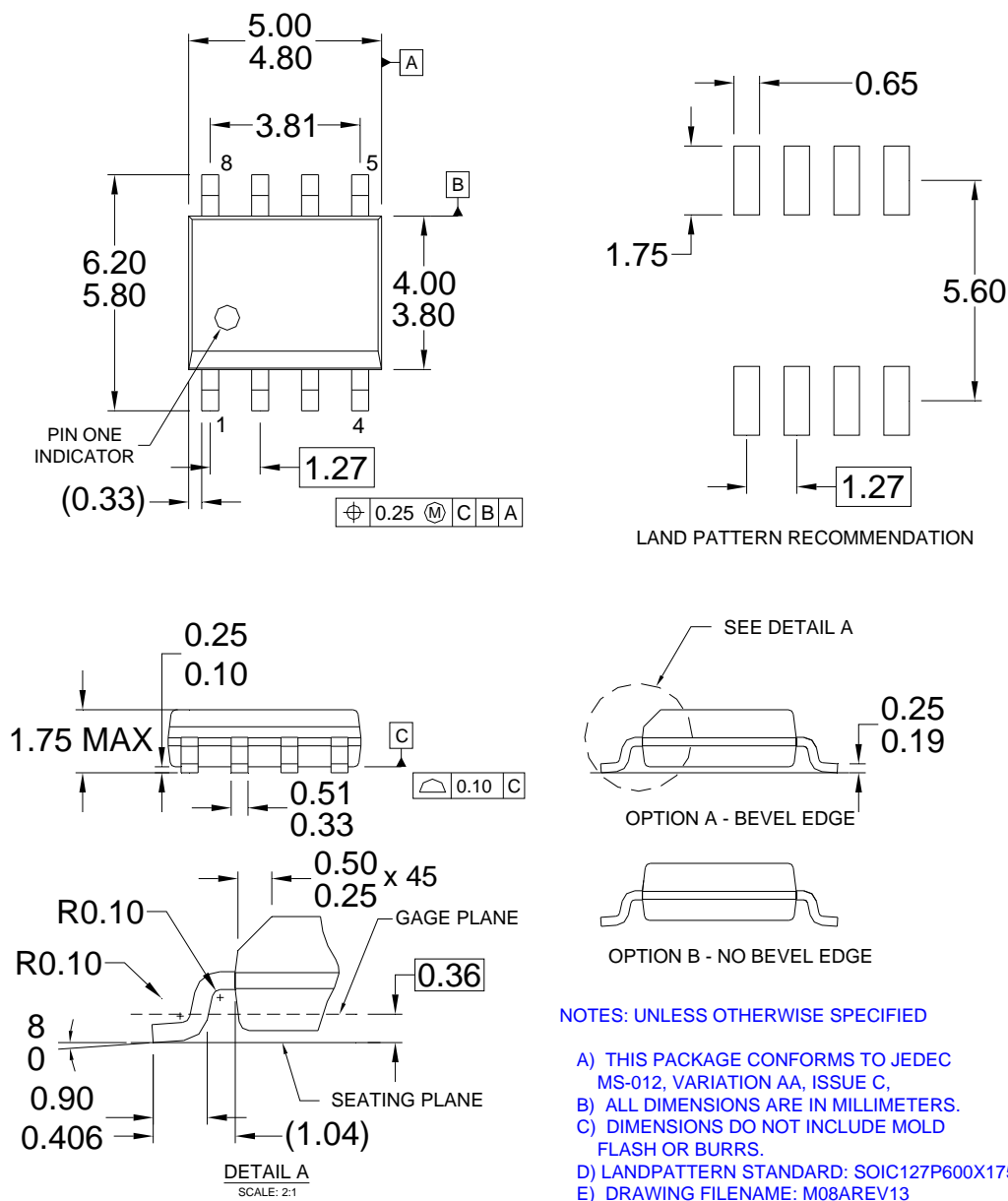


Figure 35. 8-Lead, Small Outline Package (SOP)

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### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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