High Efficiency Single-stage Grid-tied PV Inverter for Renewable Energy System

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(ABSTRACT)

A single-phase grid connected transformerless photovoltaic (PV) inverter for residential application is presented. The inverter is derived from a boost cascaded with buck converter along with a line frequency unfolding circuit. Due to its novel operating modes, high efficiency can be achieved because there is only one switch operating at high frequency at a time, and the converter allows the use of power MOSFET and ultra-fast reverse recovery diode. This dissertation begins with theoretical analysis and modeling of this boost-buck converter based inverter. And the model indicates small boost inductance will leads to increase the resonant pole frequency and decrease the peak of Q, which help the system be controlled easier and more stable. Thus, interleaved multiple phases structure is proposed to have small equivalent inductance, meanwhile the ripple can be decreased, and the inductor size can be reduced as well. A two-phase interleaved inverter is then designed accordingly.

The double-carrier modulation method is proposed based on the inverter's operation mode. The duty cycle for buck switch is always one if the inverter is running in boost mode. And the duty cycle for boost switches are always zero if the inverter is running in buck mode. Because of this, the carrier for boost mode is stacked on the top of

the carrier for buck mode, as a result, there is no need to compare the input and output voltage to decide which mode the inverter should operate in. And the inverter operates smoothly between these two modes. Based on similar concept, three advanced modulation methods are proposed. One of them can help further improve the efficiency, and one of them can help increase the bandwidth and gain, and the last one takes the advantage of both.

Based on similar concept, another three dual-mode double-carrier based SPWM inverters are proposed. With both step-up and step-down functions, this type of inverter can achieve high efficiency in a wide range because only one switch operates at the PWM frequency at a time.

Finally, the simulation and experiment results are shown to verify the concept and the tested CEC (California Energy Commission) efficiency is 97.4%. It performs up to 2% more efficiently better than the conventional solution.

To my parents
Xuesen Zhao and Peifeng Xie

To my husband
Bo Zhou

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Table of Contents

List of Figures

List of Tables

Chapter 1:
Introduction

1.1 Background

With the worsening of the world's energy shortage and environmental pollution problems, protecting the energy and the environment becomes the major problems for human beings. Thus the development and application of clean renewable energy, such as solar, wind, fuel cell, tides and geothermal heat etc., are getting more and more attention. Among them, solar power will be dominant because of its availability and reliability. As predicted by [1], the solar will provide the electricity up to 64% of the total energy by the end of this century as shown in Figure 1.1.

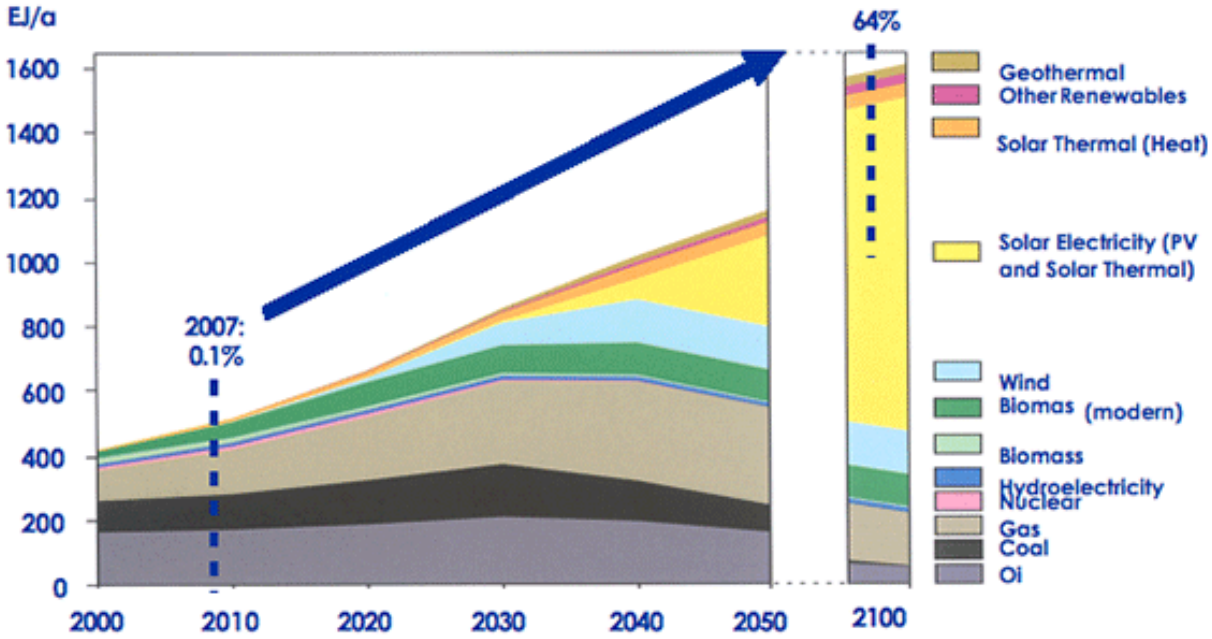


Figure 1.1 Global energy use by source in the 21st century [1].

Photovoltaic (PV) power generation has become one of the main ways to use solar energy. And the renewable energy source based distributed generation (DG) system are normally interfaced to the grid through power electronic converters or inverters [2] as shown in Figure 1.2. Thus developing a photovoltaic grid-connected inverter system is important for the mitigation of energy and environmental issues.

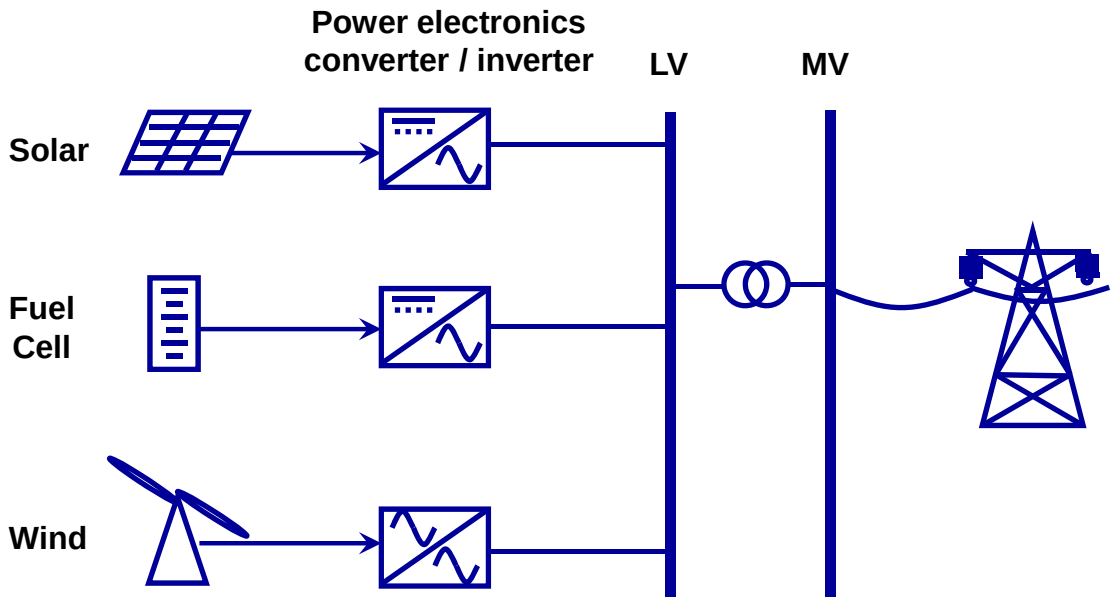


Figure 1.2 Renewable energy based distributed generation system.

1.2 Photovoltaic

Photovoltaic (PV) is a method of generating electrical power by converting solar radiation into direct current electricity using semiconductors that exhibit the photovoltaic effect. The basic PV cell model is presented in Figure 1.3 [3].

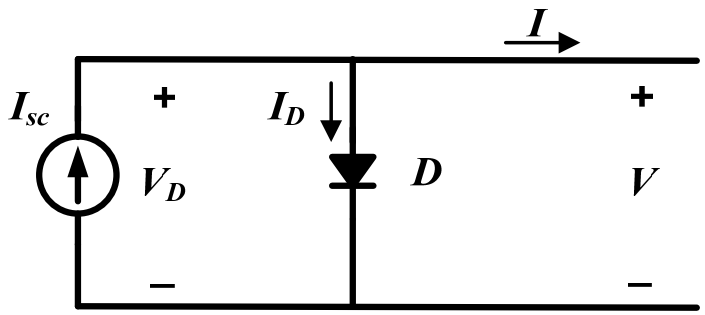


Figure 1.3 Basic PV cell model

Then the equations (1.1) through (1.3) could be obtained.

$$I_D = I_{sc} - I \tag{1.1}$$

$$I_D = I_s \cdot \left(e^{\frac{V}{n \cdot V_T}} - 1 \right) \tag{1.2}$$

$$I_D = I_{sc} - I_s \cdot \left(e^{\frac{V}{n \cdot V_T}} - 1 \right) \tag{1.3}$$

Where I_{sc} is the photo current; I_s is diode reverse saturation current; n is diode ideality factor normally between 1 and 5; $V_T = k \cdot T/q$ is temperature voltage, which is 25.7 mV at 25°C; k is Boltzmann constant, which is $1.38 \cdot 10^{-23}$ J/K; T is temperature in K and q is electron charge which is $1.6 \cdot 10^{-19}$ C.

Based on its model, Figure 1.4 could be obtained to represent the typical 72-cell PV module's current and power characteristics under different irradiations and different temperatures.

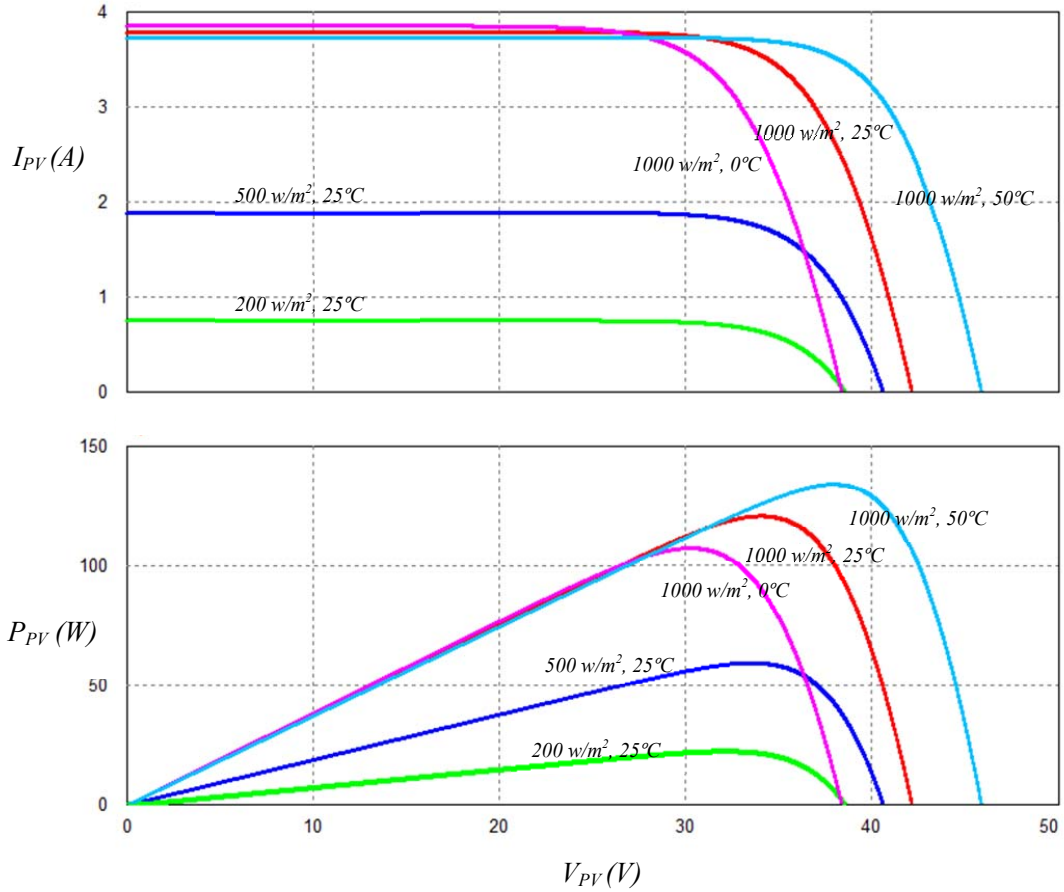


Figure 1.4 Photovoltaic module's current and power characteristics under different irradiation and temperature conditions.

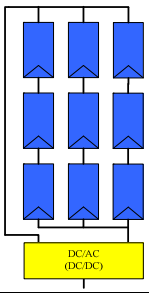
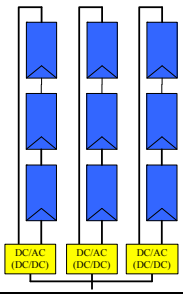
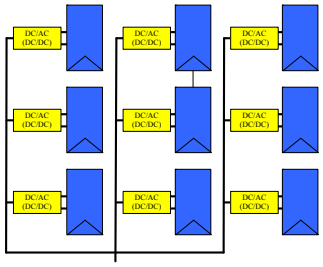
It can be observed that the PV module's short circuit current highly depends on the radiation. High radiation leads to large short circuit current. And the temperature impacts more on the open circuit voltage. High temperature leads to small open circuit voltage.

Because of its *I-V* and *P-V* characteristics, maximum power point tracking *(MPPT*) is required to extract the maximum energy that the PV module can produce.

1.3 Inverters for Photovoltaic Applications

Because photovoltaic devices generate direct current electricity with its unique *I-V* characteristics, power electronics are required to help convert its maximum power for different applications. The typical applications include PV power plants, residential PV, building integrated PV (BIPV) and PV lighting. For PV power plants, one or several centralized inverter upto1 MW is required to convert the DC power to AC power. For residential PV, a string type inverter between 1 kW and 10 kW or many micro-inverters are required to converter the power. The residential PV application utilizes either a stand-alone system or a grid-tied system. Stand-along system is always used for some remote area. In this system, the outputs of power converters or inverters connect to the local load instead of connecting to the grid. Batteries are required to store the energy for night consumption [4]. In grid-tied system, the outputs of power converters or inverters connect to the grid directly. BIPV means that PV materials are used to replace conventional building materials in parts of the building envelope such as the roof, skylight, or facades [5]. In this application, a converter is required for each panel for energy conversion [6]. And in lighting application, a converter is normally required for each panel to charge a battery for powering lamps at night [7]. Table 1.1 lists different types of PV inverters or converters.

Table 1.1 Comparisons of different types of PV inverter/converter.

Type	Central	String	Module
Circuit Topology			
DC bus	High voltage, high current	High voltage, low current	Low voltage, low current
Features	Higher power losses, mismatch losses, inflexible design, high current harmonics, lower power quality	Separate MPPT for each string, higher overall efficiency than central inverter	Higher installation cost, no mismatch losses, individual MPPT, flexible design for expansion, lower efficiency

Among these, PV power supplied to the utility grid is gaining more and more attention [8]-[13]. As a PV grid-tied inverter, it also needs to meet the requirement from the utility side. The standard IEEE 1547 [14] deals with issues as power quality, detection of islanding operation, DC current injection etc. Table 1.2 lists the requirements of IEEE 1547 standard.

Table 1.2 IEEE 1547 requirements.

Nominal power	30 kW
Harmonic currents	(2-10) 4.0% (11-16) 2.0% (17-22) 1.5% (23-34) 0.6% (>35) 0.3% THD 5%
DC current injection	< 0.5% of rated output current
Abnormal voltage disconnection	V < 50% or V >137% 6 cycles 50%< V < 88% or 110%< V < 137% 120 cycles
Abnormal frequency disconnection	f < rated – 0.7 Hz 6 cycles f > rated + 0.5 Hz 6 cycles

Numerous inverter circuits and control schemes can be used for PV power conditioning system (PCS). For residential PV power generation systems, single-phase utility interactive inverters are of particular interest [15]-[19]. This type of application normally requires a power level lower than 5 kW [16][20] and a high input voltage stack that provides a dc voltage around 400 V. However, depending on the characteristics of PV panels, the total output voltage from the PV panels varies a lot due to different temperature, irradiation conditions and the shading & clouding effects. Thus, the input voltage of a residential PV inverter can vary in a wide range, for example from 200 V to 500 V, which appears to be highly mismatched with the desirable 400-V level. Therefore,

a dc-dc converter with either step-up or step-down function or even both step-up and -down functions is needed before the dc-ac inverter stage. Such a dc-dc converter in conjunction with a dc-ac inverter arrangement has been widely used in the state-of-the-art PV PCS.

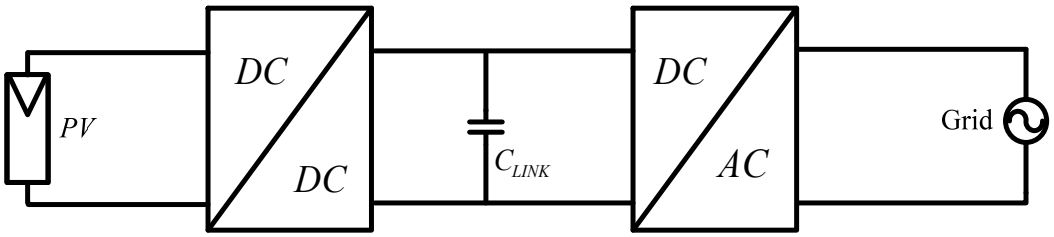


Figure 1.5 Conventional two-stage PV.

Figure 1.5 shows the block diagram of the PV PCS, which has two-stage high-frequency power conversion in cascaded configuration with dc link in the middle [21]-[25]. In this structure, the dc bus voltage should be boosted from the PV array, and the dc-ac stage can be a voltage source type high frequency inverter. Another option is to use line commuted inverter along with an isolated dc-dc stage [26]-[29]. There are many non-isolated single stage boost or buck-boost derived inverter topologies developed [30]-[33]. Their major drawbacks are limitation of input voltage range and/or requirement of two input sources [34][35]. With recent change of electric code that allows ungrounded PV panels, it is possible to replace the isolated dc-dc with non-isolated or transformerless dc-dc [36]. Without transformer, the dc-dc stage will be more reliable and cost effective [37]. This dissertation's focus is to develop a high efficiency transformeless inverter with both step-up and step-down functions.

1.4 Research Objectives and Outline

The research objectives are list as follows.

(i) Design an efficient residential power level PV inverter with wide input voltage range.

(ii) Establish a power stage model.

(iii) Design and implement a unified digital controller for smooth transition between modes.

(iv) Design the same-concept-based advanced controllers.

(v) Design the same-concept-based other efficient PV inverters.

The dissertation consists of six chapters, which are organized as follows.

Chapter 1 introduces the research background. The photovoltaic characteristic has been described. Some standards required for the inverters designed for grid-tied applications are introduced. At last, the research objectives are proposed.

In Chapter 2, the state-of-the-art single stage PV inverters are introduced. All of them produce rectified sinusoidal current in the SPWM power processing stage, and have additional switches for polarity selection. After that the energy storage used in this type of inverter and its lifetime issue are analyzed. Along with it, the lifetime issue of the electrolytic capacitors has been investigated. Because the capacitance also has an impact on MPPT efficiency, their relationship is also analyzed. Then, a novel boost-buck converter based single stage PV inverter has been presented. The first converter part operates in either boost or buck mode, thus it has a wide input voltage range, which is

good for PV application. The second inverter part is composed with unfolding circuit based on the direction of the grid. Thus from power processing point of view, this inverter is a single stage inverter. Because it process power either as a buck converter or a boost converter, high efficiency can be achieved.

In Chapter 3, averaged models for both modes have been established, which is the foundation for the controller design and optimization. After analyzing its model, an interleaved-boost-cascaded-with-buck (IBCB) converter is proposed to increase the resonant pole frequency by the use of smaller boost inductor value. As a result, the control loop bandwidth can be pushed further up to enhance the robustness of the complete system and helps the system be controlled easier. The MPPT Perturb and Observe (P&O) algorithm is introduced. In this inverter, MPPT gives an input voltage reference, which is the reference for the outer control loop. And the proposed circuit along with its controller has been designed, simulated, and tested with a hardware prototype. Finally, the results indicate that the efficiency of the proposed solution is around 2% higher than the conventional solution under the same condition and its tested CEC efficiency is 97.4%.

In Chapter 4, based on the modulation method proposed in Chpater 3, three advanced modulation methods are proposed. The first one - double-carrier with different frequencies can help further improve the efficiency. The second one - double-carrier with different magnitudes can help increase the bandwidth and gain. And the last one - double-carrier with different frequencies and magnitudes takes the advantage of both.

Chapter 5 proposed another three dual-mode double-carrier based SPWM inverters. With both step-up and step-down functions, this type of inverter can achieve

high efficiency in a wide range because only one switch operates at the PWM frequency at a time. The efficiencies and the detailed loss distribution of these inverters with one of the advanced modulation method are compared. Based on the comparison, boost mode with H5 PV inverter gives highest CEC efficiency in most cases, because it has lowest switching loss.

In Chapter 6, the conclusion is drawn and future works are summarized based upon the implementation experience and experimental results.

Chapter 2:
Proposed Single Stage High Efficiency Boost-Buck Converter Based PV Inverter

In this chapter, the state-of-the-art single stage PV inverters are reviewed firstly. For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage will be required to be higher than the peak of the grid voltage, which is not good for PV application because the PV panel's characteristics changes all the time. The energy storage needs to be at the front of a single stage inverter, and it is usually implemented by electrolytic capacitors. The lifetime issue of an electrolytic capacitor is introduced. And the conclusion can be drawn that although the electrolytic capacitors have limited lifetime, it can still be used by applying smaller voltage and current ripple to prolong its lifetime. Because the end of its life doesn't mean it failed, the electrolytic capacitor can work much longer than its estimated lifetime. As the capacitance also has an impact on MPPT efficiency, the larger capacitance leads to higher MPPT efficiency.

After that, a boost-buck converter based inverter is proposed. It operates in either boost or buck mode; thus, it has a wide input voltage range and high efficiency can be achieved. Then, the analysis of its middle capacitor and CCM/DCM operation condition is presented. Since the common-mode voltage in this inverter is equal to the grid voltage, it changes at line frequency. Thus, the leakage current of it is very small even at an extreme case.

2.1 Single Stage PV Inverter

2.1.1 State-of-the-art Single Stage PV Inverters

Here, single stage inverter is defined as an inverter with one stage of high frequency power processing. That means it has only one high switching frequency stage. Figure 2.1 through Figure 2.3 show the state-of-the-art single stage PV inverters.

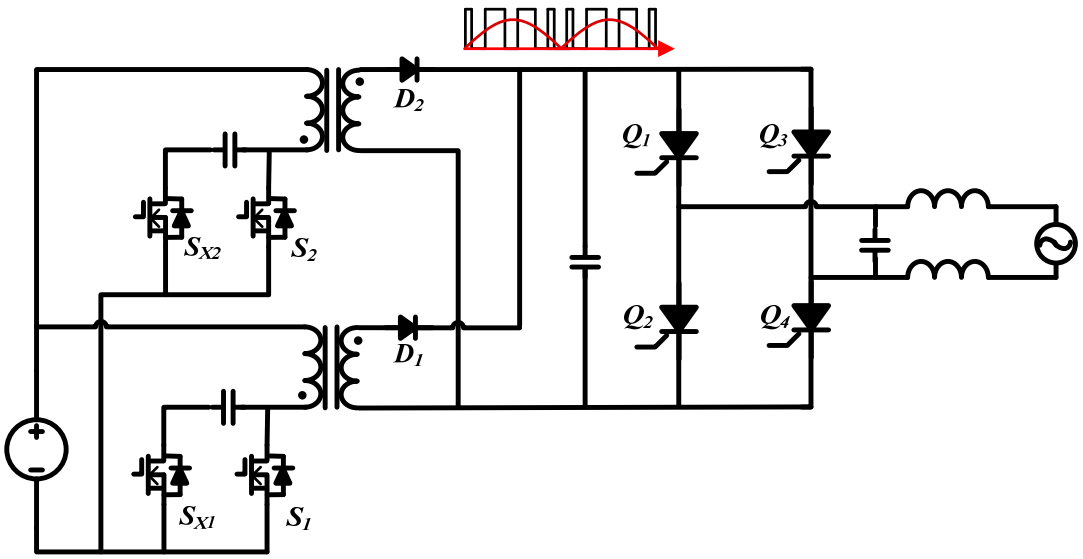


Figure 2.1 Enphase micro–inverter

In Figure 2.1, the interleaved flyback converters serve as single-stage power conversion. S_{x1} and S_{x2} are auxiliary switches for active snubber. Q_1, Q_2, Q_3, and Q_4 are thyristors, which serve as polarity selection switches.

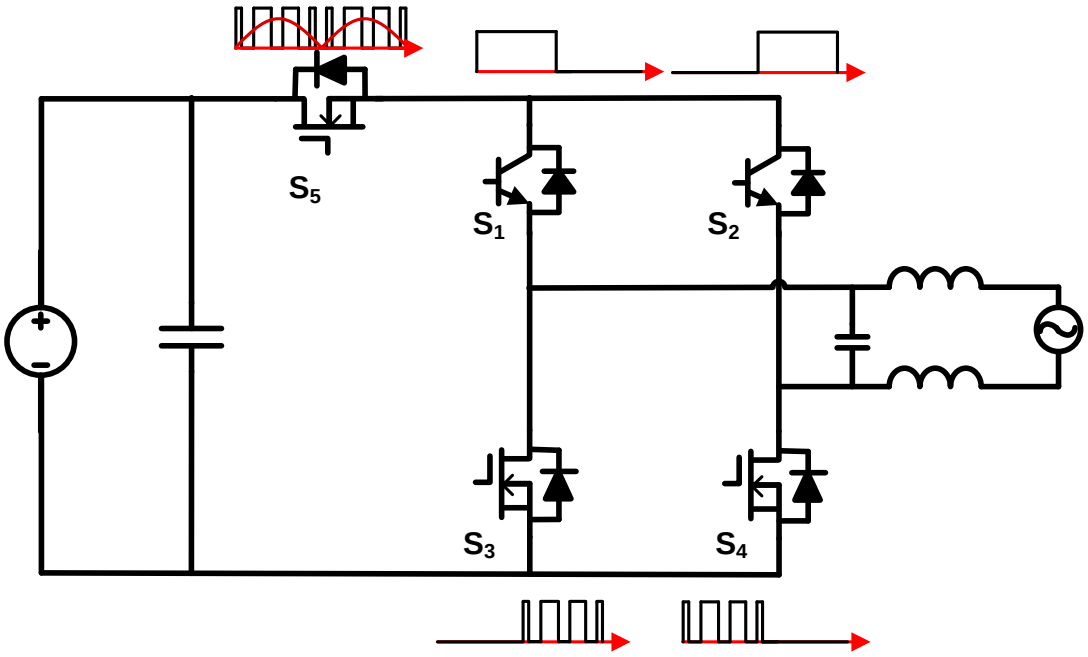


Figure 2.2 SMA H5^{TM} inverter [38].

In Figure 2.2, buck switch S_5 produces rectified SPWM. IGBT's S_1 and S_2 serve as low frequency selection network. MOSFET S_3 operates in SPWM on negative cycle. MOSFET S_4 operates in SPWM on positive cycle. Use fast recovery diode for S_1 and S_2 to reduce reverse recovery loss. S_5 and S_3 or S_4 share half the DC bus voltage, allowing low-voltage switches to be used in high voltage input. Other than high efficiency, the most advantage of this inverter is it has no leakage current, which is important for PV application. The drawback of this inverter is that the input voltage of it should be higher than the peak of the grid voltage, which limits the input voltage range for a PV inverter.

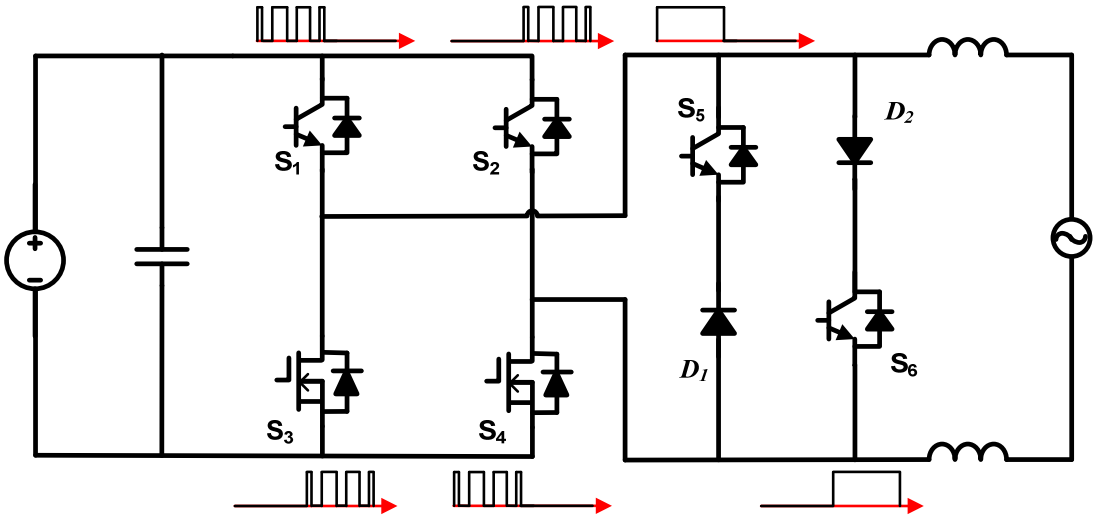


Figure 2.3 Highly efficient and reliable concept (HERIC) inverter.

Similar as H5^{TM}'s concept, the diagonal switches (S_1 – S_4) and (S_2 – S_3) pairs switch alternatively during positive and negative line cycles. Auxiliary switches (S_5 and S_6) turn on during zero states or freewheeling period and turn off during powering states, so only the auxiliary diodes need to be ultrafast reverse recovery, but the main diodes can be slow one. It should have even higher efficiency than H5^{TM} because of only two switches in series during on time. And it doesn't introduce leakage current either.

For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage requires being higher than the peak of the grid voltage, which is not good for PV application because the PV panel's *I-V* characteristics changes all the time.

2.1.2 Energy Storage in Single Stage PV Inverters

2.1.2.1 Capacitance Calculation

Figure 2.4 illustrates the relationship between the input power and output power for a single phase PV inverter. Because of the power difference, the single phase inverters always need energy storage to balance the instantaneous energy between input and output. Since single stage inverter only has one power processing stage, this energy storage need to be placed in the front of the inverter as shown in Figure 2.5.

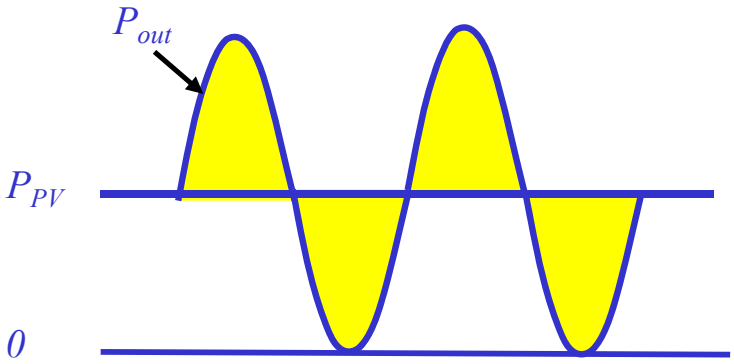


Figure 2.4 Input power and output power for a single phase PV inverter.

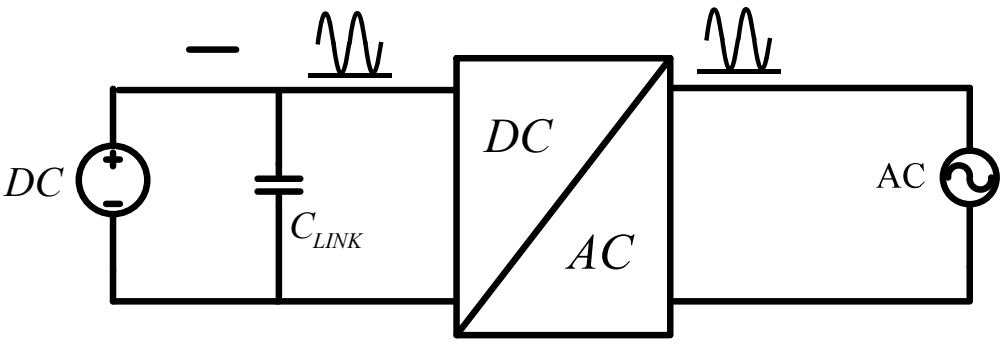


Figure 2.5 Single stage inverter.

For a grid-tied PV inverter, it is required to have unity power factor by standards [14] . In order to achieve unit power factor, the output current and voltage should have the same phase. Thus, the output power can be expressed as in (2.1).

$$p_{out}(t) = \sqrt{2}V_{grid} \cdot \sin(\omega_{grid} \cdot t) \cdot \sqrt{2}\frac{P_{PV}}{V_{grid}} \sin(\omega_{grid} \cdot t) \tag{2.1}$$

Where $P_{out}(t)$ is the instantaneous power; P_{PV} is the dc power from the input PV panels; V_{grid} is the grid's rms voltage. Thus, the output power could be simplified as in (2.2).

$$p_{out}(t) = 2P_{PV} \cdot \sin^2(\omega_{grid} \cdot t) = P_{PV} - P_{PV} \cdot \cos(2\omega_{grid} \cdot t) \tag{2.2}$$

Then the energy stored at the capacitor can be calculated as below:

$$\int [p_{out}(t) - P_{PV}] \cdot dt = \frac{1}{2}C \cdot u_{C\max}^2 - \frac{1}{2}C \cdot u_{C\min}^2 \tag{2.3}$$

Thus, the capacitance can be obtained as below:

$$C = \frac{P_{PV}}{\omega_{grid} \cdot u_C \cdot \Delta u_C} \tag{2.4}$$

Take the commercial Sunnyboy 8000TL-US grid-tied PV inverter for example. For this inverter, $P_{PV}=8000W$, $\omega_{grid}=60Hz$, $U_C=300V$ and $\Delta U_C=15V$. The required capacitance can be calculated as shown in (2.5).

$$C = \frac{P_{PV}}{\omega_{grid} \cdot U_C \cdot \Delta u_C} = \frac{8000}{2\pi \cdot 60 \cdot 300 \cdot 15} \approx 4500uF \tag{2.5}$$

Figure 2.6 shows the capacitors used for the Sunnyboy 8000TL-US PV inverter. Eighteen *1000μF* capacitors with *300 V* are used. 2 of them are connected in series for higher voltage stress and 9 of series are connected in parallel for higher capacitance.

Figure 2.6 The DC-link capacitors in the commercial product (300*V*, 18*1000*uF*).

2.1.2.2 Lifetime of Electrolytic Capacitor

Because the capacitor in this case requires large capacitance, electrolytic capacitors have been mostly chosen to decouple the power pulsation caused by single-phase power generation. The lifetime of an electrolytic capacitor is not long because the electrolytes in it evaporate. Thus, the lifetime of the inverter is shortened as well.

In order to analyze the electrolytic capacitor's lifetime, literature from many manufacturers [39]-[42] have been surveyed. It is found that different manufacturers estimate lifetimes for their products in different ways. However, the lifetime of electrolytic capacitors offered by every manufacturer has a strong relationship with the ambient temperature. The lifetime of the electrolytic capacitors from most manufacturers

does not change if smaller voltage is applied to them. Although the ripple current is the main reason of increasing core temperature, which decreases the lifetime, the maximum improvement we can make to the lifetime of the capacitors is to double the original lifetime by applying a smaller ripple current on the caps. The lifetime equations derived from the equations given by Nippon Chemi-Con and Nichicon are actually the same and can be arranged in (2.6).

$$L_n = L_O \cdot 2^{\frac{T_o - T}{10}} \cdot 2^{1-\left(\frac{I_a}{I_r}\right)^2} \qquad (2.6)$$

where L_n is the lifetime to be estimated and L_o is the base lifetime given in the datasheet. T_o is the actual ambient temperature in ˚C of the capacitor under which the base lifetime is tested, and T is the actual ambient temperature in ˚C. I_r is the specified maximum allowable ripple current (Arms) at an applied T_o, and I_a is the applied ripple current through the capacitor.

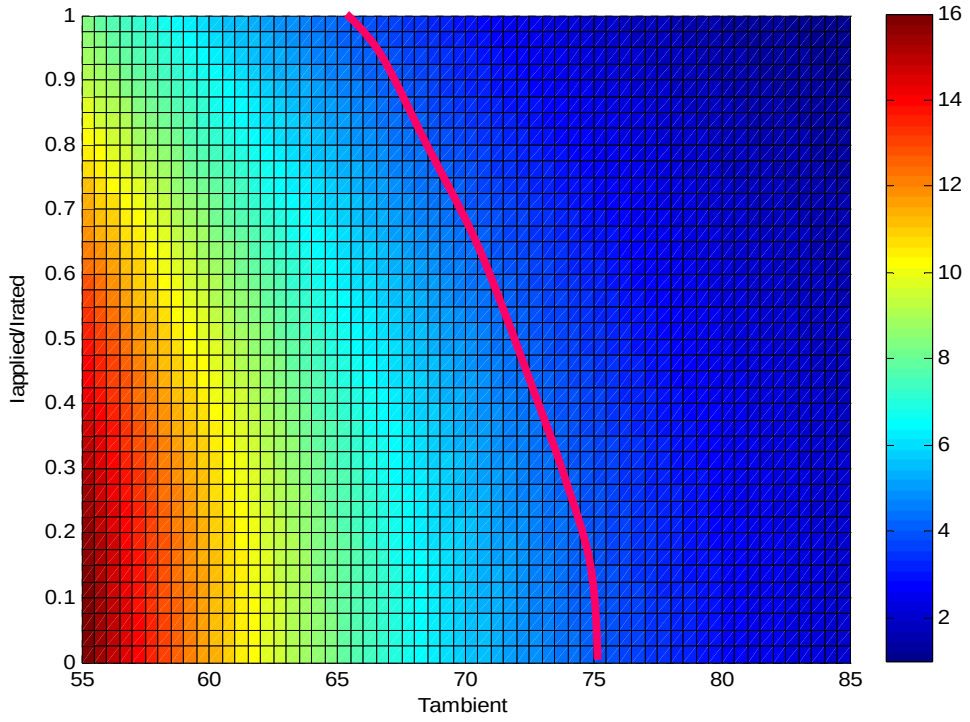


Figure 2.7 Lifetime multipliers of Nippon Chemi-Con and Nichicon vs. ambient temperature and ripple current ratio

The longest lifetime of capacitors in these two manufactures is 20,000 hours at 85˚C. The DOE's target of a twenty-year lifetime (by 2015) [43] can be calculated in hours by estimating that one PV inverter works 11 hours (7:00am-6:00pm) per day, then calculating that twenty years = 11×365×20 = 80300 hours. From Figure 2.7, it is known that it is needed to increase the current maximum lifetime of 20,000 hours fourfold in order to reach this long lifetime. Because reducing the ripple current can only extended the lifetime by two times at most, another factor, ambient temperature is important to keep further prolonging the capacitor lifetime. A very simple way to change the ambient temperature is by using a fan; however, a fan also has a limited lifetime, and the fan

creates noise (sound and electrical). Thus, the power electronics industry always tries to avoid using a fan for cooling.

It is found that Cornell Dubilier Electronics (CDE) has a specific equation of capacitor lifetime that includes a factor of the applied voltage.

$$L_n = L_O \cdot 2^{\frac{T_m - T_a}{10}} \cdot (4.3 - 3.3\frac{V_a}{V_r}) \tag{2.7}$$

where L_n is estimated lifetime and L_o is the base lifetime given in the datasheet. T_m is the maximum permitted internal operating temperature in ˚C, and is the temperature at which the base lifetime is tested; and T_a is the actual capacitor internal operating temperature in ˚C. V_r is the rated voltage and V_a is the applied voltage across the capacitor. The longest lifetime we can find for a CDE product is 10,000 hours at 105˚C. Here we should pay attention to the fact that 105˚C is the internal temperature and not the ambient temperature. If unlimited capacitors are used in series, the maximum multiplier of the lifetime can reach 4.3; even so, the maximum lifetime is only 43,000 hours, which is only slightly more than half of our target 80,300 hours (shown in Figure 2.8). In addition, with capacitors in series, additional capacitors will be used in parallel to obtain the same capacitance. This would lead to a great cost and requires more space. Thus, lowering the temperature is also the most important factor to improve the lifetime of CDE products; however, this raises the same issues as we have discussed for Nippon Chemi-Con and Nichicon products.

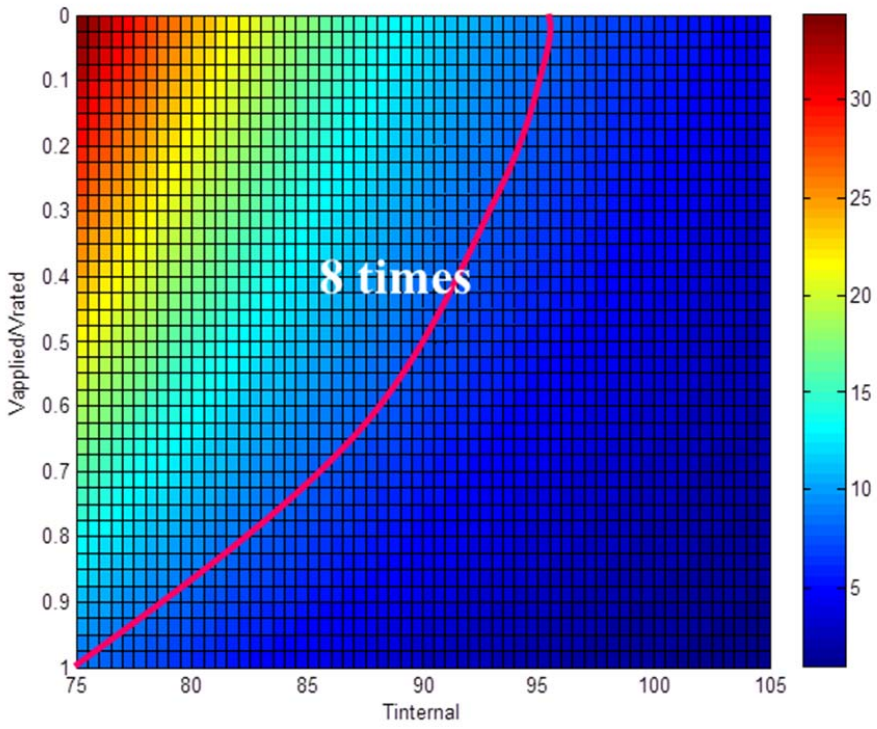


Figure 2.8 Lifetime multipliers of CDE vs. ambient temperature and ripple current ratio

Moreover, the end of life of the capacitor doesn't mean all the electrolytes in it evaporate. It is defined when one or more of the capacitor parameters have changed by a given amount, e.g. [44]:

- ΔC = 15% for V_r <=160 VDC.
- ΔC = 10% for V_r >160 VDC.
- *ESR* >= 2 times the initial value.
- *DF (tanδ)* >= 1.3 times the rated value.
- I_L >= the rated value.

Where ΔC is the change in capacitance; V_r is the rated voltage; *ESR* refers to equivalent series resistance; *DF* is dissipation factor and I_L is the leakage current.

When the electrolytic capacitor reaches its lifetime, it only means the parameters with it have been changed but not mean it is not working at all. Normally, many manufactures define that if the capacitor reaches its end of life when its capacitance is smaller than 80% of its initial value. Thus, the electrolytic capacitor can work much longer than its lifetime. Therefore it is possible to reach our target of 80,300 hours by using electrolytic capacitors.

Many researches are conducted on long lifetime PV inverter [45]-[49]. The principle of them is adding an auxiliary circuit for decoupling the energy and make use of film capacitor or other type of capacitor with smaller capacitance and longer lifetime.

2.1.3 MPPT Efficiency

For the single stage PV inverter, the energy storage capacitors are required to keep the voltage out from the PV panels with small fluctuation in order to get maximum output power from the PV panels. Because of the voltage fluctuation, the power obtained from PV panel is also fluctuated. The MPPT efficiency can be defined as (2.8) [50].

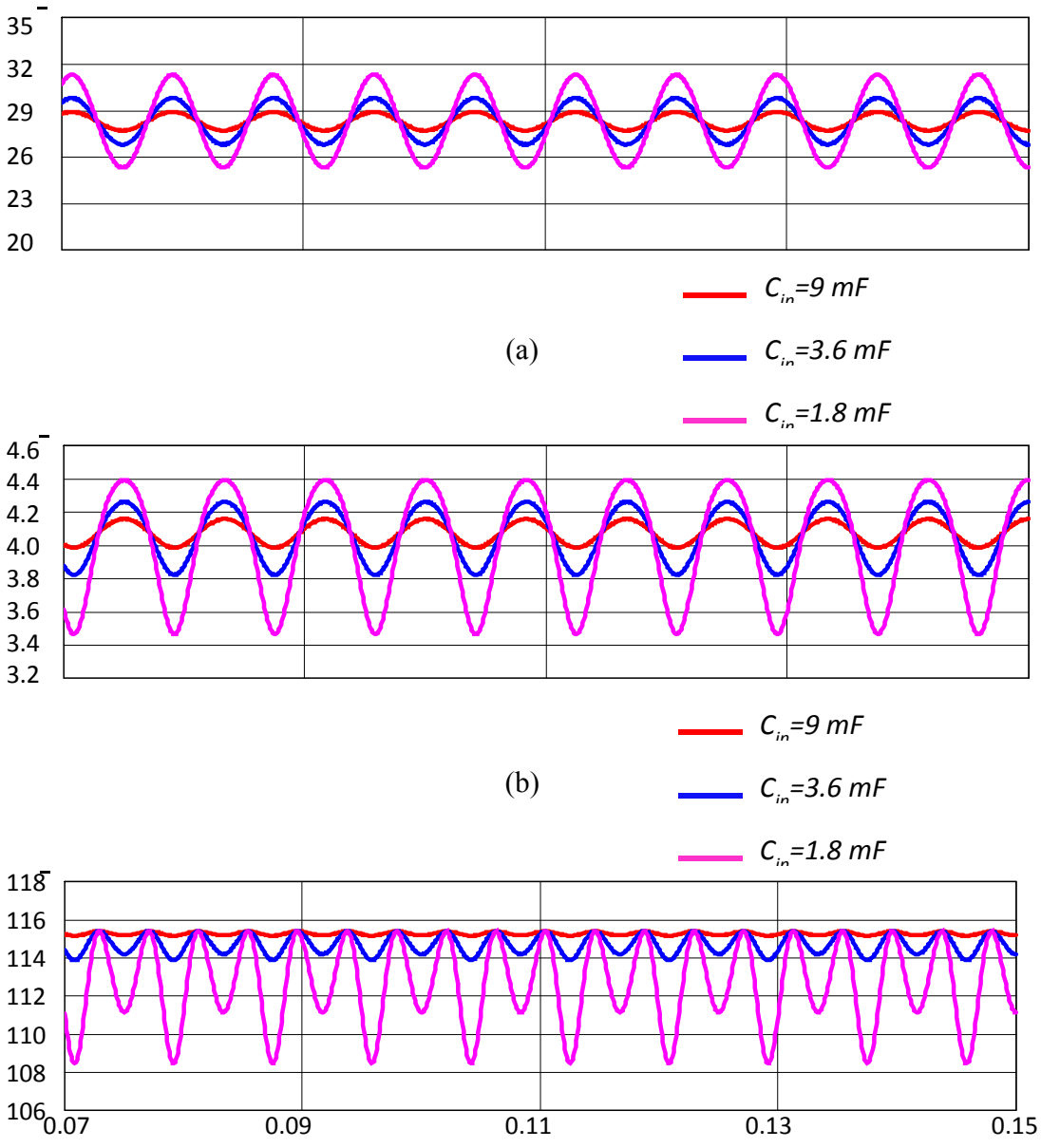
$$\eta_{MPPT} = \frac{\frac{\int_0^T P_{in}(t)\,dt}{T}}{P_{MPP}} \tag{2.8}$$

The relationship between PV panels' current and voltage could be expressed as (1.3).

$$U_{in} = U_{mpp} - \Delta u \cdot \cos(2\omega t) \tag{2.9}$$

$$\Delta u = \frac{P}{2\omega \cdot U_{mpp} \cdot C_{in}} \tag{2.10}$$

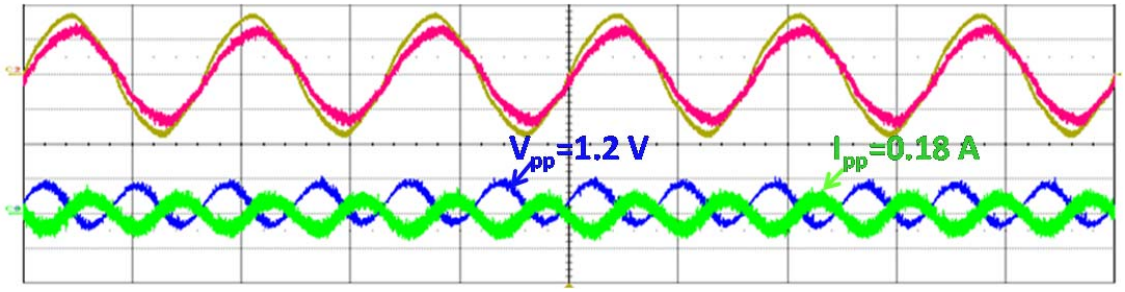
Based on (2.8) through (2.10), take a single stage micro-inverter for example, the pulsating power with different input capacitor could be illustrated in Figure 2.9.



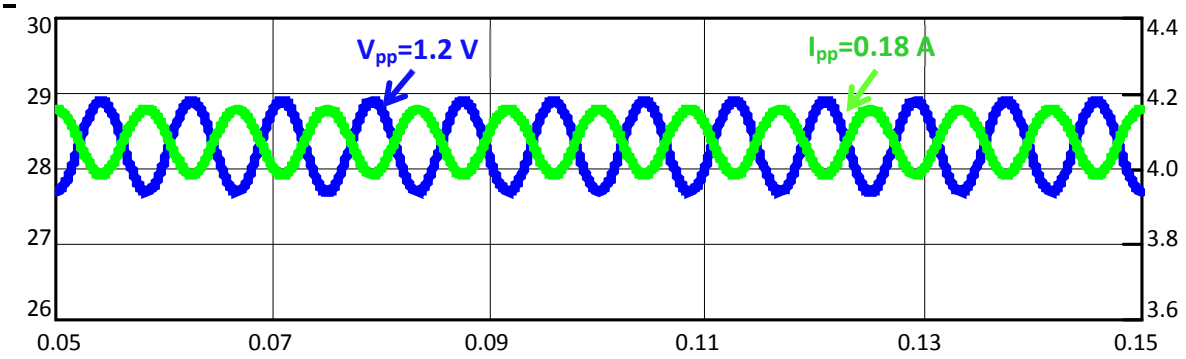
(c)

Figure 2.9 Different C_{in}'s impact on: (a) V_{in} ; (b) I_{in} ; (c) P_{in}.

It could be observed that the smaller input capacitance introduce more pulsating input voltage, input current and input power. Figure 2.10 and Figure 2.11 show the experimental results obtained from a commercial micro-inverter product and the analytical results with different energy storage capacitance. The analytical results match with experimental results very well.

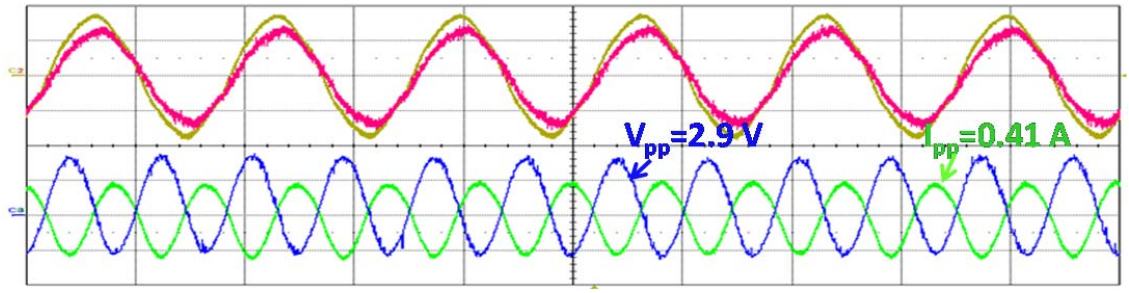


(a)

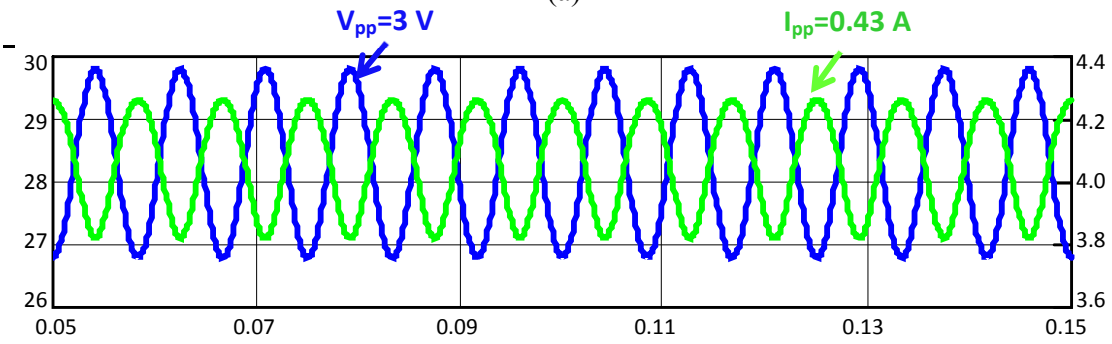


(b)

Figure 2.10 Experimental Vs. analytical results with C_{in} = 9 mF: (a) experimental; (b) analytical.



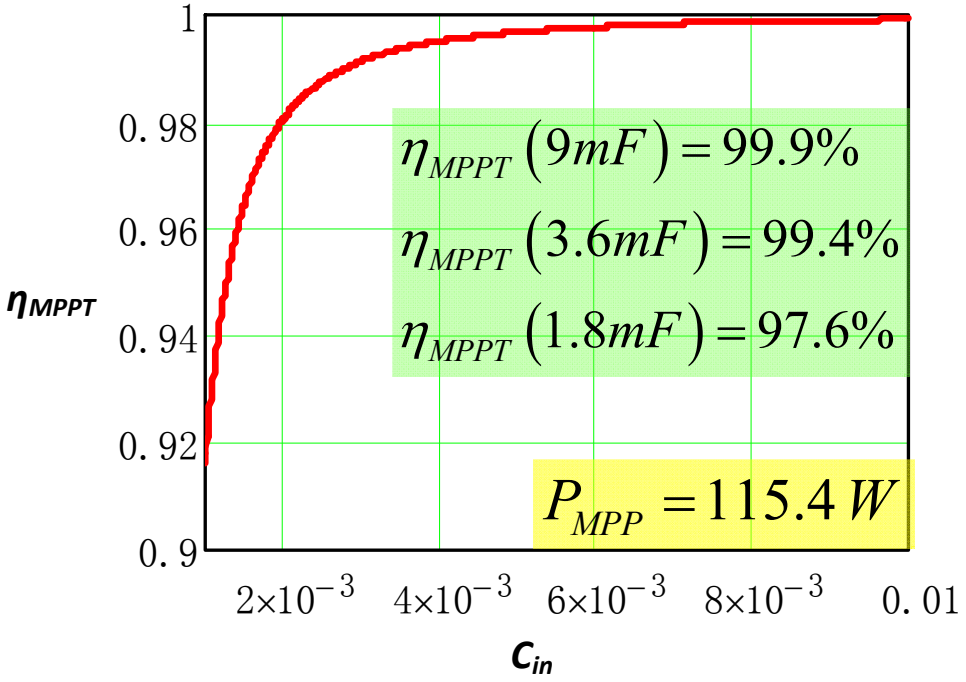
(a)



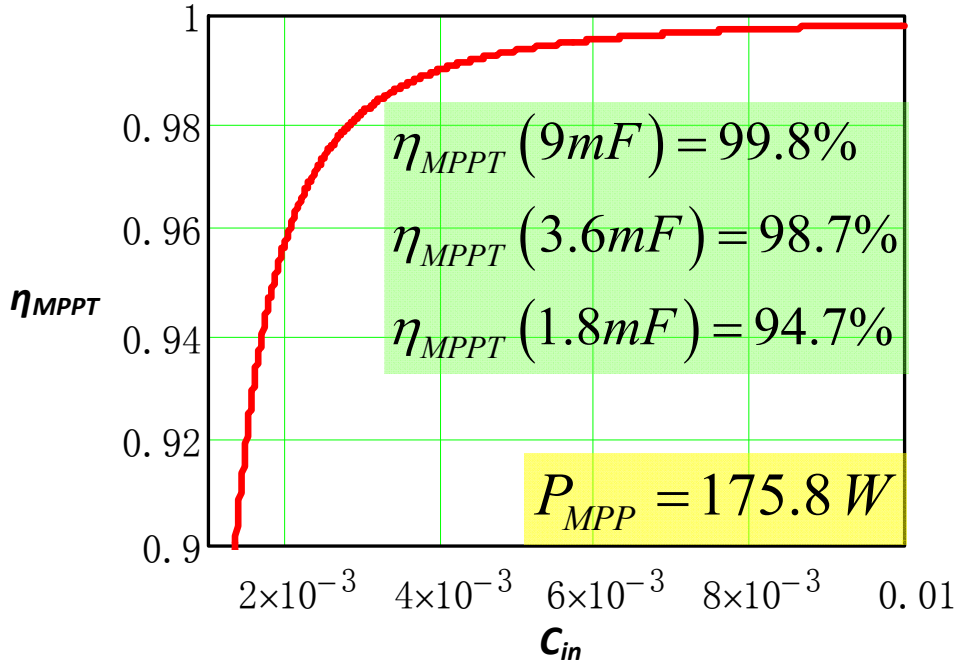
(b)

Figure 2.11 Experimental Vs. analytical results with C_{in} = *3.6 mF*: (a) experimental; (b) analytical.

Because different input energy storage capacitances introduce different input pulsating power, the MPPT efficiency changes with the input capacitances. For this micro-inverter, their relationship is shown in Figure 2.12.



(a)



(b)

Figure 2.12 MPPT efficiency Vs. C_{in} *under different power condition*: (a)P_{MPP} = *115W*; (b) P_{MPP} = *176W*;.

From the figure, it is known that less input capacitance leads to smaller MPPT efficiency and the MPPT efficiency drops more in strong irradiation case because the current is more pulsating. Different PV panel will have different MPPT efficiency curve based on its different I-V characteristics.

As time goes on, the capacitance of electrolytic capacitor will be reduced. If the capacitance is reduced a lot, the input power will be more pulsating, which reduces the MPPT efficiency and the whole system's efficiency will be lower as well.

2.2 Proposed Boost-Buck Converter Based PV Inverter

2.2.1 Boost-Buck Converter Based PV Inverter Topology

A boost-buck type dc-dc converter is proposed as the first stage with regulated output inductor current, and a full-bridge unfolding circuit with 50- or 60-Hz line frequency is applied to the dc-ac stage, which will unfold the rectified sinusoid current regulated by the dc-ac stage into a pure sinusoidal current, as shown in Figure 2.13. Since the circuit runs either in boost or buck mode, its first stage can be very efficient if the low conduction voltage drop power MOSFET and ultra-fast reverse recovery diode are used. For the second stage, because the unfolding circuit only operates at the line frequency and switches at zero voltage and current, the switching loss can be omitted. The only loss is due to the conduction voltage drop, which can be minimized with the use of low on-drop power devices, such as thyristor or slow-speed IGBT. In this version, IGBT is used in the unfolding circuit because it can be easily turned on and off with gating control.

Since only the boost dc-dc converter or buck dc-dc converter operates with high frequency switching all the time in the proposed system, the efficiency is improved [51]. And because there is only one high frequency power processing stage in this complete PCS, the reliability can be greatly enhanced [52]. Other than these, the analysis of middle capacitor and CCM/DCM operation condition is also presented.

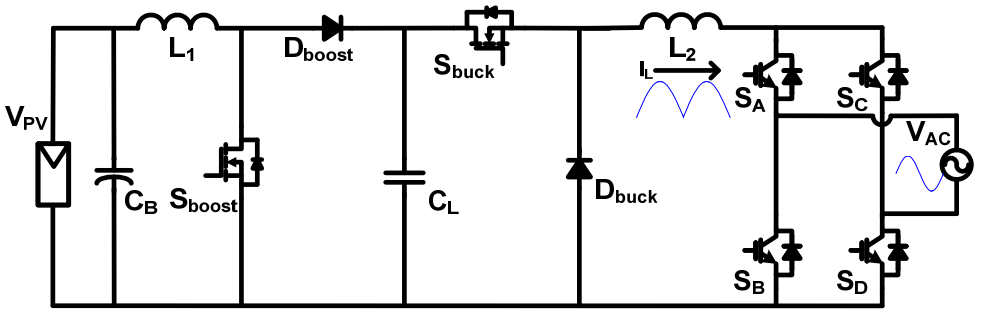


Figure 2.13 Boost-buck based PV inverter.

2.2.2 Operation Principle

A. *Boost Mode*

When the PV panel's voltage is lower than the instantaneous grid voltage, it will operate in boost mode, in which, S_{boost} will be switched on and off and S_{buck} will be always on, and the buck part of the circuit will act as an output filter as shown in Figure 2.14.

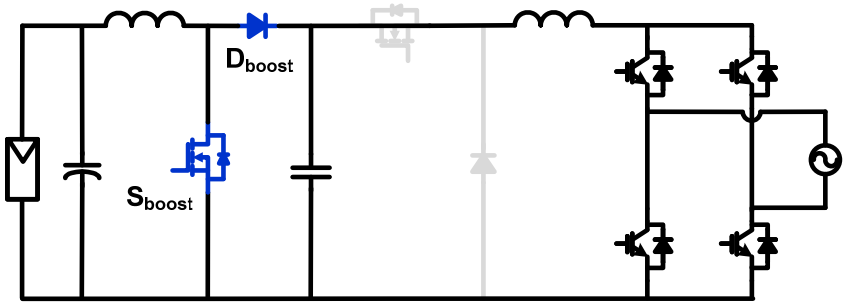


Figure 2.14 Boost mode.

In this mode, the duty cycle of S_{boost} can be found as

$$D_{boost} = 1 - \frac{V_{in}}{V_o} \tag{2.11}$$

Where $200 \le V_{in} \le 340$ and $V_o = 340 \sin \omega t$, then it is easy to get

$$0 \le D_{boost} \le 1 - \frac{V_{in}}{340} \tag{2.12}$$

B. *Buck Mode*

When the PV panel's voltage is higher than the instantaneous grid voltage, it will operate in buck mode, in which, S_{buck} will be switched on and off and S_{boost} will be always off, and the boost part of the circuit will act as an input filter as shown in Figure 2.15.

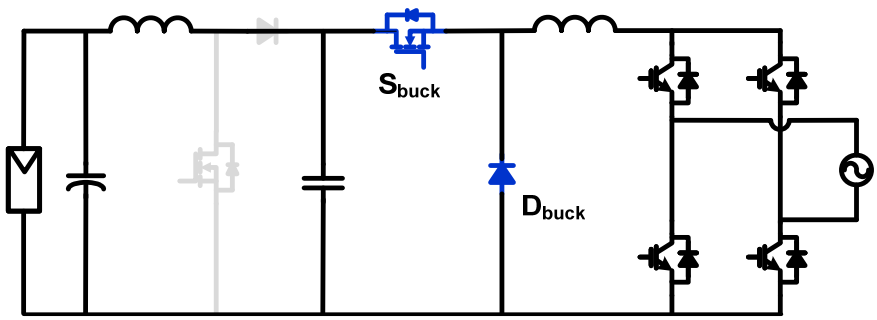


Figure 2.15 Buck mode.

In this mode, the duty cycle of S_{buck} can be found as

$$D_{buck} = \frac{V_o}{V_{in}} \tag{2.13}$$

Where $200 \le V_{in} \le 500$ and $V_o = 340 \sin \omega t$, then it is easy to get

If $340 \le V_{in} \le 500$, then

$$0 \le D_{buck} \le \frac{340}{V_{in}} \tag{2.14}$$

If $200 \le V_{in} \le 340$, then

$$0 \le D_{buck} \le 1 \tag{2.15}$$

Thus, if the PV panel's voltage is lower than the grid's peak voltage, the PV inverter will switch between buck mode and boost mode depending on the instantaneous grid voltage as shown in Figure 2.16. However, if the PV panel's voltage is higher than the grid's peak voltage, it will always run at buck mode. Instead of a dc bus in the middle, the voltage across the capacitor C_L in boost/buck PV inverter varies with the grid, if PV panel's voltage is lower than the grid's peak voltage as shown in Figure 2.17. However, if PV panel's voltage is higher than grid's peak voltage, C_L's voltage will be the same as PV panel's voltage.

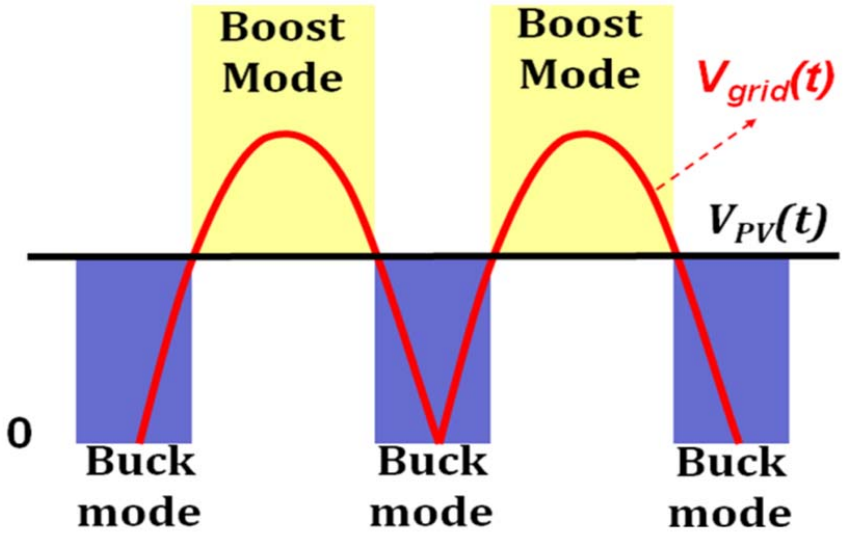


Figure 2.16 Operation mode.

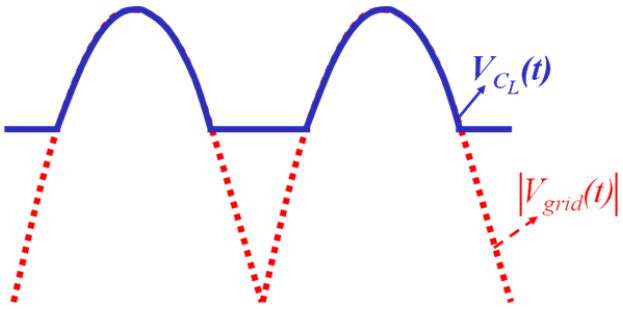


Figure 2.17 Capacitor C_L's voltage.

2.2.3 Passive Components Design

2.2.3.1 Capacitor Design

Based on the energy storage the input capacitance could be calculated as (2.16).

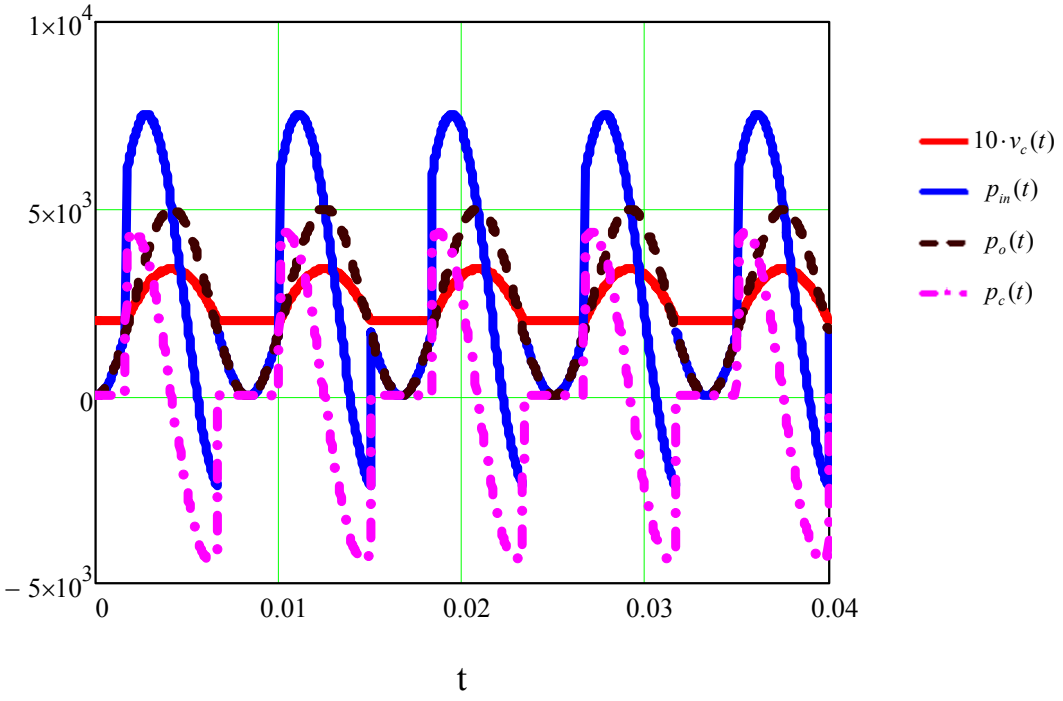
$$C_B = \frac{P_{PV}}{\omega_{grid} \cdot U_C \cdot \Delta u_C} = \frac{2500}{2\pi \cdot 60 \cdot 200 \cdot 16} \approx 2000uF \qquad (2.16)$$

The middle capacitor C_L impacts Q factor and double-pole frequency. Large C_L leads to small Q but low frequency double-pole, which is analyzed in 3.2. And also from the power decoupling point of view, as shown in Figure 2.18, large C_L also leads to large pulsating input power that means large C_{in} is needed to decouple the power, which is not expected. In our case, *2 μF* is chosen for C_L.

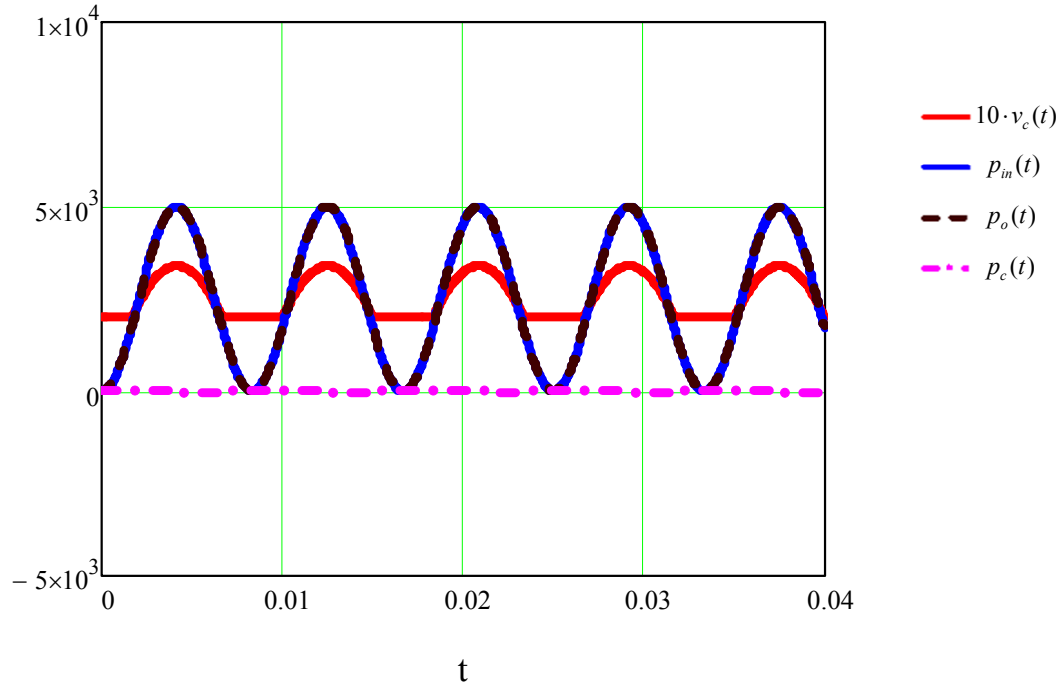
$$p_o(t) = v_o(t) \cdot i_{L_2}(t) = V_o \sin \omega t \cdot I_{L_2} \sin \omega t = V_o \cdot I_{L_2} \frac{1 - \cos 2\omega t}{2} \tag{2.17}$$

$$p_c(t) = C_L \frac{dv_c(t)}{dt} \cdot v_c(t) = \begin{cases} C_L \dfrac{d\left(V_o \sqrt{\dfrac{1-\cos 2\omega t}{2}} \right)}{dt} \cdot V_o \sqrt{\dfrac{1-\cos 2\omega t}{2}} & if\ V_{PV} < v_o(t) \\ C_L \dfrac{dV_{PV}}{dt} \cdot V_{PV} = 0 & if\ V_{PV} > v_o(t) \end{cases} \tag{2.18}$$

$$p_{in}(t) = p_c(t) + p_o(t) = \begin{cases} C_L \dfrac{d\left(V_o \sqrt{\dfrac{1-\cos 2\omega t}{2}} \right)}{dt} \cdot V_o \sqrt{\dfrac{1-\cos 2\omega t}{2}} + V_o \cdot I_{L_2} \dfrac{1-\cos 2\omega t}{2} & if\ V_{PV} < v_o(t) \\ V_o \cdot I_{L_2} \dfrac{1-\cos 2\omega t}{2} & if\ V_{PV} > v_o(t) \end{cases} \tag{2.19}$$



(a)



(b)

Figure 2.18 Pulsating power on input, output and C_L: (a) C_L = *200 uF;* (b) C_L = *2 uF.*

2.2.3.2 Inductor Design

During the buck mode, the input current can be treated as the input filter's inductor's current, whose ripple is much reduced from the filtering effect. Thus the input inductor is designed based on the current ripple in boost mode.

$$\Delta i_1 = V_{in}\frac{\Delta T}{L_1} = V_{in}\frac{T\left(1-\frac{V_{in}}{v_o(t)}\right)}{L_1} = \frac{T}{L_1}\left(1-\frac{V_{in}}{v_o(t)}\right)V_{in} \tag{2.20}$$

Because $v_o(t) \le 340V$

$$\Delta i_1 \ge \frac{T}{L_1}\left(1-\frac{V_{in}}{340}\right)V_{in} = \frac{T}{L_1}\cdot\frac{-V_{in}^2+340V_{in}}{340} \tag{2.21}$$

And because $V_{in} \ge 200V$

$$\Delta i_{1\max} = 82.4\cdot\frac{T}{L_1} \tag{2.22}$$

Thus,

$$L_1 = 82.4\cdot\frac{T}{\Delta i_{1\max}} = 82.4\cdot\frac{1/50000}{50\%\times 17} \approx 200\mu H \tag{2.23}$$

Similarly, during the boost mode, the output current can be treated as the output filter's inductor's current, whose ripple is also much mitigated. Thus, the output inductor is also designed based on the current ripple in buck mode.

$$\Delta i_{L2} = V_{L_2}\frac{\Delta T}{L_2} = v_o(t)\frac{T(1-\frac{v_o(t)}{V_{in}})}{L_2} = \frac{T}{L_2}(1-\frac{v_o(t)}{V_{in}})v_o(t) \tag{2.24}$$

Because $V_{in} \le 500V$

$$\Delta i_{L2} \geq \frac{T}{L_2}(1-\frac{v_o(t)}{500})v_o(t) = \frac{T}{L_2}\frac{-v_o^2(t)+500v_o(t)}{500} \tag{2.25}$$

Thus,

$$\Delta i_{L2\max} = 125 \cdot \frac{T}{L_2} \tag{2.26}$$

Thus,

$$L_2 = 125 \cdot \frac{T}{\Delta i_{2\max}} = 125 \cdot \frac{1/50000}{14.7 \times 0.4} \approx 400\mu H \tag{2.27}$$

Table 2.1 lists the summary of every passive components parameter.

Table 2.1 Passive components parameter.

L_1	*200 μH*
L_2	*400 μH*
C_B	*2 mF*
C_L	*2 μF*

2.2.4 Boundary Mode Analysis

As mentioned before, during the buck mode, the input current can be treated as the input filter's inductor's current, whose ripple is much reduced from the filtering effect. Similarly, during the boost mode, the output current can be treated as the output filter's inductor's current, whose ripple is also much mitigated. Due to this dual filter effect, the DCM mode operation is very rare in the proposed circuit.

In fact, the circuit is always running in continuous current mode (CCM) for input current in buck mode and output current in boost mode. That also indicates that discontinuous current mode (DCM) or boundary mode can happen only in output current in buck mode and input current in boost mode. Then it can be analyzed as a normal buck and boost converter. The boundary condition can be derived based on the input current ripple for boost mode and output current ripple for buck mode as below:

$$\Delta I_{in} = \frac{1}{2} \cdot \frac{\Delta T}{L} \cdot V = \frac{1}{2} \cdot \frac{\frac{1}{f_{sw}} \cdot (1 - \frac{V_{in}}{V_o})}{L_{1a}} \cdot V_{in} = \frac{1}{20} \cdot \frac{V_{in} \cdot V_o - V_{in}^2}{V_o} \tag{2.28}$$

$$\Delta I_o = \frac{\Delta T}{L} \cdot V = \frac{\frac{1}{f_{sw}} \cdot (1 - \frac{V_o}{V_{in}})}{L_2} \cdot V_o = \frac{1}{20} \cdot \frac{V_{in} \cdot V_o - V_o^2}{V_{in}} \tag{2.29}$$

Based on the equations above, it is easy to derive that the maximum ripple of input current happens when $V_{in} = 200\,V$ and $V_o = 340\,V$, then $\Delta I_{in\_\max} = 4.12\,A$. And the maximum ripple of output current happens when $V_{in} = 500\,V$ and $V_o = 250\,V$, then $\Delta I_{o\_\max} = 6.25\,A$. Thus, the boundary power for different input voltage can be obtained shown in Figure 2.19 and Figure 2.20.

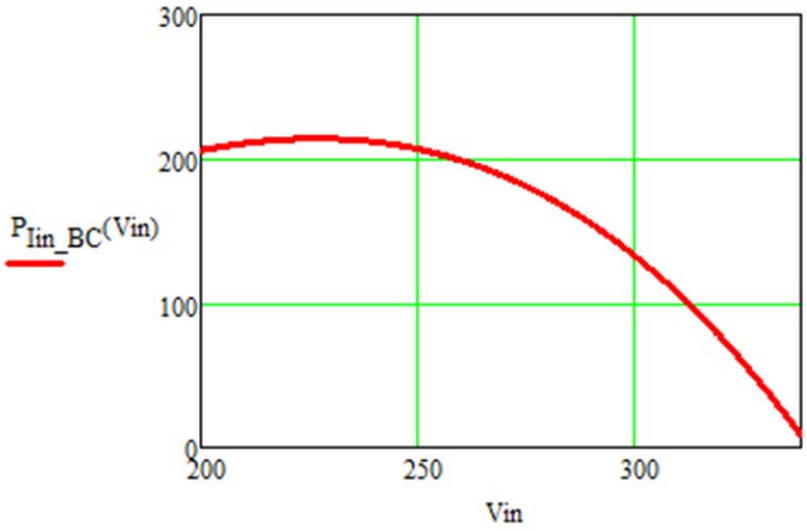


Figure 2.19 Boundary power condition for input current with different input voltage.

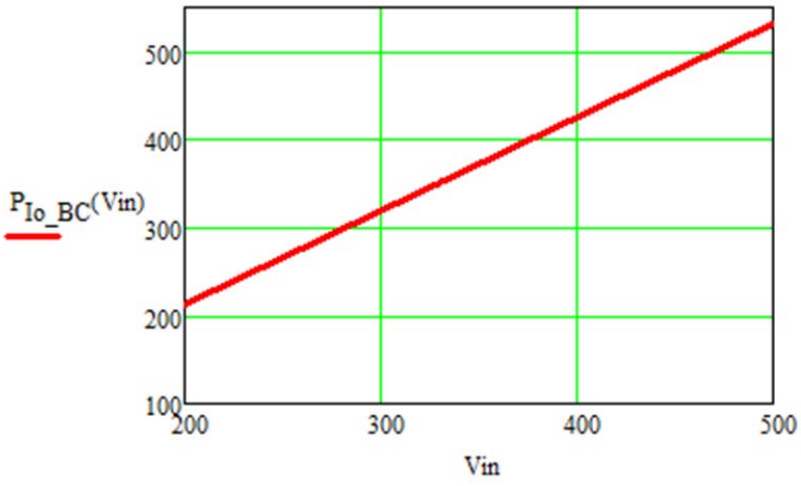


Figure 2.20 Boundary power condition for output current with different input voltage.

It is obviously noticed from Figure 2.19 and Figure 2.20 that the input current will go to DCM at very light power condition, which is even lower than 10% of the rated power. And the output current will go to DCM at light power condition as well, which is

lower than 20% of the rated power at most of the input voltage. If DCM is not desired, burst mode can be implemented at light power condition [53].

2.2.5 Leakage Current Analysis

[53] has reported that the capacitance between the point of contact and a single PV module has been calculated to range between 100 – 400 *pF*. The capacitance depends on weather conditions, and in the worst case as rainy days, the capacitance can be as high as 80 *nF/kW* [55]. Because of there is no isolation between the input and output without a transformer, the transformerless inverter needs to consider the leakage current issue as shown in Figure 2.21. The maximum current which can flow through the human body is 0.2 mA. And the German standard [56] lists the disconnection time for different levels of leakage currents as shown in Table 2.2.

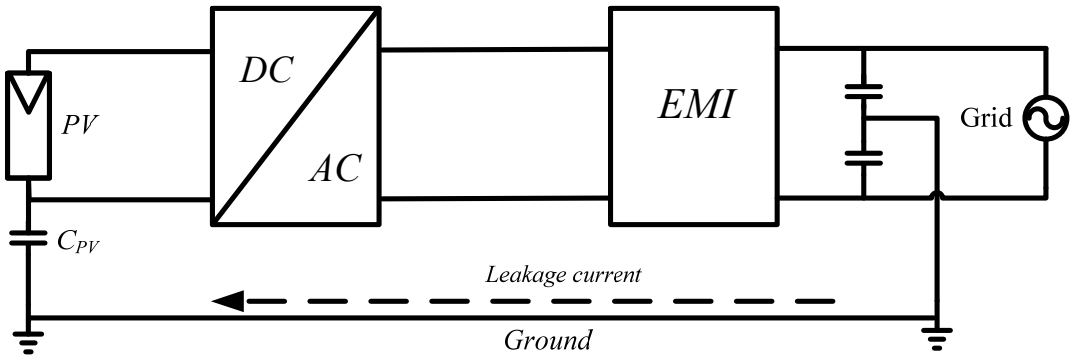


Figure 2.21 Leakage current in a PV transformerless trid-tied inverter system.

Table 2.2 Leakage current and corresponding disconnection time [56] .

RMS value of the leakage current (mA)	Disconnection time (s)
30	*0.3*
60	*0.15*
150	*0.04*

Because of this safety issue, the leakage current should be as small as possible for transformerless inverter. Many literatures [57]-[59] analyzed the leakage current in transformerless grid-connected inverter. For the proposed topology, the negative terminal "*O*" of solar modules is set as the reference point, and the middle points of the bridge legs are set as "*P*" and "*N*" for the output terminals as shown in Figure 2.22.

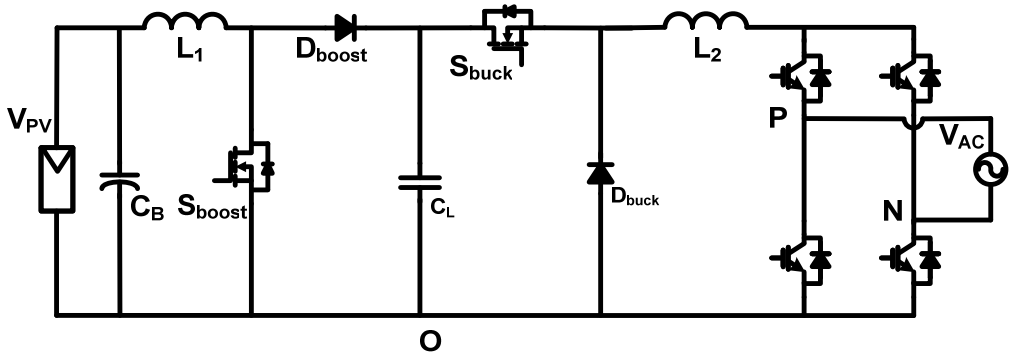


Figure 2.22 Boost-buck based PV inverter.

Then the instantaneous common-mode voltage v_{cm} can be calculated as

$$v_{cm} = \frac{(v_{PO} + v_{NO})}{2} \tag{2.30}$$

If v_{cm} is keeping constant all the time, the leakage current could be avoided [57]. For the proposed inverter, (2.31) can be obtained.

$$\begin{cases} v_{PO} = v_{grid} \quad v_{NO} = 0 \quad if\ v_{grid} > 0 \\ v_{PO} = 0 \quad v_{NO} = -v_{grid} \quad if\ v_{grid} < 0 \end{cases} \tag{2.31}$$

Thus,

$$v_{cm} = \frac{|v_{grid}|}{2} \tag{2.32}$$

Since v_{grid} is not constant but sinusoidal with 60 Hz, there is a small line frequency leakage current in the proposed inverter. For a 2.5 *kW* system, the capacitance between the PV modules and the ground C_{PV} would as high as 200 *nF*. The simulated leakage current in this extreme case is shown in Figure 2.23. It shows that even in this extreme case, the leakage current is still far below the standard.

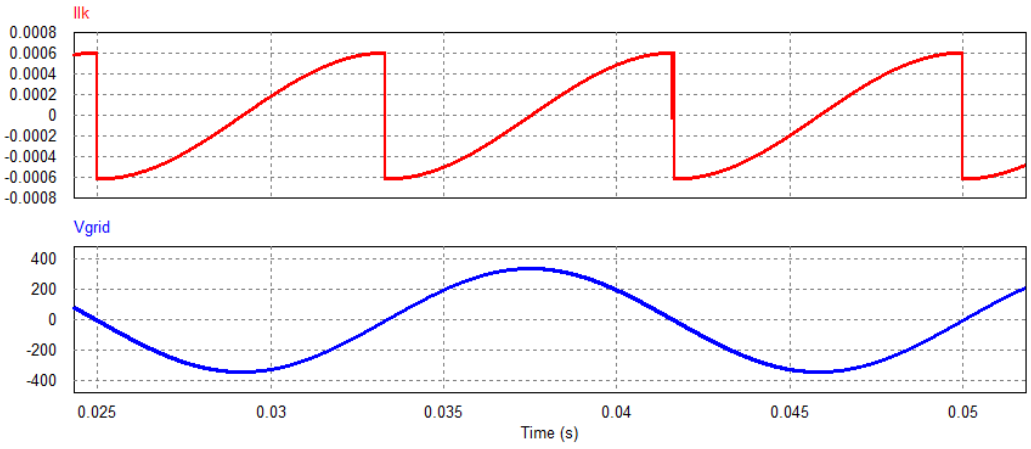


Figure 2.23 Leakage current with C_{PV} = 200 *nF*.

2.3 Summary

In this chapter, the state-of-the-art single stage PV inverters are reviewed firstly. For these single stage PV inverters, either a transformer is used for boosting the input voltage or the input voltage requires being higher than the peak of the grid voltage, which is not good for PV application because the PV panel's I-V characteristics changes all the time.

Following the topology review, the energy storage used in this type of inverter and its lifetime issue are discussed. Although the electrolytic capacitors have limited lifetime, it can still be used by applying smaller voltage and current ripple to prolong its lifetime. Because the end of its life doesn't mean its failure, the electrolytic capacitor can work much longer than its estimated lifetime. Moreover, the capacitance also has an impact on MPPT efficiency. The larger capacitance leads to higher MPPT efficiency.

After that a novel boost-buck converter based inverter has been presented. The first converter part operates in either boost or buck mode, which offers a wide input voltage range and presents a big advantage in PV inverter applications. The second inverter part is composed with unfolding circuit based on the direction of the grid. Thus from power processing point of view, this inverter is considered as a single stage inverter. Because it process power either as a buck converter or a boost converter, high efficiency can be achieved.

And then the analysis of its middle capacitor is presented. This capacitor is not used for energy storage. For power balance, if it is chosen large, the input energy storage capacitor needs to be large. Thus this middle capacitor is preferred to be small.

Other than those, CCM/DCM operation condition is also presented. For the current design, the input current will normally be in CCM for more than 10% rated power, and the output current will be always in CCM for more than 20% rated power.

Since the common-mode voltage in this inverter is equal to the grid voltage, it changes at line frequency. Thus the leakage current of it is small even at some extreme case.

Chapter 3:
Modeling and Control of Boost-Buck Converter Based PV Inverter

In previous chapter, a boost-buck converter based high efficiency PV inverter is proposed. In order to control it well, the modeling will be described in this chapter. After modeling the two modes separately, it can be derived that small L_1 and large L_2 are preferred because they help the controller design. Because of this, an interleaved-boost-cascaded-with-buck (IBCB) converter is proposed to increase the resonant pole frequency by the use of smaller boost inductor value. As a result, the control loop bandwidth can be pushed further up to enhance the robustness of the complete system and helps the system be controlled easier. The MPPT P&O algorithm is introduced in this chapter as well. The proposed circuit along with its controller has been designed, simulated, and tested with a hardware prototype. Finally, the results indicate that the efficiency of the proposed solution is up to 2% higher than the conventional solution under the same condition and its tested CEC efficiency is 97.4%.

3.1 Modeling of Boost-Buck Converter Based PV Inverter

In order to achieve unity power factor, the current of inductor L_2 needs to be controlled as a rectified sinusoidal shape. The pulse-width modulation (PWM) switch

models have been established for this PV inverter both in buck mode and boost mode with parasitic parameters considered.

3.1.1 Boost Mode Modeling

The PV panel is simplified as a DC voltage source and the grid with bridge switches are simplified as a rectified sinusoidal voltage source. Although the output voltage is rectified sinusoidal instead of constant output, it can also be treated as "steady-state", since the output voltage is changing with line frequency that is much smaller than switching frequency as shown in Figure 3.1. Under steady-state condition, the average model [61] of boost mode can be obtained as shown in Figure 3.2. Figure 3.3 shows their simplified model. Based on the model, its transfer functions can be obtained as follows.

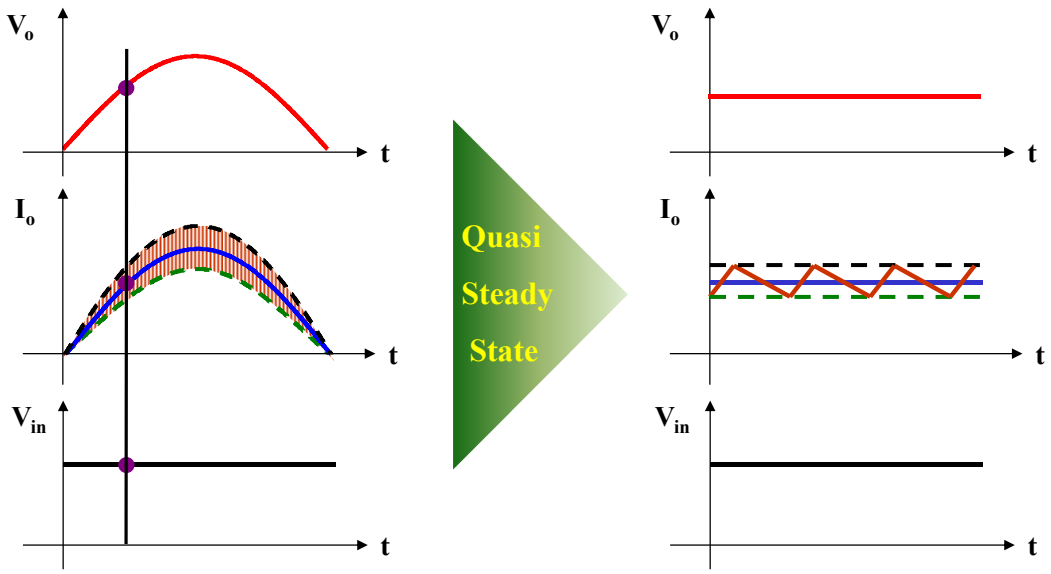


Figure 3.1 Quasi Steady State Concept.

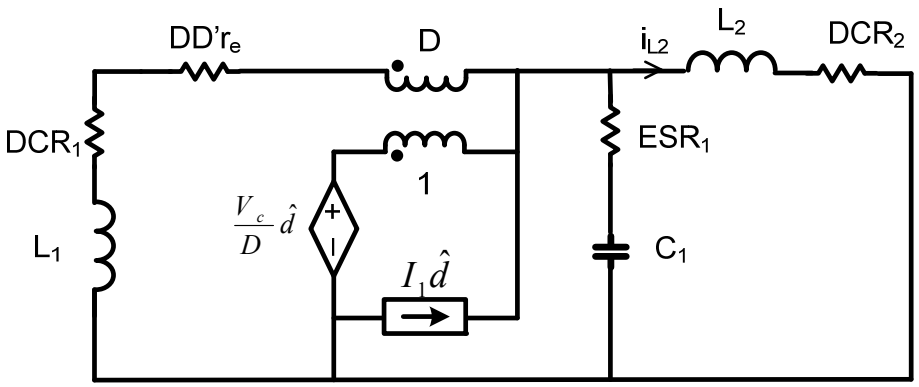


Figure 3.2 Model of boost mode.

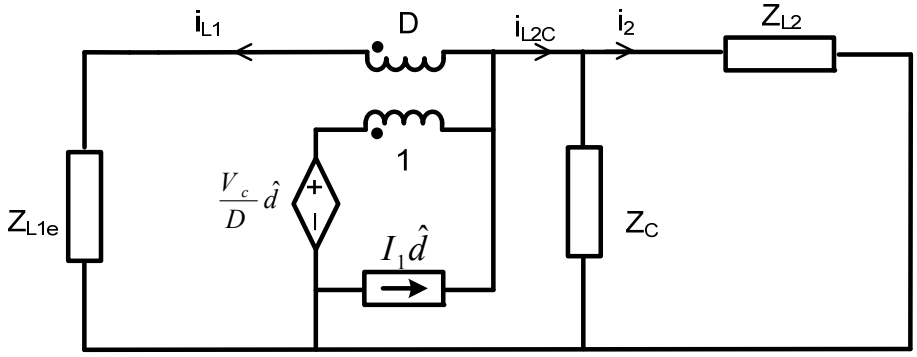


Figure 3.3 Simplified model of boost mode.

$$\begin{cases} \hat{i}_{L1} \cdot D + I_1 \hat{d} = \hat{i}_{L1} + \hat{i}_{L2C} \\ D(\frac{V_c}{D}\hat{d} - \hat{i}_{L2C} Z_{L2C}) + \hat{i}_{L2C} Z_{L2C} = \hat{i}_{L1} Z_{L1e} \end{cases} \tag{3.1}$$

where

$$\hat{i}_{L2} = \hat{i}_{L2C} \frac{Z_C}{Z_{L2} + Z_C} \tag{3.2}$$

$$Z_{L2C} = \frac{Z_C Z_{L2}}{Z_{L2} + Z_C} \tag{3.3}$$

$$I_1 = -I_{L1},\ V_c = -V_o \tag{3.4}$$

$$r_e = DCR_2 \| ESR_1 \tag{3.5}$$

where

$$\begin{cases} Z_{L_1 e} = \left(sL_1 + DCR_1 + D'Dr_e \right) \\ Z_C = \dfrac{1}{sC_1} + ESR_1 \\ Z_{L2} = sL_2 + DCR_2 \end{cases} \tag{3.6}$$

Thus,

$$Z_{L2C} = Z_C \| Z_{L2} = \frac{\left(\dfrac{1}{sC_1} + ESR_1 \right)\left(sL_2 + DCR_2 \right)}{\left(\dfrac{1}{sC_1} + ESR_1 \right) + \left(sL_2 + DCR_2 \right)} \tag{3.7}$$

Thus, G_{id_boost} can be derived as follow shown from (3.8) to (3.12).

$$\hat{i}_{L2} = \hat{i}_{L2C} \frac{Z_C}{Z_{L2} + Z_C} \Rightarrow G_{id} = \frac{\hat{i}_2}{\hat{d}} = \frac{\hat{i}_{L2C}}{\hat{d}} \cdot \frac{Z_C}{Z_{L2} + Z_C} \tag{3.8}$$

$$\hat{i}_{L1} \cdot D + I_1 \hat{d} = \hat{i}_{L1} + \hat{i}_{L2C} \Rightarrow \hat{i}_{L1} = \frac{I_1 \hat{d} - \hat{i}_{L2C}}{1 - D} \tag{3.9}$$

$$\begin{aligned} & D\left(\frac{V_c}{D}\hat{d} - \hat{i}_{L2C} Z_{L2C}\right) + \hat{i}_{L2C} Z_{L2C} = \frac{I_1 \hat{d} - \hat{i}_{L2C}}{1 - D} Z_{L1e} \\ & \Rightarrow V_c \hat{d} + \hat{i}_{L2C} Z_{L2C} (1 - D) = \frac{I_1 \hat{d}}{1 - D} Z_{L1e} - \frac{\hat{i}_{L2C}}{1 - D} Z_{L1e} \\ & \Rightarrow \hat{i}_{L2C} \left[Z_{L2C} (1 - D) + \frac{Z_{L1e}}{1 - D} \right] = \left(\frac{I_1 \cdot Z_{L1e}}{1 - D} - V_c \right) \hat{d} \\ & \Rightarrow \frac{\hat{i}_{L2C}}{\hat{d}} = \frac{\dfrac{I_1 \cdot Z_{L1e}}{1 - D} - V_c}{Z_{L2C}(1 - D) + \dfrac{Z_{L1e}}{1 - D}} = \frac{I_1 \cdot Z_{L1e} - V_c D'}{Z_{L2C} D'^2 + Z_{L1e}} = \frac{V_o D' - I_{L1} \cdot Z_{L1e}}{Z_{L2C} D'^2 + Z_{L1e}} \end{aligned} \tag{3.10}$$

$$G_{id\_boost} = \frac{\hat{i}_2}{\hat{d}} = \frac{\hat{i}_{L2C}}{\hat{d}} \cdot \frac{Z_C}{Z_{L2} + Z_C} = \frac{V_o D' - I_{L1} \cdot Z_{L1e}}{Z_{L2C} D'^2 + Z_{L1e}} \cdot \frac{Z_C}{Z_{L2} + Z_C} = \frac{V_o D' - I_{L1} \cdot Z_{L1e}}{\frac{Z_C Z_{L2}}{Z_{L2} + Z_C} D'^2 + Z_{L_1 e}} \cdot \frac{Z_C}{Z_{L2} + Z_C} \quad (3.11)$$

$$G_{id\_boost} = \frac{V_o D' - I_{L1} \cdot \left(sL_1 + DCR_1 + D'Dr_e\right)}{\frac{\left(\frac{1}{sC_1} + ESR_1\right)\left(sL_2 + DCR_2\right)}{\left(\frac{1}{sC_1} + ESR_1\right) + \left(sL_2 + DCR_2\right)} D'^2 + \left(sL_1 + DCR_1 + D'Dr_e\right)} \cdot \frac{\left(\frac{1}{sC_1} + ESR_1\right)}{\left(sL_2 + DCR_2\right) + \left(\frac{1}{sC_1} + ESR_1\right)}$$

$$= \frac{V_o D' - I_{L1} \cdot \left(sL_1 + DCR_1 + D'Dr_e\right)}{\left(\frac{1}{sC_1} + ESR_1\right)\left(sL_2 + DCR_2\right) D'^2 + \left(sL_1 + DCR_1 + D'Dr_e\right)\left[\left(sL_2 + DCR_2\right) + \left(\frac{1}{sC_1} + ESR_1\right)\right]} \cdot \left(\frac{1}{sC_1} + ESR_1\right)$$

$$= \frac{V_o D' - I_{L1} \cdot \left(sL_1 + DCR_1 + D'Dr_e\right)}{\left(1 + sC_1 ESR_1\right)\left(sL_2 + DCR_2\right) D'^2 + \left(sL_1 + DCR_1 + D'Dr_e\right)\left[\left(1 + sC_1 ESR_1\right) + \left(s^2 C_1 L_2 + sC_1 DCR_2\right)\right]} \cdot \left(1 + sC_1 ESR_1\right) \quad (3.12)$$

Thus, G_{id_boost} can be expressed as shown in (3.13).

$$G_{id\_boost} = \frac{-\left(sL_1 + DCR_1 + D'Dr_e\right) \cdot I_{L1} + V_o \cdot D'}{\left(1 + sC_1 ESR_1\right)\left(sL_2 + DCR_2\right) D'^2 + \left(sL_1 + DCR_1 + D'Dr_e\right)\left[\left(1 + sC_1 ESR_1\right) + \left(s^2 C_1 L_2 + sC_1 DCR_2\right)\right]} \cdot \left(1 + sC_1 ESR_1\right) \quad (3.13)$$

The simulation model for AC analysis of control - to - output inductor current has been built as shown in Figure 3.4. The Bode plot of its transfer function is extracted. The Bode plot data obtained from simulation is put into a Mathcad file and compared with that of derived averaged model in (3.13). In Figure 3.5, under condition $V_{in} = 200\ V$ and $V_o = 340\ V$, the blue dashed curve is from Simplis simulation model and the red solid one is obtained from mathematic model. It is noticed that at the switching frequency, both gain and phase have a little glitch in simulation result, whereas the derived model does not have. With exception at this switching frequency and its multiples, the simulated result matches that of the mathematic model very well. Thus, the mathematic model could be used for further analysis.

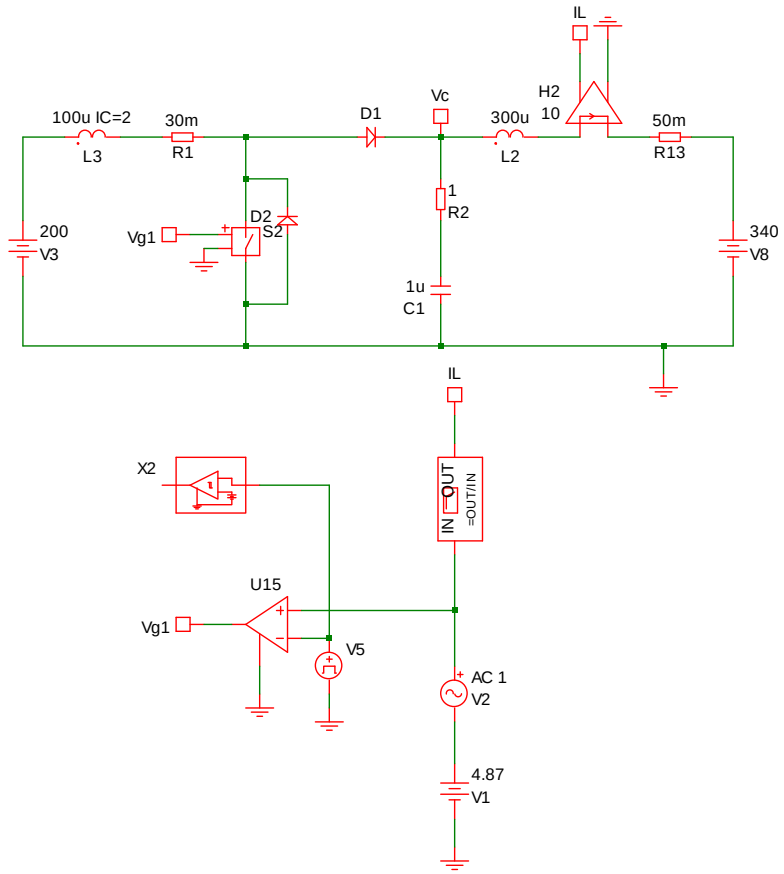


Figure 3.4 Boost mode simulation model in Simplis.

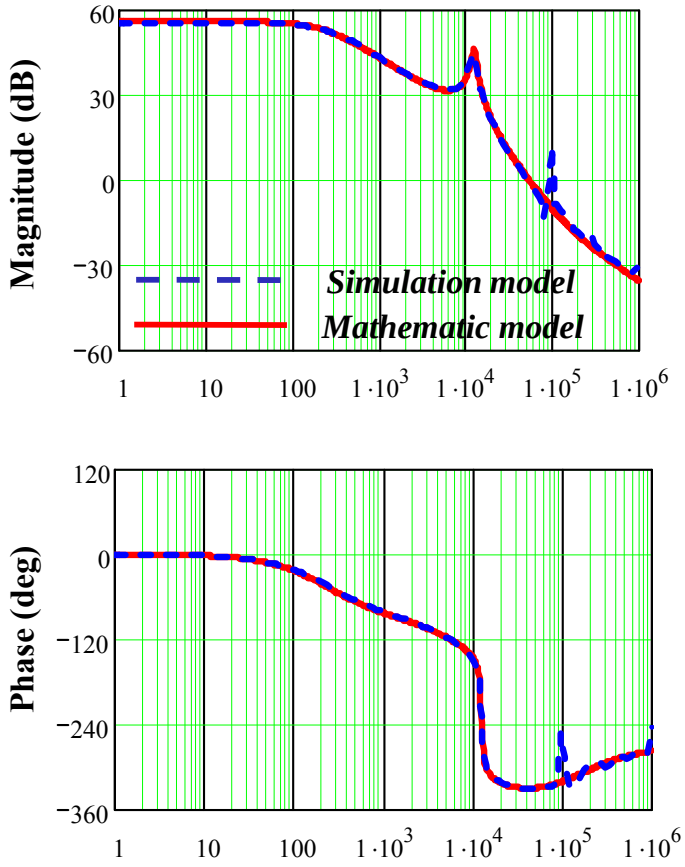


Figure 3.5 Comparison between mathematic model and Simplis simulation model.

Based on (3.13), when $f = 0$, DC gain could be obtained as

$$G_{id\_boost} = \frac{-\left(DCR_1 + D'Dr_e\right)\cdot I_{L1} + V_o \cdot D'}{DCR_2 \cdot D'^2 + DCR_1 + D'Dr_e} \approx \frac{V_{in}}{DCR_2 \cdot D'^2 + DCR_1 + D'Dr_e} \tag{3.14}$$

It could be easily found that the DC gain is related to input voltage V_{in}, duty cycle D and the parasitic resistance.

From its numerator's expression, it can be noticed that G_{id_boost} contains both right half plane (RHP) zero and left half plane (LHP) zero. In order to obtain its zeros position,

the numerator of G_{id_boost} needs to be zero. Therefore, the RHP zero could be obtained as shown in (3.15) and (3.16).

$$-\left(sL_1 + DCR_1 + D'Dr_e\right)\cdot I_{L1} + V_o \cdot D' = 0 \tag{3.15}$$

$$s = \frac{V_o \cdot D' / I_{L1} - \left(DCR_1 + D'Dr_e\right)}{L_1} = \frac{V_{in} / I_{L1} - \left(DCR_1 + D'Dr_e\right)}{L_1} \tag{3.16}$$

And the LHP zero can be obtained as shown in (3.17) and (3.18).

$$1 + sC_1ESR_1 = 0 \tag{3.17}$$

$$s = -\frac{1}{C_1ESR_1} \tag{3.18}$$

Thus it could be easily found that the RHP zero is related to voltage V_{in}, duty cycle D, inductors L_1, the current going through inductor L_1 and the parasitic resistance. The LHP zero is related to capacitor C_1 and its parasitic ESR_1.

In order to obtain the double - pole position, the numerator of G_{id_boost} needs to be zero as well.

$$\begin{aligned}&\left(1 + sC_1ESR_1\right)\left(sL_2 + DCR_2\right)D'^2 + \left(sL_1 + DCR_1 + D'Dr_e\right)\left[\left(1 + sC_1ESR_1\right) + \left(s^2C_1L_2 + sC_1DCR_2\right)\right] \\ &\approx sL_2D'^2 + sL_1\left(1 + s^2C_1L_2\right) = 0\end{aligned} \tag{3.19}$$

Thus, the double - pole position can be obtained as:

$$s = \pm\sqrt{\frac{L_2D'^2 + L_1}{C_1L_1L_2}}\,j \tag{3.20}$$

It could be easily found that the double - pole position is related to duty cycle D, two inductors L_1 and L_2 and capacitor C_1, especially C_1.

Similarly, single pole position can be obtained as shown in (3.21) and (3.22).

$$\begin{aligned}&\left(1+sC_1ESR_1\right)\left(sL_2+DCR_2\right)D'^2+\left(sL_1+DCR_1+D'Dr_e\right)\left[\left(1+sC_1ESR_1\right)+\left(s^2C_1L_2+sC_1DCR_2\right)\right]\\&\approx\left(sL_2+DCR_2\right)D'^2+\left(sL_1+DCR_1+D'Dr_e\right)=0\end{aligned} \tag{3.21}$$

$$s=-\frac{DCR_2\cdot D'^2+DCR_1+D'Dr_e}{L_2\cdot D'^2+L_1} \tag{3.22}$$

It can also be found that the single pole position is related to duty cycle D, two inductors L_1 and parasitic resistance.

Since there are double - pole and a single pole in G_{id_boost}, the denominator can be expressed as below:

$$\left(s^2+\frac{\omega_0}{Q}s+\omega_0^2\right)\left(s+s_p\right)=s^3+\left(\frac{\omega_0}{Q}+s_p\right)s^2+\left(\omega_0^2+\frac{\omega_0\cdot s_p}{Q}\right)s+\omega_0^2\cdot s_p \tag{3.23}$$

Then

$$\left.\begin{aligned}s_p&=\frac{DCR_2\cdot D'^2+DCR_1+D'Dr_e}{L_2\cdot D'^2+L_1}\\\omega_0^2\cdot s_p&=\frac{DCR_2\cdot D'^2+DCR_1+D'Dr_e}{C_1L_1L_2}\end{aligned}\right\}\Rightarrow\omega_0=\sqrt{\frac{L_2\cdot D'^2+L_1}{C_1L_1L_2}} \tag{3.24}$$

Thus,

$$\begin{aligned}&\frac{\omega_0}{Q}+s_p\\&=\frac{D'^2\,C_1ESR_1L_2+L_1C_1\left(ESR_1+DCR_2\right)+C_1L_2\left(DCR_1+D'Dr_e\right)}{C_1L_1L_2}\\&=\frac{D'^2\,ESR_1+DCR_1+D'Dr_e}{L_1}+\frac{ESR_1+DCR_2}{L_2}\end{aligned}\tag{3.25}$$

Thus, Q could be obtained as shown in (3.26).

$$Q=\frac{\sqrt{\frac{L_2\cdot D'^2+L_1}{C_1L_1L_2}}}{\frac{D'^2\,ESR_1+DCR_1+D'Dr_e}{L_1}+\frac{ESR_1+DCR_2}{L_2}-\frac{DCR_2\cdot D'^2+DCR_1+D'Dr_e}{L_2\cdot D'^2+L_1}}\tag{3.26}$$

Assume $ESR_1\gg DCR_1, ESR_1\gg DCR_2, and\ L_2>L_1$, then Q could be approximated as below:

$$Q\approx\frac{\sqrt{\frac{L_2\cdot D'^2+L_1}{C_1L_1L_2}}}{\frac{D'^2\,ESR_1}{L_1}}\tag{3.27}$$

$$Q\approx\frac{\sqrt{\frac{\left(L_2\cdot D'^2+L_1\right)L_1}{D'^4\,C_1L_2}}}{ESR_1}\tag{3.28}$$

From the expression of Q, it can be noticed that Q will change apparently with D, C_1, L_1, ESR_1 and L_2. And L_1 impacts Q more than L_2 and C_1. Since Q changes with D, Q will be always changing in the line cycle. The larger D and L_1 are, the larger Q will be. The larger C_1, ESR_1 and L_2 are, the smaller Q will be. Since $\frac{200}{340}\le D'\le 1$, the largest Q happens at $D'=\frac{200}{340}$.

3.1.2 Buck Mode Modeling

Similar to 3.1.1, under steady-state condition, the average model of buck mode can be obtained as shown in Figure 3.6 and Figure 3.7. Figure 3.8 shows their simplified model. Based on its model, its transfer functions can be obtained as follows.

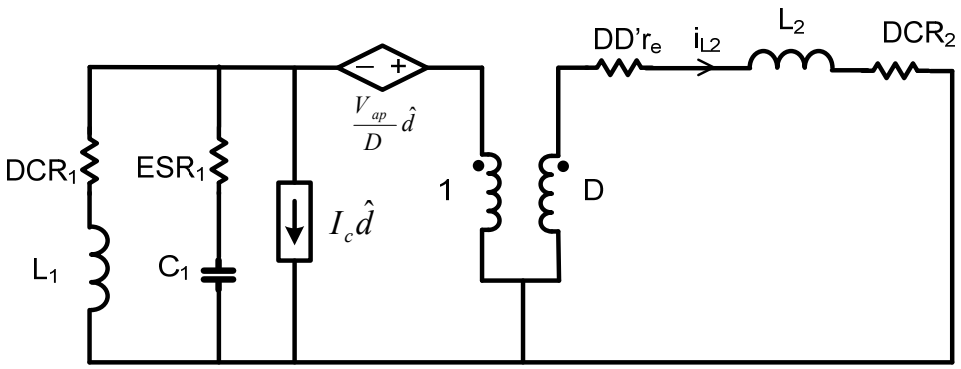


Figure 3.6 Model of buck mode.

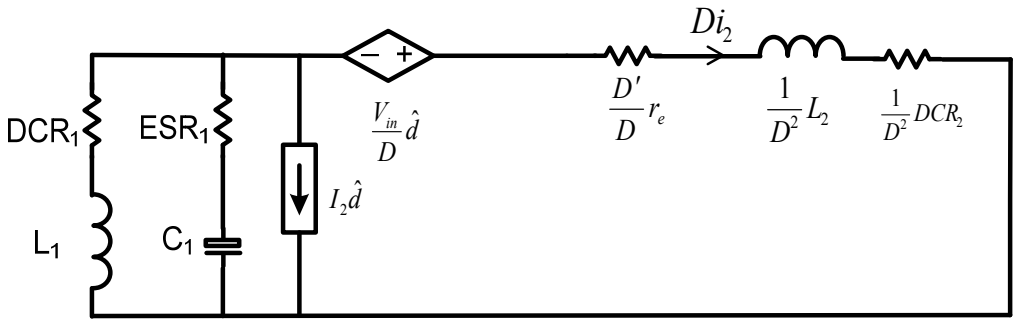


Figure 3.7 Model of buck mode.

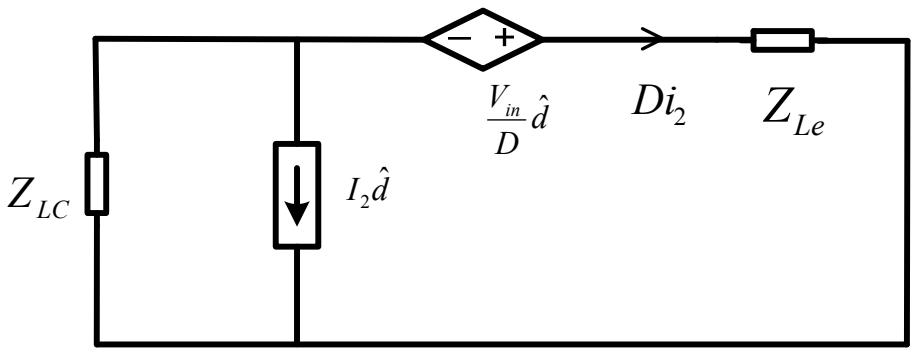


Figure 3.8 Simplified model of buck mode.

$$Z_{LC}(I_2\hat{d} + D\hat{i}_2) = \frac{V_{in}}{D}\hat{d} - Z_{Le}\cdot D\hat{i}_2 \tag{3.29}$$

$$\begin{aligned} &Z_{LC}(I_2\hat{d} + D\hat{i}_2) = \frac{V_{in}}{D}\hat{d} - Z_{Le}\cdot D\hat{i}_2 \\ &\Rightarrow G_{id} = \frac{\hat{i}_2}{\hat{d}} = \frac{\frac{V_{in}}{D\cdot Z_{LC}} - I_2}{D\cdot(1+\frac{Z_{Le}}{Z_{LC}})} \end{aligned} \tag{3.30}$$

where

$$Z_{LC} = (sL_1 + DCR_1)\left\|(\frac{1}{sC_1} + ESR_1)\right. \tag{3.31}$$

$$r_e = DCR_1 \left\| ESR_1 \right. \tag{3.32}$$

$$Z_{Le} = s\frac{L_2}{D^2} + \frac{DCR_2}{D^2} + \frac{D'}{D}r_e = s\frac{L_2}{D^2} + \frac{DCR_2}{D^2} + \frac{D'}{D}(DCR_1 \left\| ESR_1 \right.) \tag{3.33}$$

Thus,

$$G_{id\_buck} = \frac{\hat{i}_2}{\hat{d}} = \frac{\frac{V_{in}}{D\cdot Z_{LC}} - I_2}{D\cdot(1+\frac{Z_{Le}}{Z_{LC}})} = \frac{V_{in} - I_2 Z_{LC} D}{D^2\cdot(Z_{LC}+Z_{Le})} = \frac{V_{in} - I_2\frac{(sL_1+DCR_1)(\frac{1}{sC_1}+ESR_1)}{(sL_1+DCR_1)+(\frac{1}{sC_1}+ESR_1)}D}{D^2\cdot(\frac{(sL_1+DCR_1)(\frac{1}{sC_1}+ESR_1)}{(sL_1+DCR_1)+(\frac{1}{sC_1}+ESR_1)} + s\frac{L_2}{D^2} + \frac{DCR_2}{D^2} + \frac{D'}{D}r_e)} \tag{3.34}$$

Then G_{id_buck} can be derived as

$$G_{id\_buck}=\frac{V_{in}\left[(sL_1+DCR_1)+(\frac{1}{sC_1}+ESR_1)\right]-I_2(sL_1+DCR_1)(\frac{1}{sC_1}+ESR_1)D}{D^2\cdot\left\{(sL_1+DCR_1)(\frac{1}{sC_1}+ESR_1)+\left(s\frac{L_2}{D^2}+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\left[(sL_1+DCR_1)+(\frac{1}{sC_1}+ESR_1)\right]\right\}}$$

$$=\frac{V_{in}\left[(s^2C_1L_1+sC_1\cdot DCR_1)+(1+sC_1\cdot ESR_1)\right]-I_2(sL_1+DCR_1)(1+sC_1\cdot ESR_1)D}{D^2\cdot\left\{(sL_1+DCR_1)(1+sC_1\cdot ESR_1)+\left(s\frac{L_2}{D^2}+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\left[(s^2C_1L_1+sC_1\cdot DCR_1)+(1+sC_1\cdot ESR_1)\right]\right\}}$$

$$=\frac{V_{in}\left[(s^2C_1L_1+sC_1\cdot(ESR_1+DCR_1)+1\right]-I_2D\left[s^2C_1L_1\cdot ESR_1+s(L_1+C_1\cdot ESR_1\cdot DCR_1)+DCR_1\right]}{D^2\cdot\left\{\left(s^2C_1L_1\cdot ESR_1+s(L_1+C_1\cdot ESR_1\cdot DCR_1+\frac{L_2}{D^2})+DCR_1\right)+\left(s\frac{L_2}{D^2}+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\left[s^2C_1L_1+sC_1\cdot(ESR_1+DCR_1)+1\right]\right\}}$$

$$=\frac{V_{in}\left[(s^2C_1L_1+sC_1\cdot(ESR_1+DCR_1)+1\right]-I_2D\left[s^2C_1L_1\cdot ESR_1+s(L_1+C_1\cdot ESR_1\cdot DCR_1)+DCR_1\right]}{D^2\cdot\left\{\left(s^2C_1L_1\cdot ESR_1+s(L_1+C_1\cdot ESR_1\cdot DCR_1+\frac{L_2}{D^2})+DCR_1\right)+\left[s^3C_1L_1\frac{L_2}{D^2}+s^2C_1\left(\frac{L_2}{D^2}\cdot(ESR_1+DCR_1)+L_1\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\right)+s\left(\frac{L_2}{D^2}+C_1(ESR_1+DCR_1)\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\right)+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right]\right\}}$$

$$=\frac{V_{in}\left[(s^2C_1L_1+sC_1\cdot(ESR_1+DCR_1)+1\right]-I_2D\left[s^2C_1L_1\cdot ESR_1+s(L_1+C_1\cdot ESR_1\cdot DCR_1)+DCR_1\right]}{D^2\cdot\left[s^3C_1L_1\frac{L_2}{D^2}+s^2C_1\left(L_1\cdot ESR_1+\frac{L_2}{D^2}\cdot(ESR_1+DCR_1)+L_1\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\right)+s\left(\frac{L_2}{D^2}+C_1(ESR_1+DCR_1)\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)+L_1+C_1\cdot ESR_1\cdot DCR_1+\frac{L_2}{D^2}\right)+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e+DCR_1\right]}$$

(3.35)

$$G_{id\_buck}=\frac{s^2C_1L_1(V_{in}-I_2D\cdot ESR_1)+s\left[V_{in}C_1\cdot(ESR_1+DCR_1)-I_2D(L_1+C_1\cdot ESR_1\cdot DCR_1)\right]+V_{in}-I_2D\cdot DCR_1}{D^2\cdot\left[s^3C_1L_1\frac{L_2}{D^2}+s^2C_1\left(L_1\cdot ESR_1+\frac{L_2}{D^2}\cdot(ESR_1+DCR_1)+L_1\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)\right)+s\left(\frac{L_2}{D^2}+C_1(ESR_1+DCR_1)\left(\frac{DCR_2}{D^2}+\frac{D'}{D}r_e\right)+L_1+C_1\cdot ESR_1\cdot DCR_1\right)+\frac{DCR_2}{D^2}+\frac{D'}{D}r_e+DCR_1\right]}$$

(3.36)

Similarly to 3.1.1, the simulation model of buck mode for AC analysis of control - to - output inductor current has been built as shown in Figure 3.9. The Bode plot of its transfer function is extracted and the Bode plot data obtained from simulation is put into a Mathcad file and compared with that of derived averaged model in (3.36). In Figure 3.10, under condition V_{in} = *200 V* and V_o = *10 V*, the blue dashed curve is from Simplis simulation model and the red solid one is obtained from the mathematic model. It is noticed that at the switching frequency, both gain and phase have a little glitch in simulation result, whereas the derived model does not have. Except at this switching frequency and its multiples, the simulated result matches that of the mathematic model very well. Thus, the mathematic model could be used for further analysis.

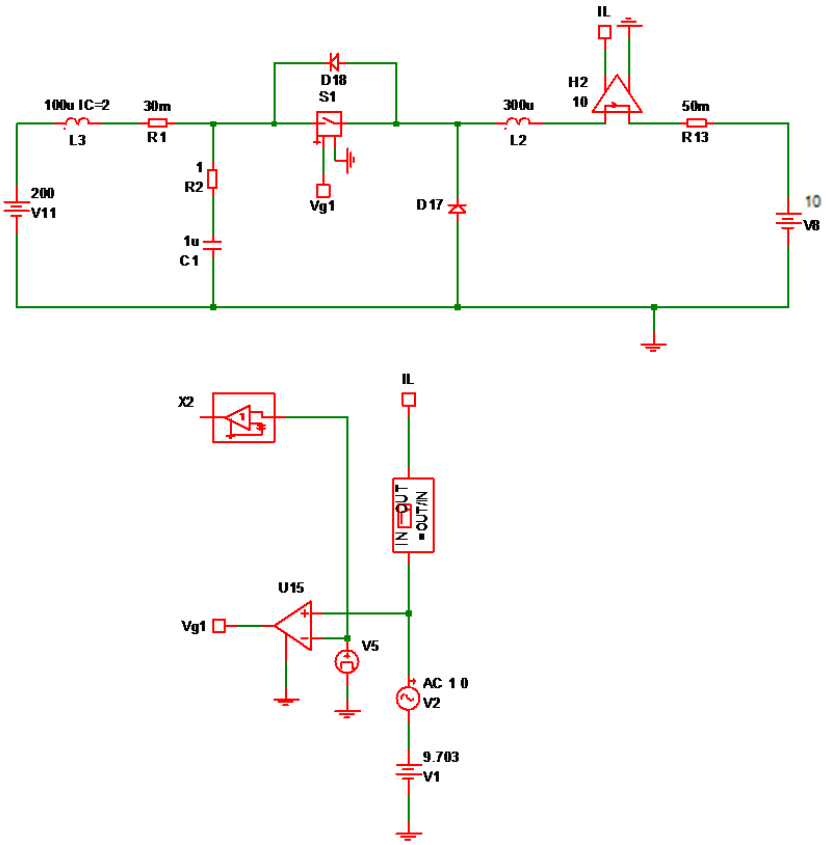


Figure 3.9 Buck mode simulation Model in Simplis.

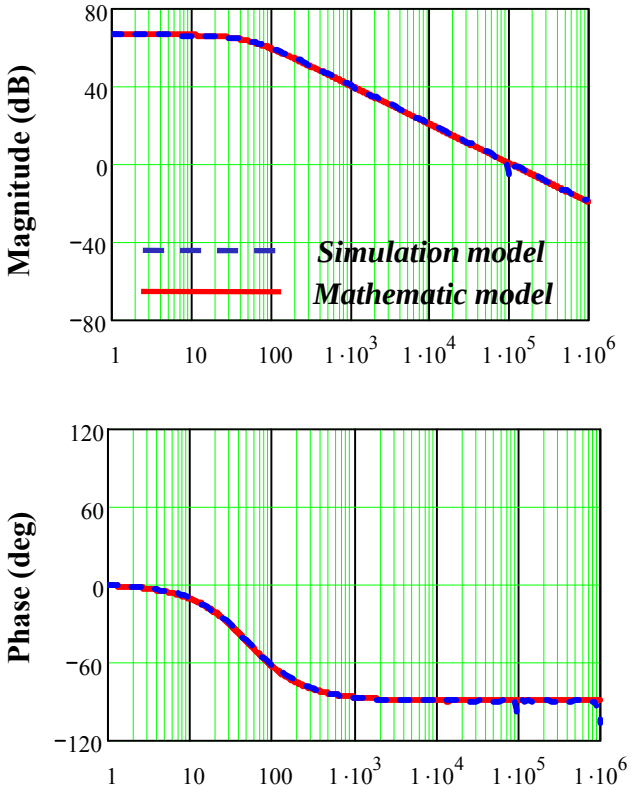


Figure 3.10 Comparison between mathematic model and Simplis simulation model.

Based on (3.36), when $f = 0$, DC gain could be obtained as below:

$$G_{id\_buck} = \frac{V_{in} - I_2 D \cdot DCR_1}{DCR_2 + D'Dr_e + D^2 \cdot DCR_1} \approx \frac{V_{in}}{DCR_2 + D'Dr_e + D^2 \cdot DCR_1} \tag{3.37}$$

It could be easily found that the DC gain is related to input voltage V_{in}, duty cycle D and the parasitic resistance.

In order to obtain the single pole and double - pole position, the denominator of G_{id_buck} needs to be zero. However, some approximations are needed since it is a very complicated expression. From the Bode plot, it is found that the single pole is in low

frequency range, and the double - pole is in high frequency range. Therefore, the approximations could be obtained to find out the single pole and double - pole positions as shown in (3.38) and (3.39).

$$D^2\left[\begin{array}{l} s^3C_1L_1\dfrac{L_2}{D^2}+s^2C_1\left(L_1\cdot ESR_1+\dfrac{L_2}{D^2}\cdot(ESR_1+DCR_1)+L_1\left(\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e\right)\right) \\ +s\left(\dfrac{L_2}{D^2}+C_1(ESR_1+DCR_1)\left(\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e\right)+L_1+C_1\cdot ESR_1\cdot DCR_1+\dfrac{L_2}{D^2}\right)+\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e+DCR_1 \end{array}\right] \quad (3.38)$$

$$\approx s\left(2L_2+L_1\cdot D^2\right)+DCR_2+D'Dr_e+D^2\cdot DCR_1=0$$

Thus, the single pole position can be obtained as:

$$s=-\frac{DCR_2+D'Dr_e+D^2\cdot DCR_1}{2L_2+L_1\cdot D^2} \quad (3.39)$$

It could be easily found that the single pole position is related to duty cycle D, two inductors L_1 and L_2 and the parasitic resistance.

In order to obtain the double - pole position, the numerator of G_{id_buck} needs to be zero as well.

$$D^2\left[\begin{array}{l} s^3C_1L_1\dfrac{L_2}{D^2}+s^2C_1\left(L_1\cdot ESR_1+\dfrac{L_2}{D^2}\cdot(ESR_1+DCR_1)+L_1\left(\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e\right)\right) \\ +s\left(\dfrac{L_2}{D^2}+C_1(ESR_1+DCR_1)\left(\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e\right)+L_1+C_1\cdot ESR_1\cdot DCR_1+\dfrac{L_2}{D^2}\right)+\dfrac{DCR_2}{D^2}+\dfrac{D'}{D}r_e+DCR_1 \end{array}\right] \quad (3.40)$$

$$\approx s^3C_1L_1L_2+s\left(L_2+L_1\cdot D^2\right)=0$$

Thus, the double - pole position can be obtained as:

$$s=\pm\sqrt{\frac{L_2+L_1\cdot D^2}{C_1L_1L_2}}j \quad (3.41)$$

It could be easily found that the double - pole position is related to duty cycle D, two inductors L_1 and L_2 and capacitor C_1.

Similarly, double - zero position can be obtained as shown in (3.42) – (3.44).

$$\begin{aligned} & s^2 C_1 L_1 (V_{in} - I_2 D \cdot ESR_1) + s\left[V_{in} C_1 \cdot (ESR_1 + DCR_1) - I_2 D(L_1 + C_1 \cdot ESR_1 \cdot DCR_1)\right] + V_{in} - I_2 D \cdot DCR_1 \\ & \approx s^2 C_1 L_1 V_{in} + s\left[V_{in} C_1 \cdot (ESR_1 + DCR_1) - I_2 D \cdot L_1\right] + V_{in} = 0 \end{aligned} \tag{3.42}$$

$$s = \frac{-\left[V_{in} C_1 \cdot (ESR_1 + DCR_1) - I_2 D \cdot L_1\right] \pm \sqrt{\left[V_{in} C_1 \cdot (ESR_1 + DCR_1) - I_2 D \cdot L_1\right]^2 - 4 C_1 L_1 V_{in} \cdot V_{in}}}{2 C_1 L_1 V_{in}} \tag{3.43}$$

$$s = \frac{\left[I_2 D \cdot L_1 \Big/ V_{in} - C_1 \cdot (ESR_1 + DCR_1)\right] \pm \sqrt{4 C_1 L_1}\, j}{2 C_1 L_1} \tag{3.44}$$

It can also be found that the double - zero position is related to duty cycle D, inductors L_1, the current going through inductor L_2, capacitor C_1 and parasitic resistance. And it also need to be noted that the double - zero will move from left half plane (LHP) to right half plane (RHP) if $I_2 D$ becomes larger than $C_1 \cdot (ESR_1 + DCR_1) \cdot V_{in} \Big/ L_1$.

Where $I_2 D = \begin{cases} I_2 \dfrac{V_o}{V_{in}} = \dfrac{P_o}{V_{in}} & (V_{in} \geq 340V) \\ I_2 \dfrac{V_{in}}{V_{in}} = I_2 & (V_{in} < 340V) \end{cases}$. Thus, the double - zero will be in RHP if in heavy power condition.

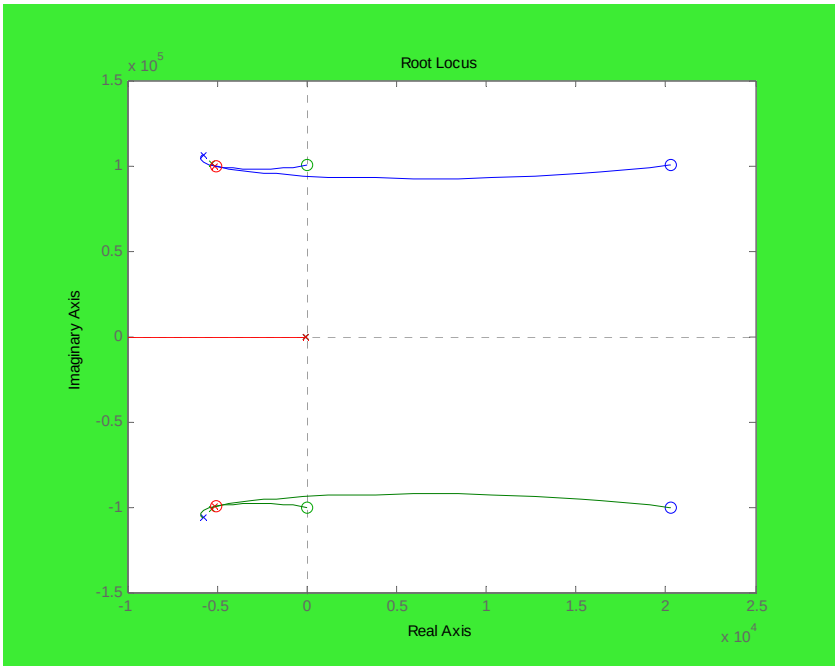


Figure 3.11 Root locus of different D (V_{in}=340)

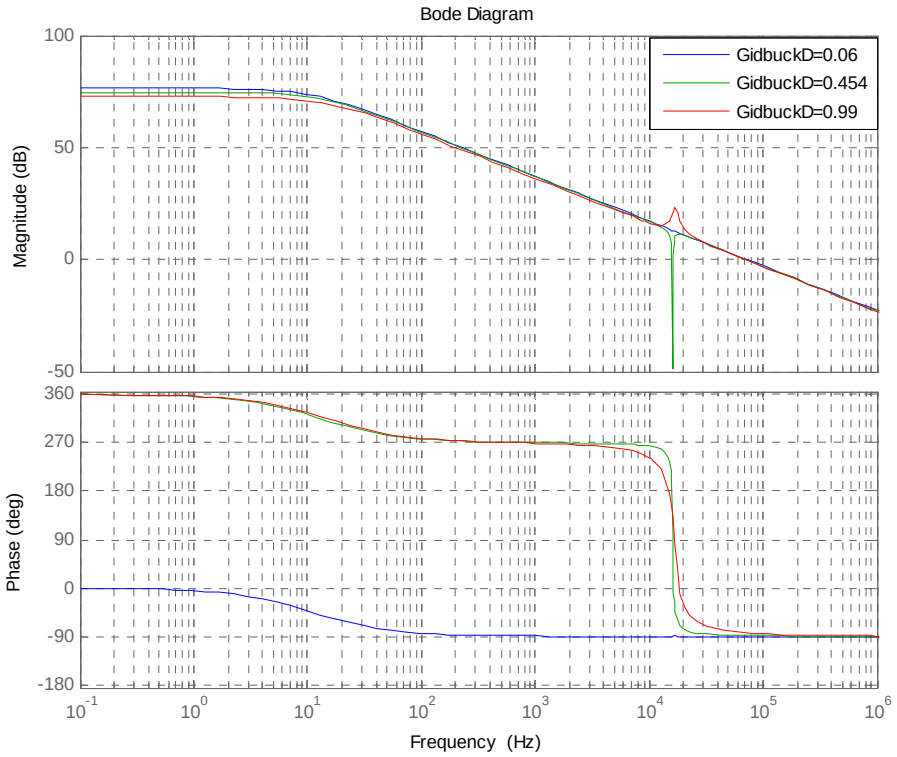


Figure 3.12 Bode plot of different D (V_{in}=340)

From Figure 3.11 and Figure 3.12, some features of buck mode could be noticed.

- The double-pole and double-zero positions are very close to each other.
- The buck mode is automatically stable, if the double-zero is in LHP.
- There will be a high Q, if the double-zero is in RHP.
- Because of the RHP double-zero, we need a compensator which can make the crossover happen before the position of Q.
- There is a need to design based on the worst condition, which is the one with highest Q.

Since there are double - pole and a single pole in G_{id_buck}, the denominator can be expressed as below:

$$\left(s^2+\frac{\omega_0}{Q}s+\omega_0^2\right)\left(s+s_p\right)=s^3+\left(\frac{\omega_0}{Q}+s_p\right)s^2+\left(\omega_0^2+\frac{\omega_0\cdot s_p}{Q}\right)s+\omega_0^2\cdot s_p \tag{3.45}$$

Then

$$\left.\begin{aligned} s_p &= \frac{DCR_2+D'Dr_e+DCR_1\cdot D^2}{2L_2+L_1\cdot D^2} \\ \omega_0^2\cdot s_p &= \frac{DCR_2+D'Dr_e+DCR_1\cdot D^2}{C_1L_1L_2} \end{aligned}\right\} \Rightarrow \omega_0=\sqrt{\frac{2L_2+L_1\cdot D^2}{C_1L_1L_2}} \tag{3.46}$$

Thus,

$$\begin{aligned} \frac{\omega_0}{Q}+s_p &= \frac{C_1\left(L_1\cdot ESR_1\cdot D^2+L_2\cdot(ESR_1+DCR_1)+L_1\left(DCR_2+D'Dr_e\right)\right)}{C_1L_1L_2} \\ &= \frac{ESR_1\cdot D^2+DCR_2+D'Dr_e}{L_2}+\frac{ESR_1+DCR_1}{L_1} \end{aligned} \tag{3.47}$$

Thus, Q could be obtained as shown in (3.48).

$$Q = \frac{\sqrt{\frac{2L_2 + L_1 \cdot D^2}{C_1 L_1 L_2}}}{\frac{ESR_1 \cdot D^2 + DCR_2 + D'Dr_e}{L_2} + \frac{ESR_1 + DCR_1}{L_1} - \frac{DCR_2 + D'Dr_e + DCR_1 \cdot D^2}{2L_2 + L_1 \cdot D^2}} \tag{3.48}$$

Assume $ESR_1 \gg DCR_1, ESR_1 \gg DCR_2, and\ L_2 > L_1$, then Q could be approximated as below:

$$Q \approx \frac{\sqrt{\frac{2L_2 + L_1 \cdot D^2}{C_1 L_1 L_2}}}{\frac{(2ESR_1 - DCR_1) \cdot D^2 + DCR_2}{2L_2} + \frac{ESR_1 + DCR_1}{L_1}} \tag{3.49}$$

$$Q \approx \frac{\sqrt{\frac{L_1\left(2L_2 + L_1 \cdot D^2\right)}{C_1 L_2}}}{ESR_1 + DCR_1} \tag{3.50}$$

From the expression of Q, it can be noticed that Q will change apparently with D, C_1, L_1, ESR_1, DCR_1 and L_2. And L_1 impacts Q more than L_2 and C_1. Since Q changes with D, Q will be always changing in the line cycle. The larger D and L_1 are, the larger Q will be. The larger C_1, ESR_1, DCR_1 and L_2 are, the smaller Q will be. Since $0 \le D \le 1$, the largest Q happens at $D = 1$.

3.2 Control of Boost-Buck Converter Based PV Inverter

During buck mode, L_2's current can be treated as normal buck converter's output inductor current which can be easily controlled. However, it is critical to control L_2's current in boost mode because the control target in this mode is its output filter's inductor current. Thus, the compensator for boost mode needs to be designed first and then applies

it to buck mode. In practice, if the boost mode is stable and well controlled, buck mode will be stable and well controlled as well. The loop gains of boost mode at different operating points are shown in Figure 3.13. It clearly shows that the RHP zero and double-pole make 270° phase delay, which makes it difficult to be compensated. Thus, the compensated crossover frequency needs to be before double-pole's frequency of the boost mode and to insure that the peak Q value is lower than 0dB. In order to have a compensator that is good for every operation point, the compensator design is based on the worst conditions, which is defined as a condition with highest Q_{pk} and the earliest phase drop. In our case, worst condition happens when input voltage is the lowest defined value 200 V and output voltage is the peak voltage of the grid 340 V.

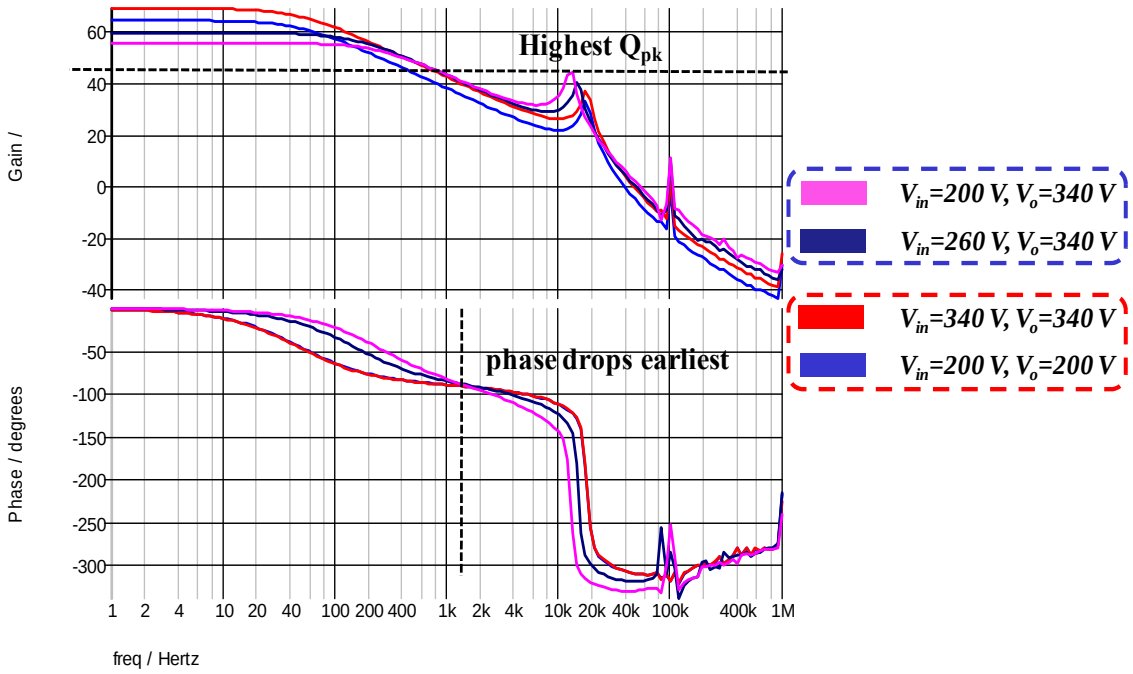


Figure 3.13 Loop gain of boost mode at different operating point.

In order to achieve smooth waveform in transition between boost to buck modes, an offset of the sawtooth carrier right on the top of the buck mode PWM modulator needs to be applied to boost mode as shown in Figure 3.14. The high gain of buck mode can be realized by reducing the carrier magnitude for buck mode as described in 4.2. As a result, universal control for both modes can be achieved. If a digital signal processor (DSP) is employed as a controller, smooth transition between the two modes can be achieved in various ways by taking advantage of flexible algorithm implementation. For example, in our test-bed system, the signal after compensator is deducted by a unit as shown in Figure 3.15 in order to achieve smooth transition between the two modes.

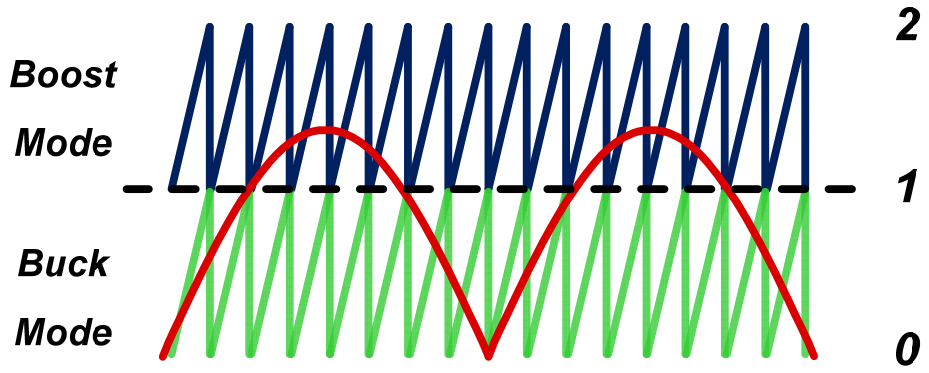


Figure 3.14 Analog control for smooth.

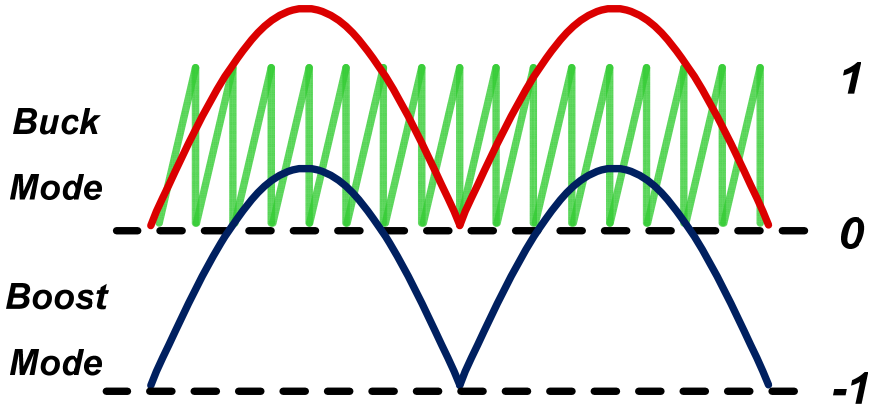


Figure 3.15 Digital control for smooth.

3.3 Proposed Partial - Interleaved PV Inverter

Table 3.1 lists the transfer function derivation results for both boost and buck modes. It can be seen that the inductor value is the dominant factor to the resonant frequency, or double-pole frequency. If L_1 can be reduced, the double-pole position, which is considered as the frequency wall of bandwidth, will be pushed to higher frequency. Moreover, the gain will increase as well, and also the Q factor will be reduced accordingly as shown in Figure 3.16, which benefits the high bandwidth design for the boost mode. However, decreasing L_2 will keep the same double-pole position and have higher Q factor as shown in Figure 3.17, which won't help controller design. As a result, small L_1 and large L_2 are preferred from the design point of view.

Table 3.1 Bode plot parameters derivation.

BOOST MODE		BUCK MODE		
Double-pole position	Q	Double-pole position	Double-zero position	Q
$s = \pm\sqrt{\frac{L_2 D'^2 + L_1}{C_1 L_1 L_2}}\,j$	$Q \approx \frac{\sqrt{\left(L_2 \cdot D'^2 + L_1\right) L_1}}{D'^4 C_1 L_2}}{ESR_1}$	$s = \pm\sqrt{\frac{L_2 + L_1 \cdot D^2}{C_1 L_1 L_2}}\,j$	$s = \frac{\left[I_2 D \cdot L_1 \middle/ V_{in} - C_1 \cdot (ESR_1 + DCR_1) \right] \pm \sqrt{4 C_1 L_1}\,j}{2 C_1 L_1}$	$Q \approx \frac{\sqrt{\frac{L_1\left(2L_2 + L_1 \cdot D^2\right)}{C_1 L_2}}}{ESR_1 + DCR_1}$

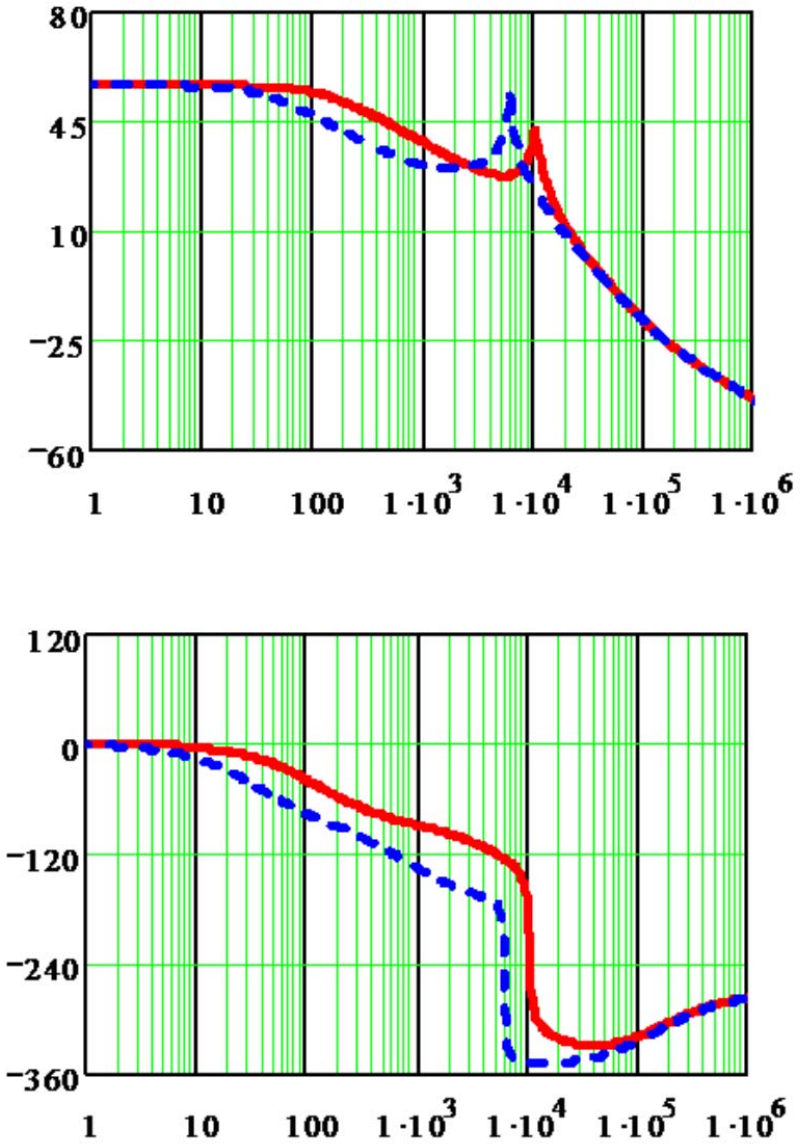


Figure 3.16 Boost inductance L_1's impact on boost mode bode plot G_{id_boost}.

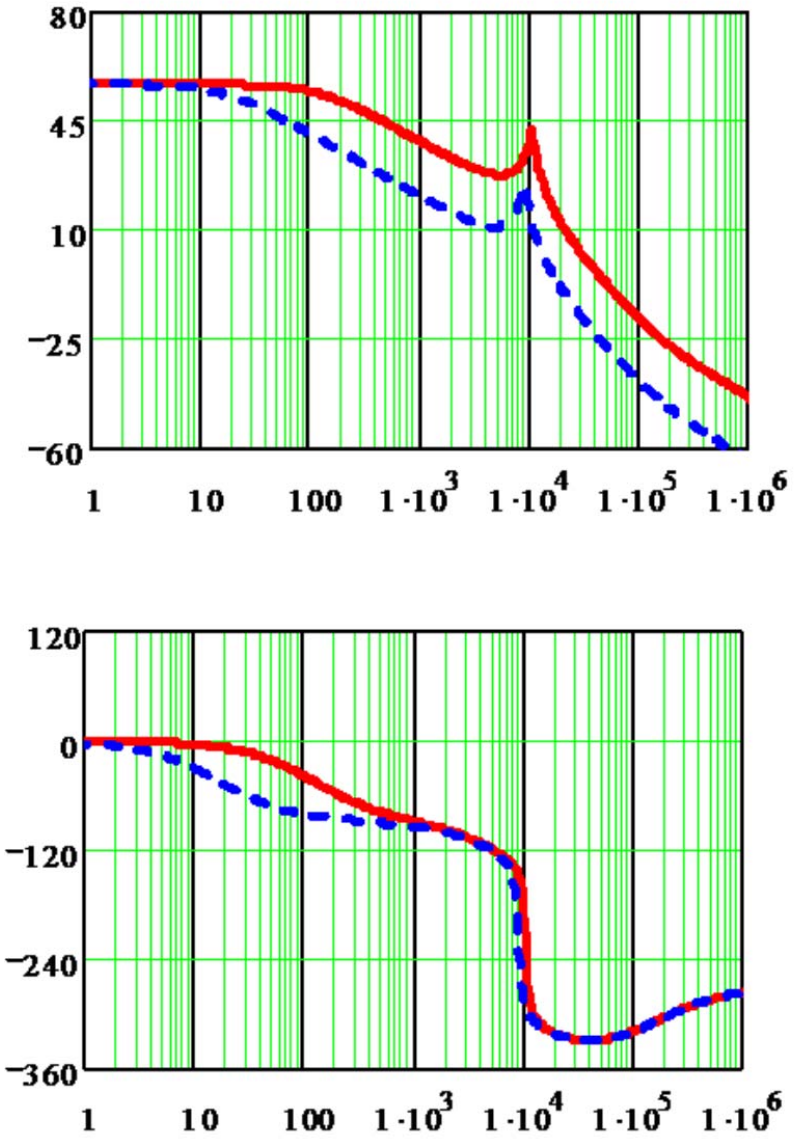


Figure 3.17 Buck inductance L_2's impact on boost mode bode plot G_{id_boost}.

If the switching frequency can be increased so that a smaller inductance is utilized, the system will be easier to compensate and more stable. However, the efficiency may decrease in this case. In order to keep high efficiency and stability, an interleaved-boost-

cascaded-with-buck converter [62] is proposed. Figure 3.18 shows the complete circuit diagram.

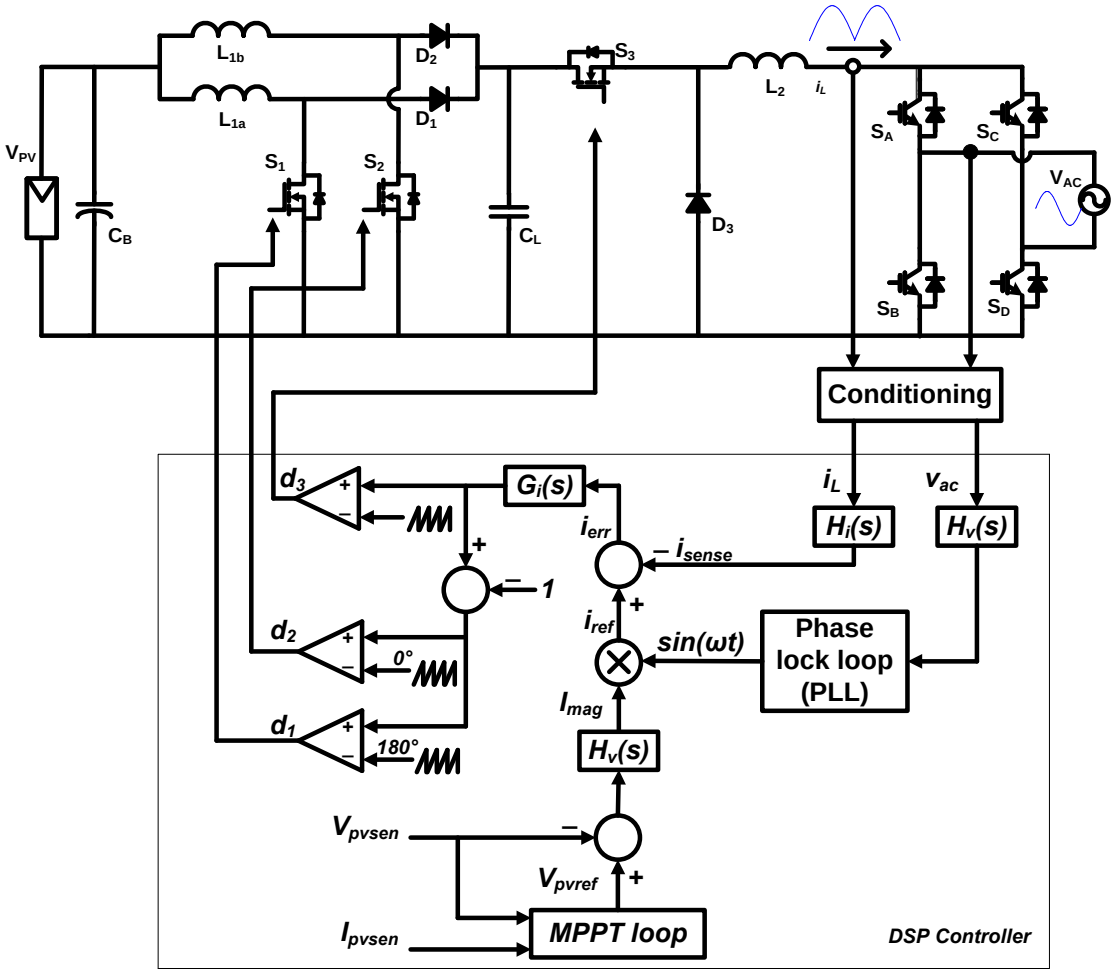


Figure 3.18 Circuit diagram of proposed PV inverter.

3.3.1 Control of the Proposed Interleaved PV Inverter

The model of such a circuit is similar to that of the circuit shown in Figure 3.2 and Figure 3.6, so the same model derived in this section can be used for compensator design. The maximum power point tracking can be implemented as an outer loop with lower

bandwidth control, providing the magnitude of the output current reference [63]-[66]. Figure 3.19 and Figure 3.20 show the analog control diagram and digital control diagram for smooth transition between buck and boost modes respectively. Similar as non-interleaved circuit, for analog control, the boost carrier should be on the top of the carrier for the buck with 180° phase shift for interleaving. For digital control, the boost carrier has the same level as buck carrier with 180° phase shift for interleaving. Furthermore, the compensated signal should be minus one as well as in non-interleaved circuit.

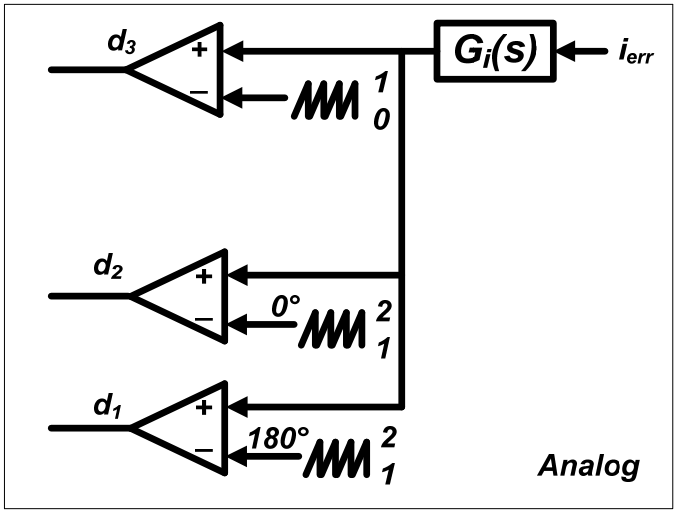


Figure 3.19 Analog control for smooth transition between modes.

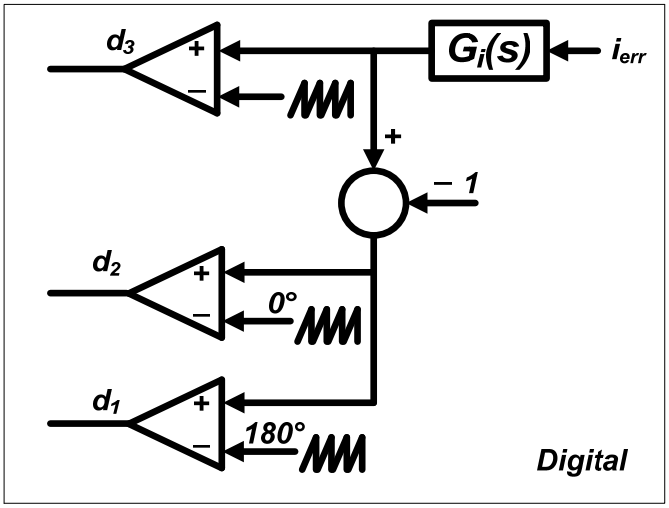


Figure 3.20 Digital control for smooth transition between modes.

Figure 3.21 and Figure 3.22 show the analog control and digital circuit in PSIM, respectively. In the PSIM simulation, the system is considered as continuous-time system since the analog - to - digital (ADC) is not used.

Figure 3.23 and Figure 3.24 illustrate the simulation results using analog control and digital control respectively. These simulation results match the analysis very well and verify that both control methods work for the proposed dual - mode inverter.

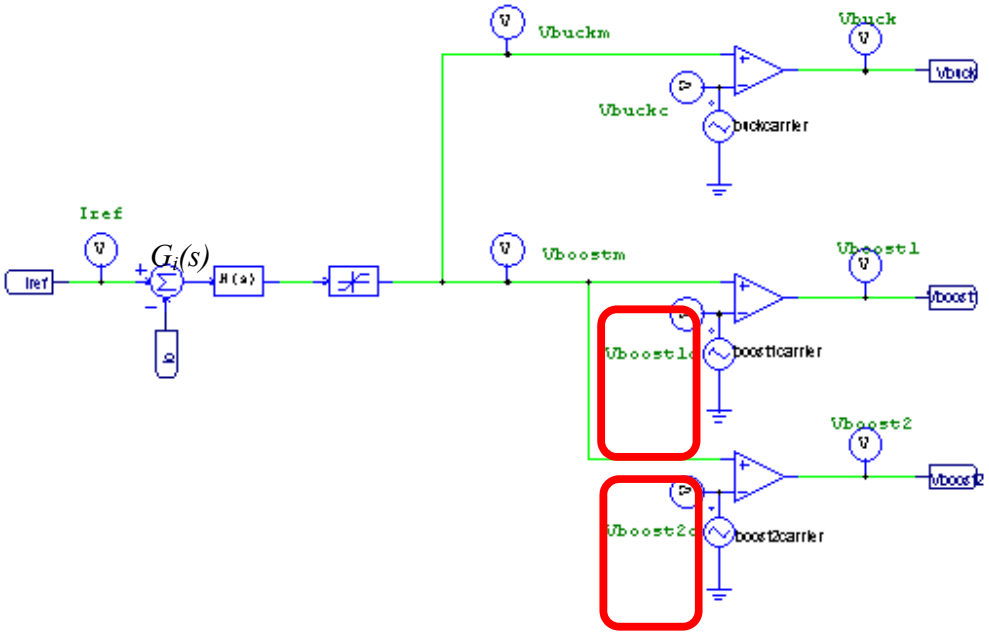


Figure 3.21 Analog control circuit in PSIM.

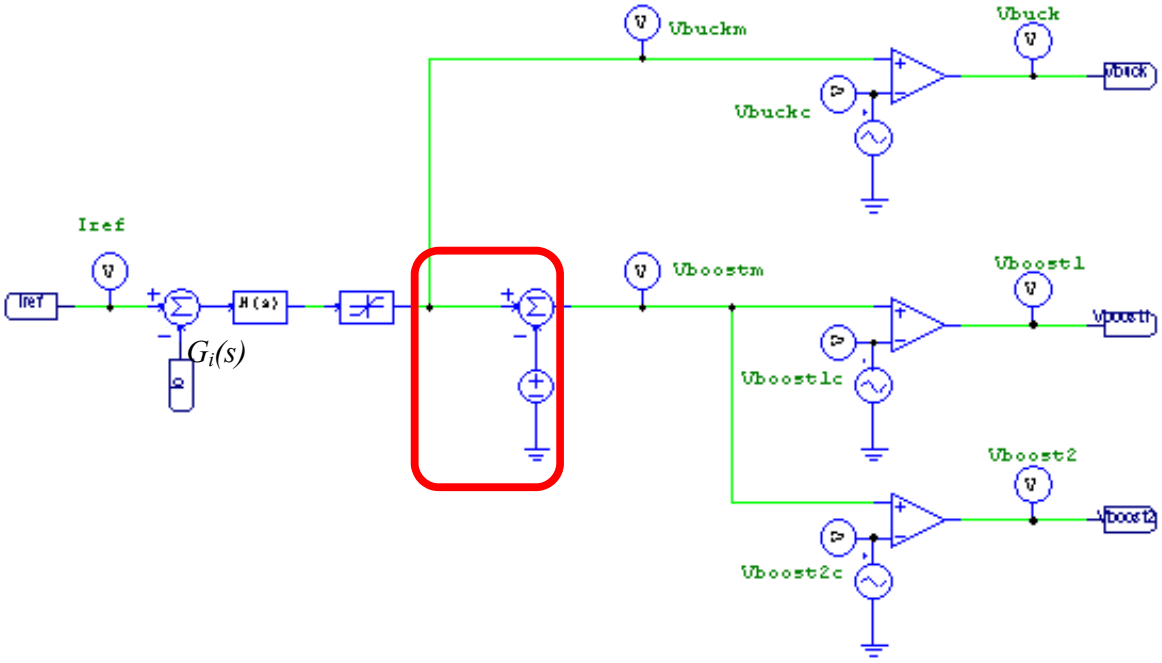


Figure 3.22 Digital control circuit in PSIM.

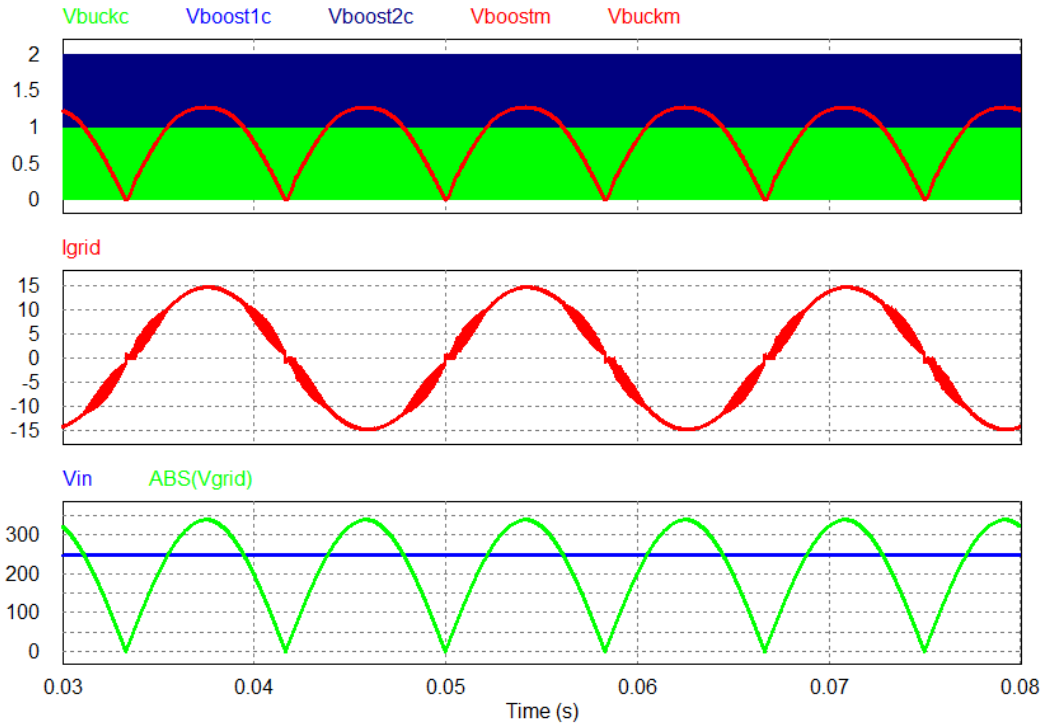


Figure 3.23 Simulation results with analog control.

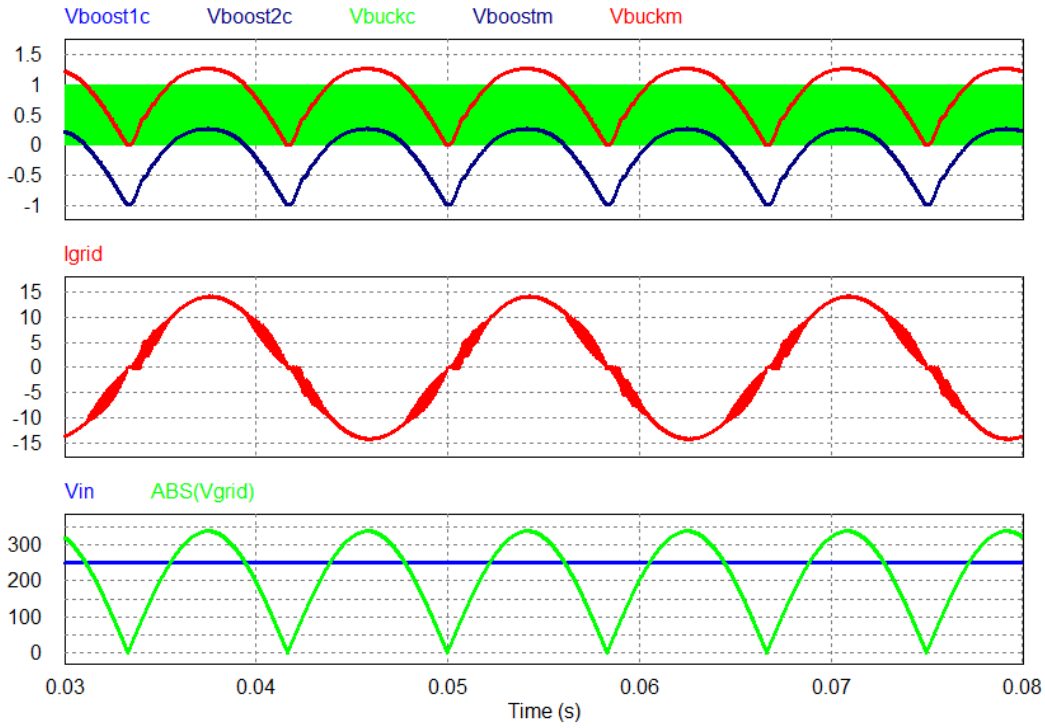


Figure 3.24 Simulation results with digital control.

3.3.2 Maximum Power Point Tracking (MPPT)

The relationship between output voltage and current from the PV module is a function of solar irradiation, module temperature, and amount of partial shadow, as seen in Figure 1.4. According to its *I-V* curve, there is a point where the PV module generates the most power. This point is called the Maximum Power Point (MPP), and the corresponding current and voltage are denoted as I_{MPP} and U_{MPP}. The MPP is different as the PV module's I - V curve changes with irradiance and module temperature. Sometimes it changes rapidly due to fast changes in the weather

conditions such as partial cloudy day; otherwise it is almost constant in a sunny day without clouds.

Because of this characteristic of MPP, some proper algorithms are required for Maximum Power Point Tracking (MPPT). Many researches are conducted of different MPPT techniques [67]-[72]. There are three main methods, which are the most widely used [71]: Perturb and Observe (P&O); Incremental Conductance (INC) and Constant Voltage (CV). The first two are essentially "hill-climbing" methods because they share the same scenario as shown in Table 3.2.

Table 3.2 Scenarios of three most common MPPT methods.

Hill - climbing methods		
Perturb and Observe (P&O)	Incremental Conductance (INC)	Constant Voltage (CV)
Left of the MPP: $\frac{dP}{dV} > 0$ Right of the MPP: $\frac{dP}{dV} < 0$		$\frac{V_{MPP}}{V_{OC}} \approx 0.76$

Here, the P&O MPPT method is chosen. The algorithm for P&O MPPT is shown in Figure 3.25. If logic '1' is set for the 'yes' in the algorithm and logic '0' is set for the 'no' in the algorithm, and this algorithm could be summarized as illustrate in Table 3.3. Then, an XOR logic gate can be used in simulation, as shown in Figure 3.26.

Table 3.3 MPPT logic table.

$P_k > P_{k-1}$	1	1	0	0
$V_k > V_{k-1}$	1	0	1	0
$V_{ref} = V_k + \Delta V$	1	0	0	1

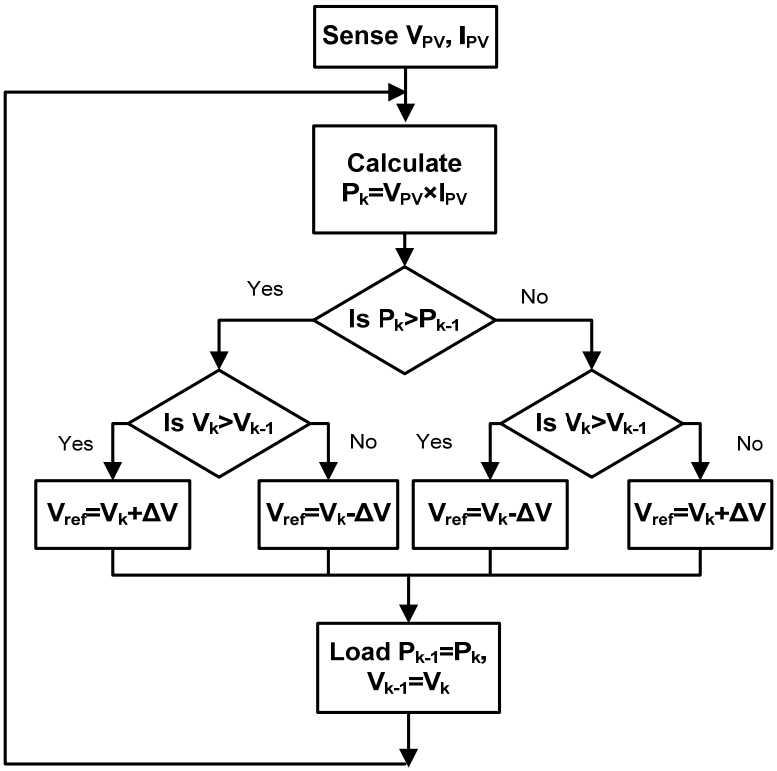


Figure 3.25 P&O MPPT algorithm.

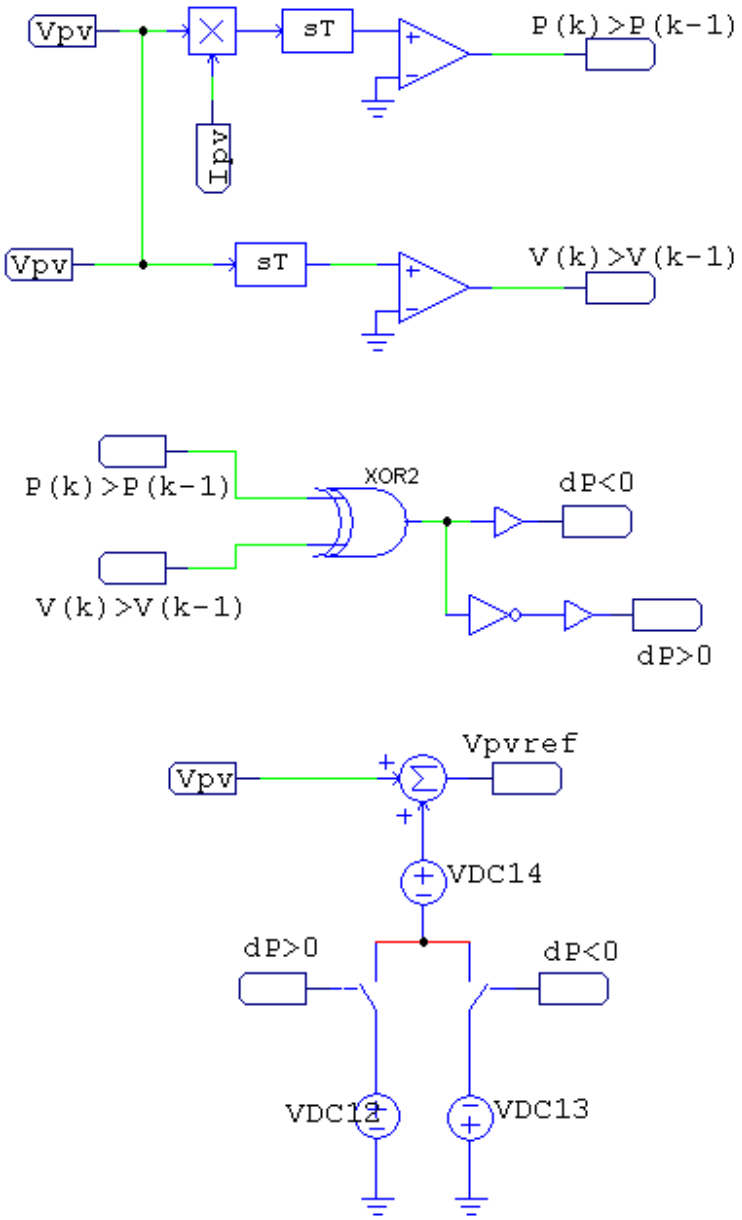
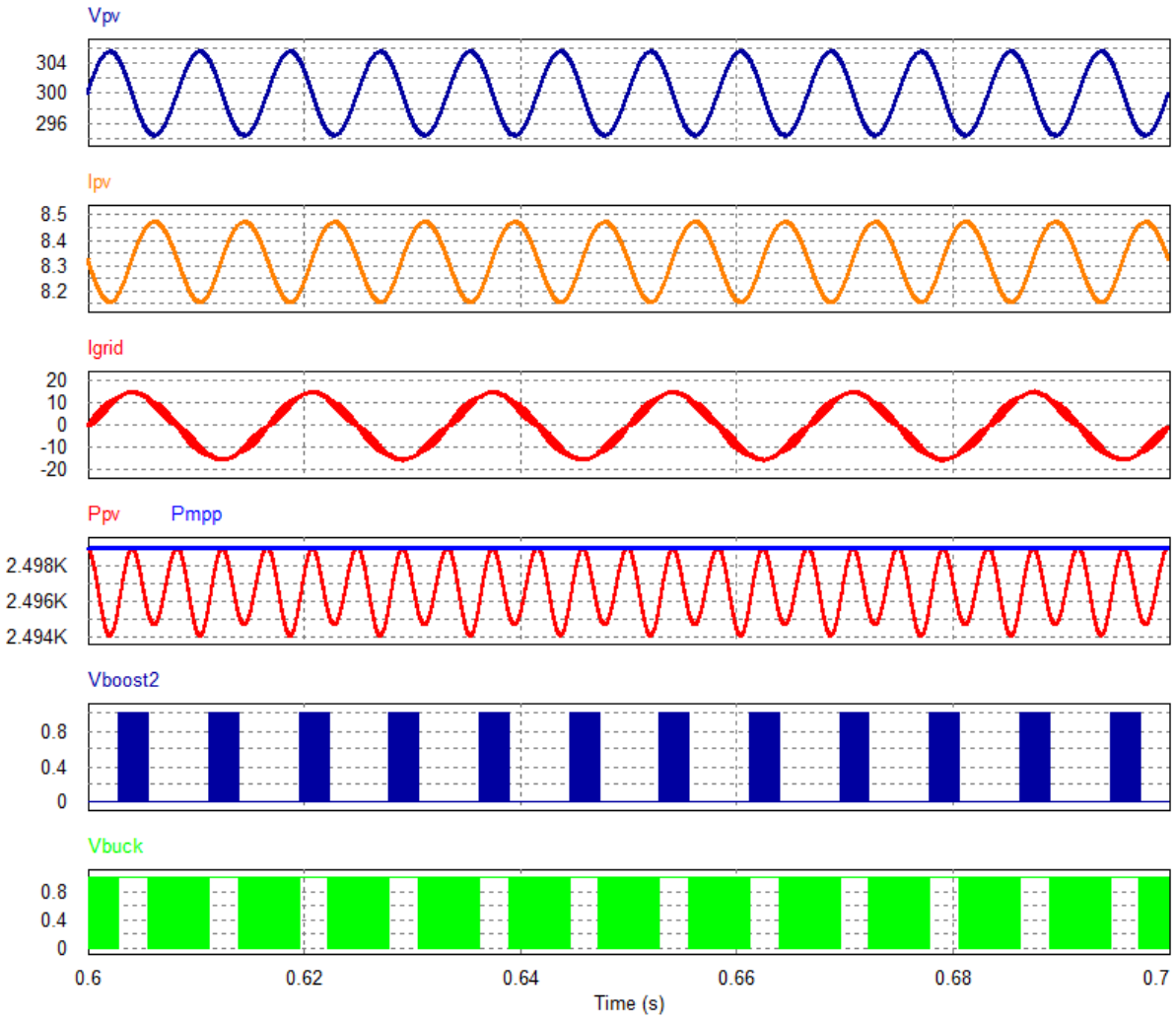
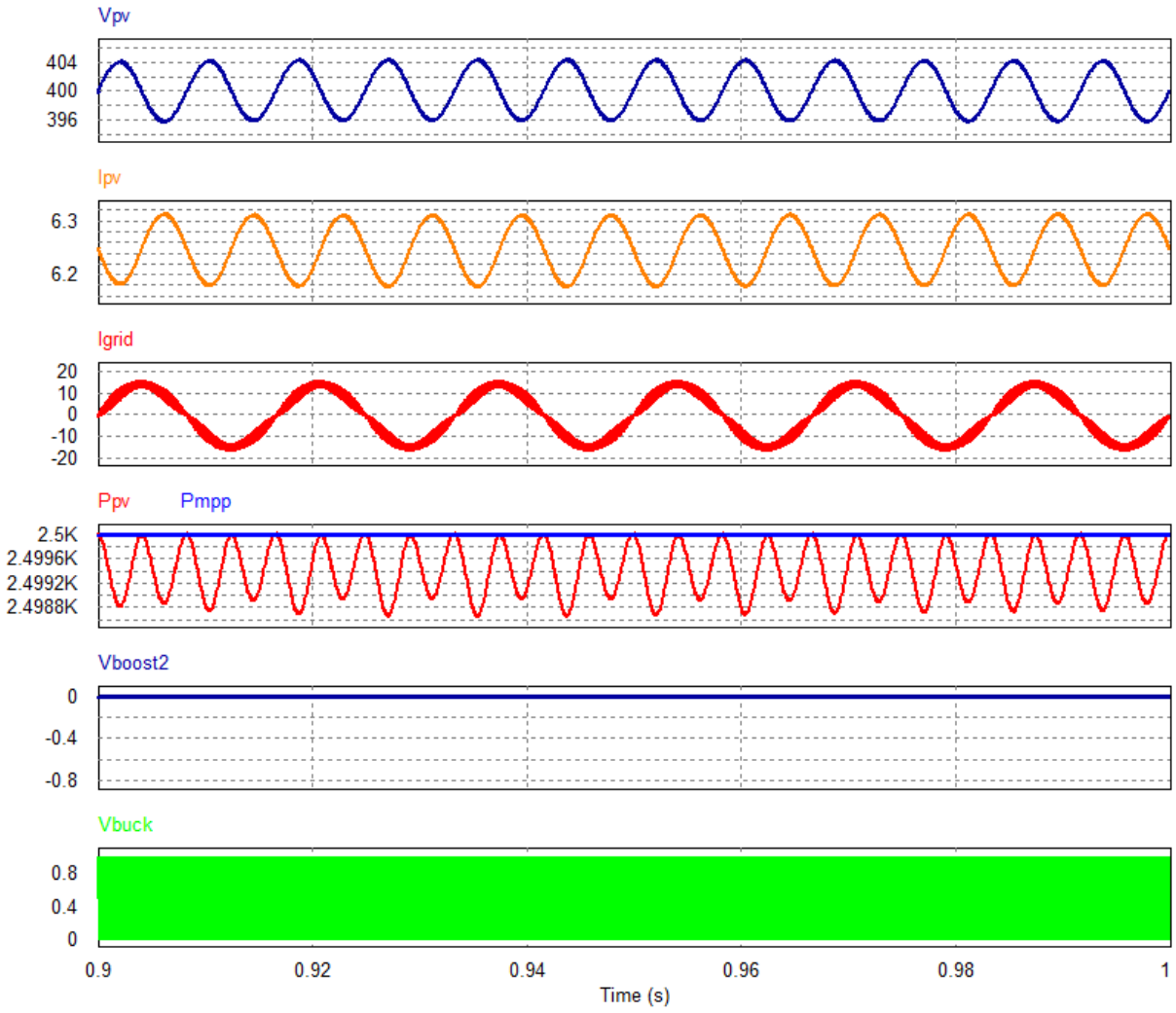


Figure 3.26 P&O MPPT algorithm.


Vpv
304
300
296
Ipv
8.5
8.4
8.3
8.2
Igrid
20
10
0
-10
-20
Ppv
Pmpp
2.498K
2.496K
2.494K
Vboost2
0.8
0.4
0
Vbuck
0.8
0.4
0
0.6
0.62
0.64
0.66
0.68
0.7
Time (s)

(a)



(b)

Figure 3.27 Simulation results with MPPT algorithm in PSIM: (a*) V_{MPP}=300 V; (b) V_{MPP}=400 V*.

3.4 Simulation Results

The proposed PV inverter along with its closed-loop controller has been simulated in PSIM. Figure 3.28 and Figure 3.29 compare the simulation results with different input voltage conditions. In Figure 3.28, the input voltage V_{in} is assumed to be 200 V. As can

be seen in the figure, buck or boost switch does not work simultaneously. S_{boost} works when V_{in} is smaller than the instantaneous grid voltage while S_{buck} works when V_{in} is larger than the instantaneous grid voltage. In this case, the ripple current of L_2 during boost mode is smaller than that during buck mode, because L_2 performs as the output filter's inductor of boost converter but performs a normal output inductor of buck converter. Figure 3.29 shows the simulation results when the input voltage is 400 V. Unlike the previous case, there is no boost mode, and only S_{buck} *is* working. The voltage on middle capacitor C_L always equals to the input voltage since D_{boost} is always conducting.

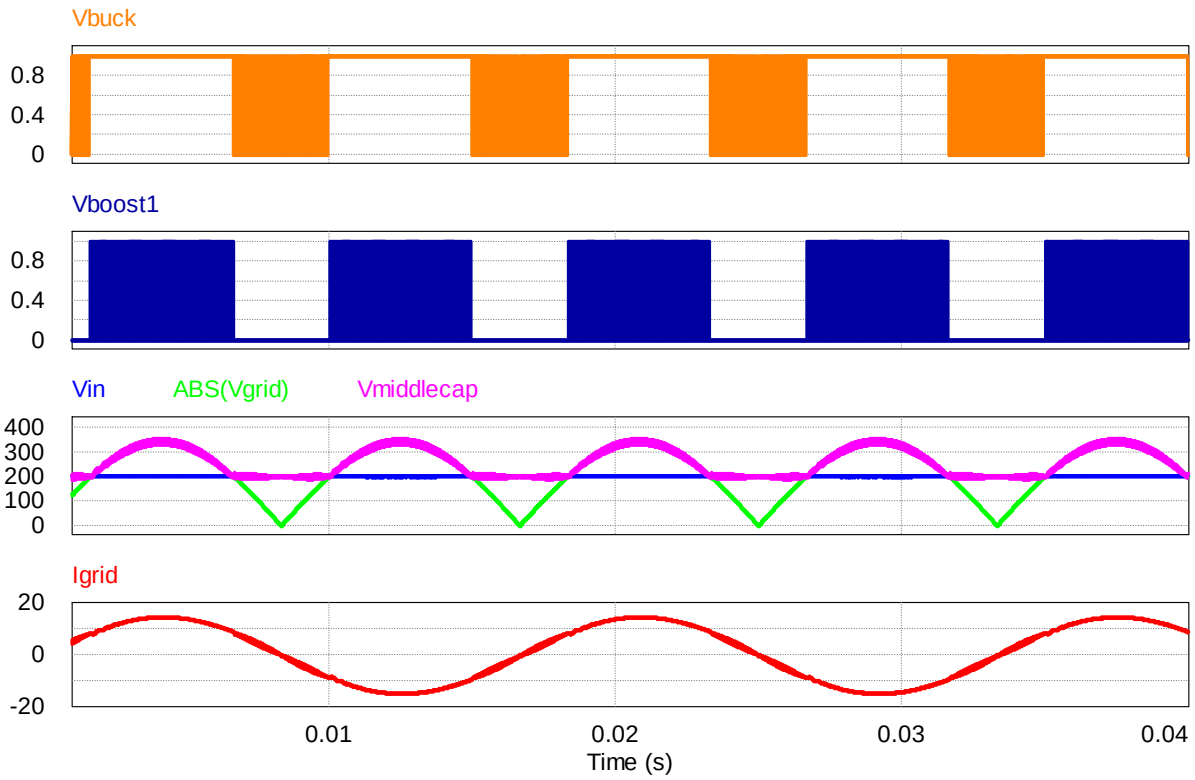


Figure 3.28 Simulation results with small input voltage.

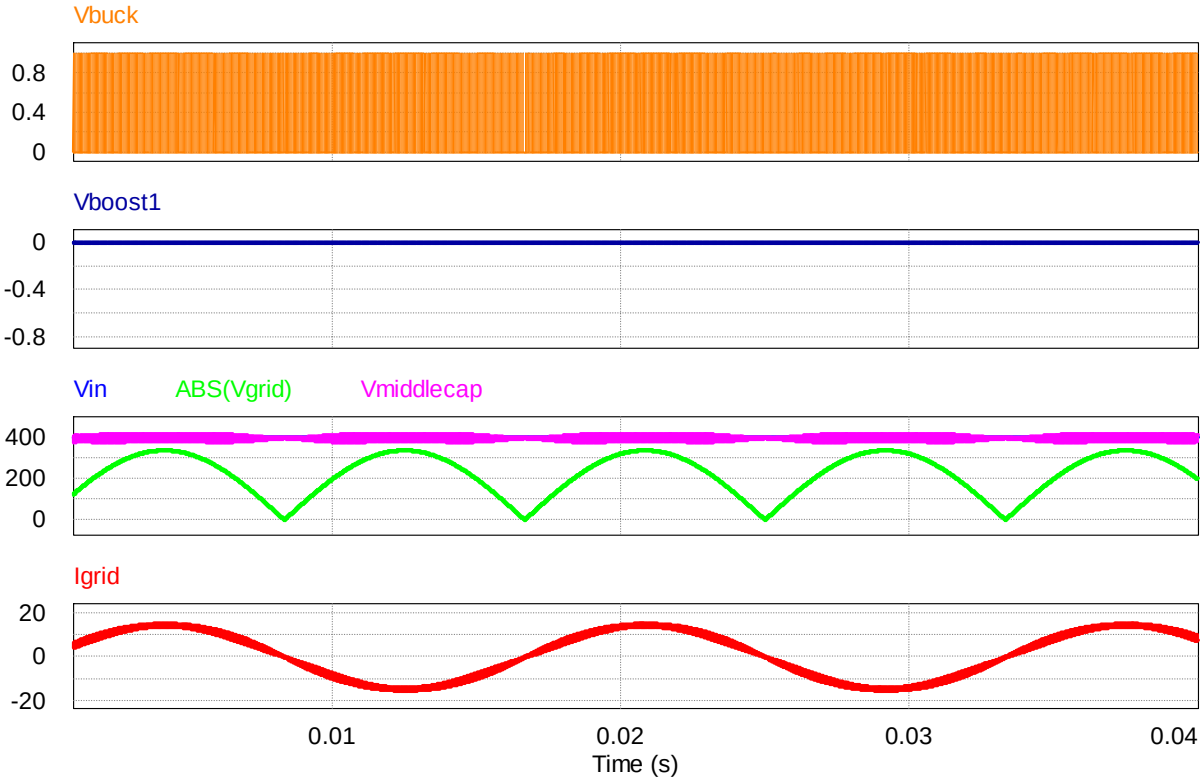


Figure 3.29 Simulation results with large input voltage.

3.5 Experimental Results

Figure 3.30 shows the photograph of the test-bed hardware prototype and Table 3.4 and Table 3.5 list the design parameters and components selection. DSP TMS320F28335 from Texas Instruments has been implemented in the system. Figure 19 shows the PWM and the reference control signals. Figure 3.32 shows the testing results when V_{in} is smaller than the peak of output voltage and Figure 3.33 shows the testing results when V_{in} is almost the same as the peak of output voltage. Figure 3.34 shows the testing results when V_{in} is greater than the peak of output voltage.

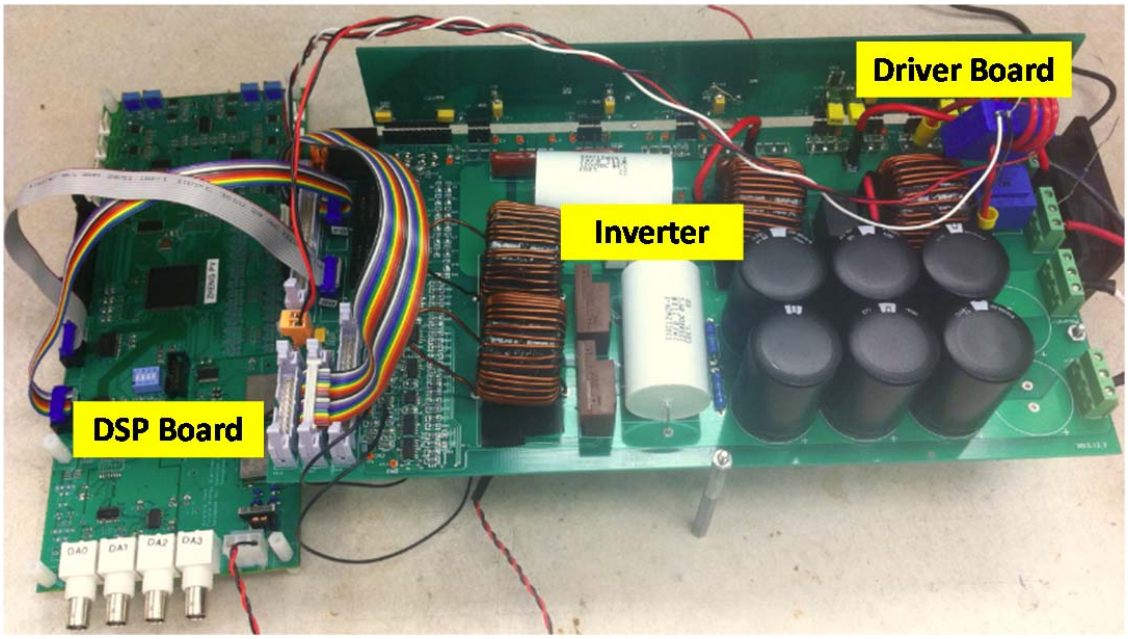


Figure 3.30 Test-bed hardware prototype.

Table 3.4 Design parameters.

Rated Power	2.5 kW
Grid Voltage	208 V_{ac} / 240 V_{ac}
Grid frequency	60 Hz
Input Voltage	200 – 500 V
Switching frequency	50 kHz

Table 3.5 Component selection.

L_{1A}, L_{1B}	200 μH
L_2	400 μH
C_B	2 MF
C_L	2 μF
S_1, S_2, S_3	SPW47N60C3
D_1, D_2, D_3	C3D20060D
S_A, S_B, S_B, S_D	FGH30N60LSD

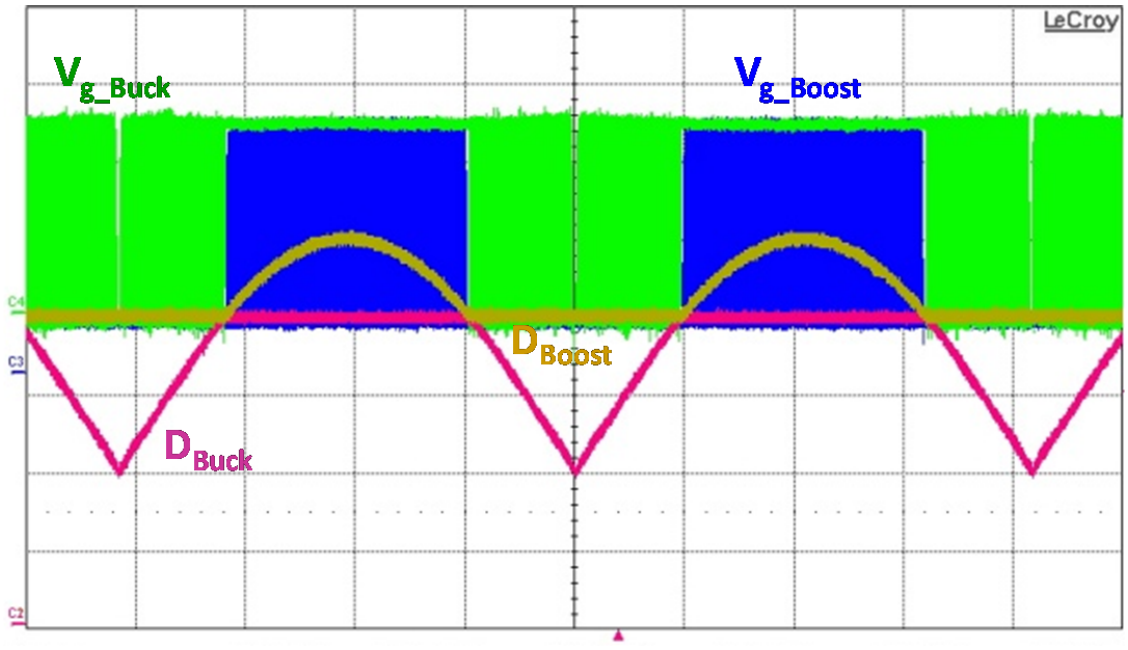


Figure 3.31 Experiment results of PWM signals.

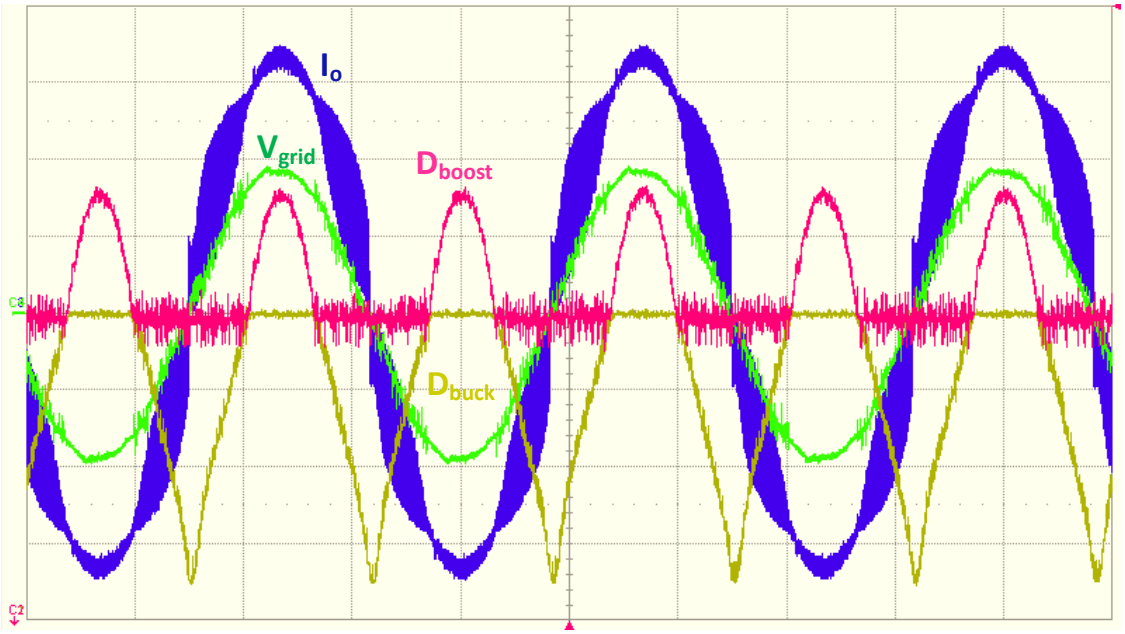


Figure 3.32 Experimental results with small input voltage.

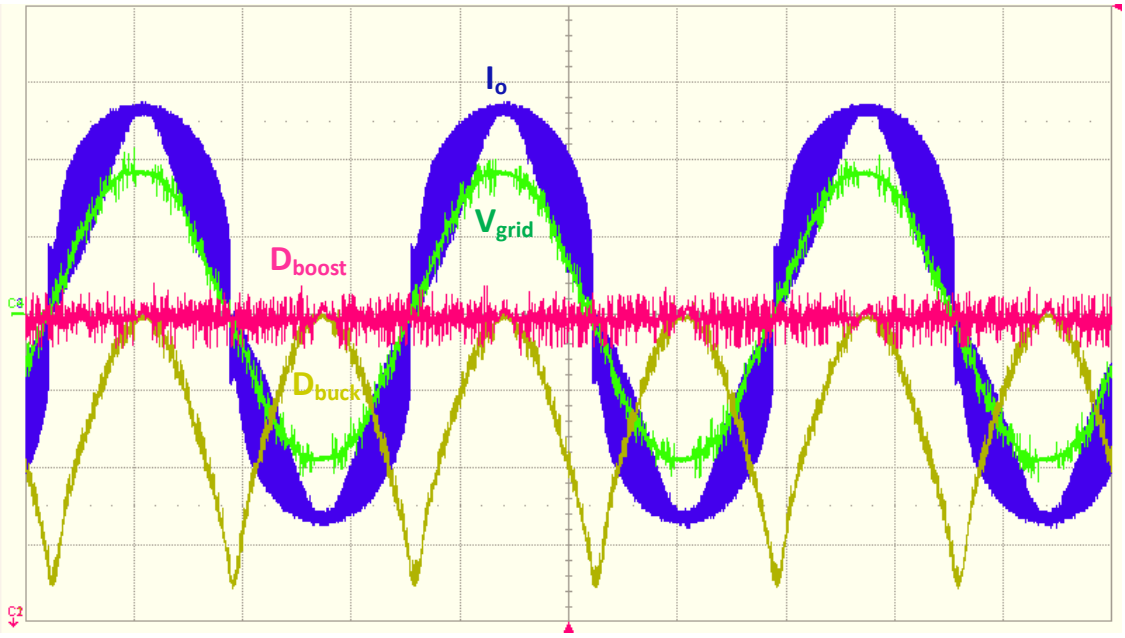


Figure 3.33 Experimental results with middle input voltage.

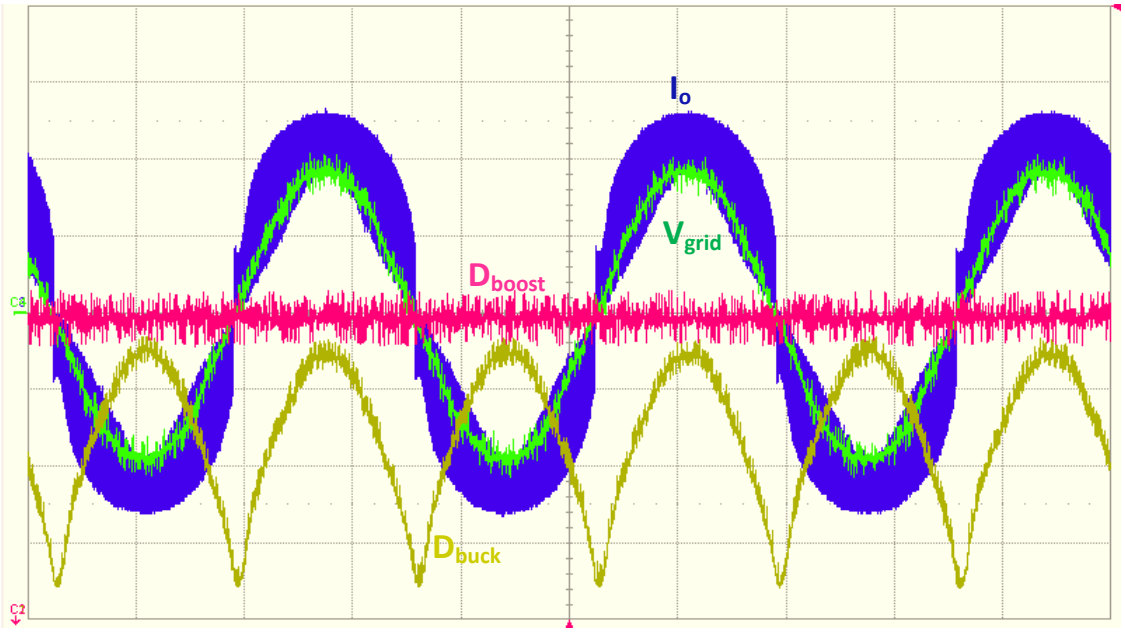


Figure 3.34 Experimental results with large input voltage.

Figure 3.35 shows efficiency curves with different input voltage under different power condition. The California Energy Commission (CEC) efficiency of a PV inverter could be calculated as below.

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (3.51)$$

Thus this test-bed inverter has a CEC efficiency of 97.4%.

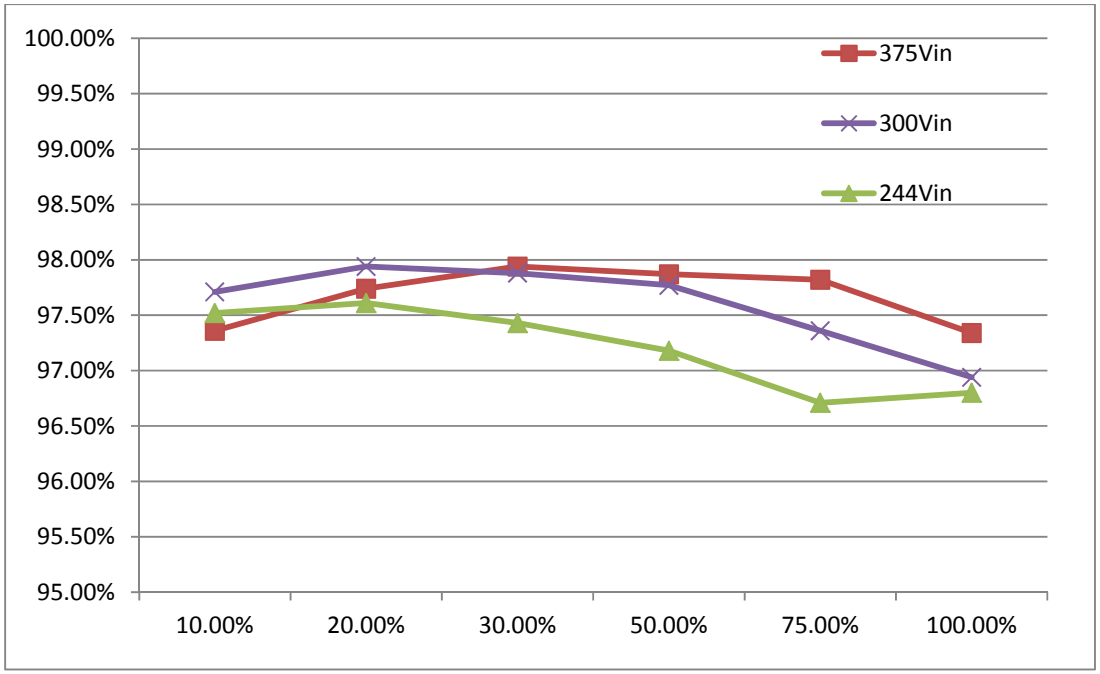


Figure 3.35 Efficiency curves of different input voltage under different load condition.

Testing with conventional control methods with constant voltages on C_L has also been conducted. Figure 3.36 shows efficiency comparisons of the proposed inverter and the traditional inverter under different input and load condition. The results demonstrate the proposed inverter can improve up to 2% in efficiency especially at light power condition, because the current is small and the switching losses become dominant in this case. During heavy power condition, the current becomes large and the conduction losses become dominant. Nonetheless, the proposed inverter still performs better than the conventional one. Nearly a 1% improvement in efficiency is measured in the heavy power condition.

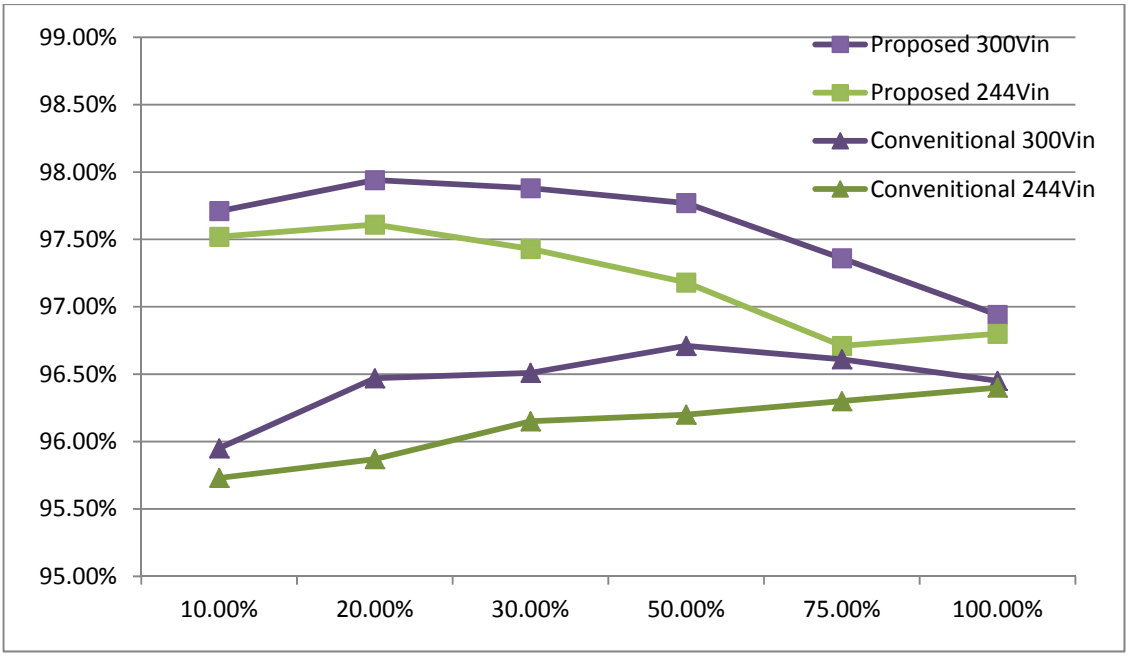


Figure 3.36 Efficiency comparisons of the proposed inverter and the traditional inverter under different input and load condition.

3.6 Summary

The averaged models for both modes have been established, which is the foundation for the controller design and optimization. After analyzing its model, it is known that if L_1 can be reduced, the double-pole position, which is considered as the frequency wall of bandwidth, will be pushed to higher frequency. Moreover, the gain will increase as well. Also, the Q factor will be reduced accordingly, which benefits the high bandwidth design for the boost mode. However, decreasing L_2 will keep the same double-pole position and have higher Q factor, which won't help controller design. As a result, small L_1 and large L_2 are preferred from the design point of view.

Because small L_1 is preferred for easier controller design, an interleaved-boost-cascaded-with-buck (IBCB) converter is proposed to increase the resonant pole frequency by the use of smaller boost inductor value. As a result, the control loop bandwidth can be pushed further up to enhance the robustness of the complete system and helps the system be controlled easier.

The proposed circuit along with its controller has been designed, simulated, and tested with a hardware prototype. Finally, the results indicate that the efficiency of the proposed solution is up to 2% higher than the conventional solution under the same condition and its tested CEC efficiency is 97.4%.

Chapter 4:
Advanced Double-Carrier based SPWM Control

In the previous chapters, an offset of the sawtooth carrier right on the top of the buck mode PWM modulator needs to be applied to boost mode in order to achieve smooth waveform in transition between boost and buck modes. Based on the similar concept, with different magnitudes and/or different frequencies for these two carriers, another three advanced double-carrier based SPWM modulation methods are proposed in this chapter. They help to further improve the efficiency and/or increase the bandwidth and gain.

4.1 Double-Carrier with Different Frequencies

From 3.3, small boost inductance L_1 *and* L_2 and large buck inductance L_o help compensator design. Thus, it is good to increase the carrier frequency for boost mode and reduce the carrier frequency for buck mode as shown in Figure 4.1. Figure 4.2 and Figure 4.3 illustrate a digital implementation. In this method, the same current ripple can be obtained by enlarging *Lo* and reducing L_1 *and* L_2. If only the carrier frequency for buck mode is reduced and the carrier frequency for boost mode is kept the same, switching loss can be reduced. However, since the inductance L_o needs to be increased, copper loss

introduced by this inductor may increase as well. As a result, the frequency should be selected by compromising between switching loss, core loss and copper loss.

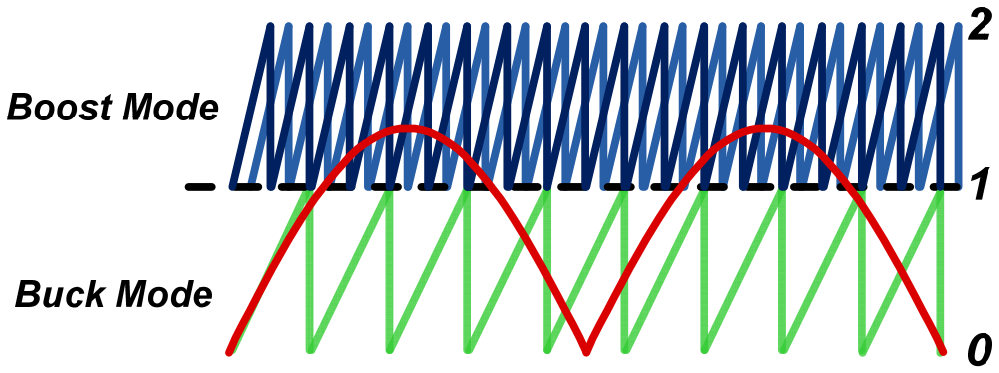


Figure 4.1 Double-carrier with different frequencies in analog control.

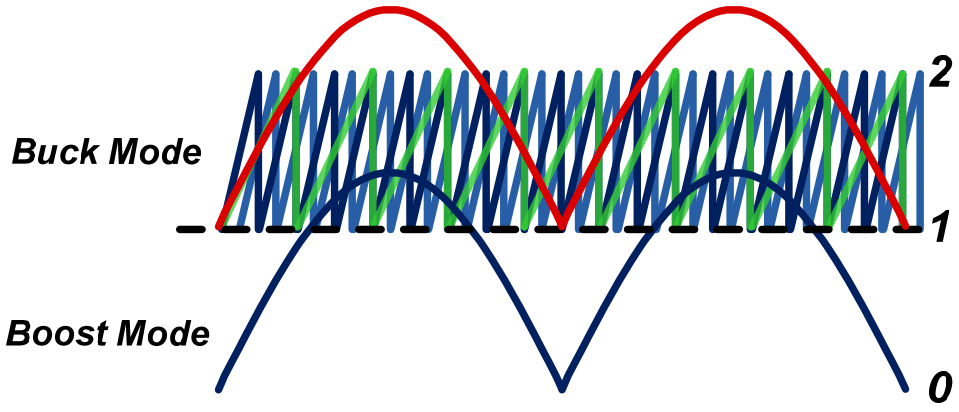


Figure 4.2 Double-carrier with different frequencies in digital control.

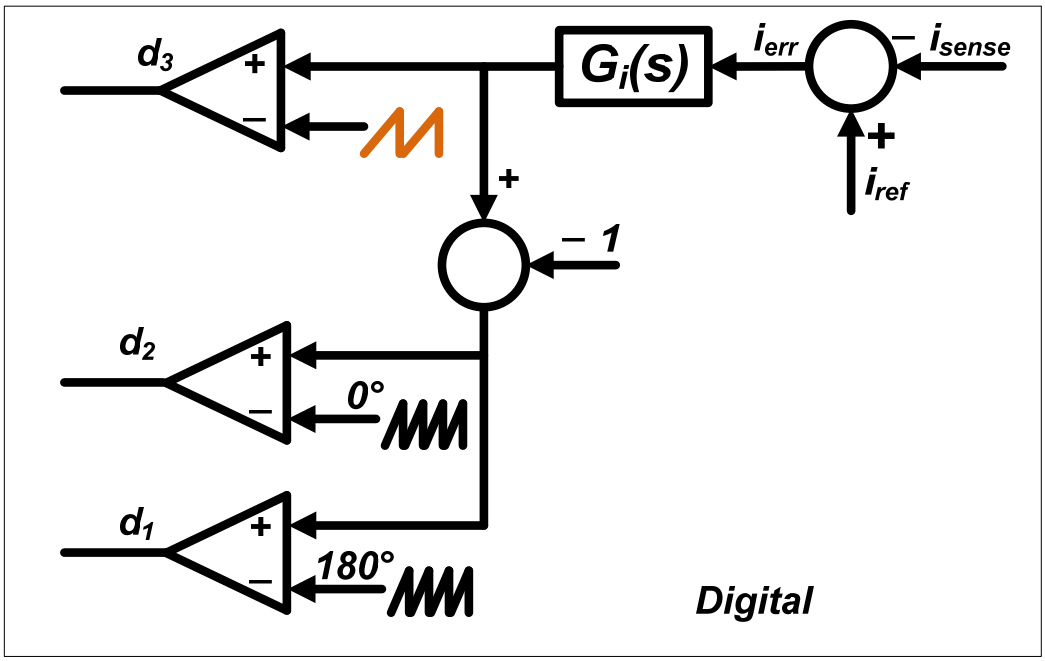


Figure 4.3 Digital control diagram for double-carrier with different frequencies.

Figure 4.4 and Figure 4.5, respectively, show the analog control and digital circuit in PSIM. The only difference with these figures and Figure 3.21 and Figure 3.22 is that the carrier frequency for the buck switch S_3 has been reduced. Figure 4.6 shows simulation results using analog control and digital control, respectively. In order to have the same current ripple, the inductance needs to be increased properly. As a result, these simulations results are the same as the ones shown in Figure 3.23 and Figure 3.24. These simulation results verify that both control methods work for the proposed dual - mode inverter.

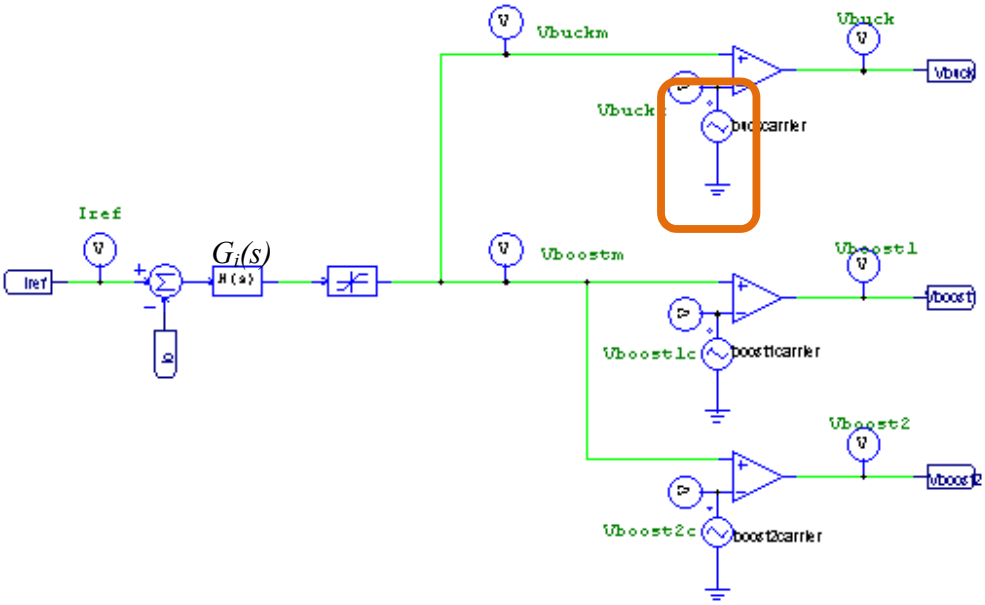


Figure 4.4 Analog control for smooth transition between modes.

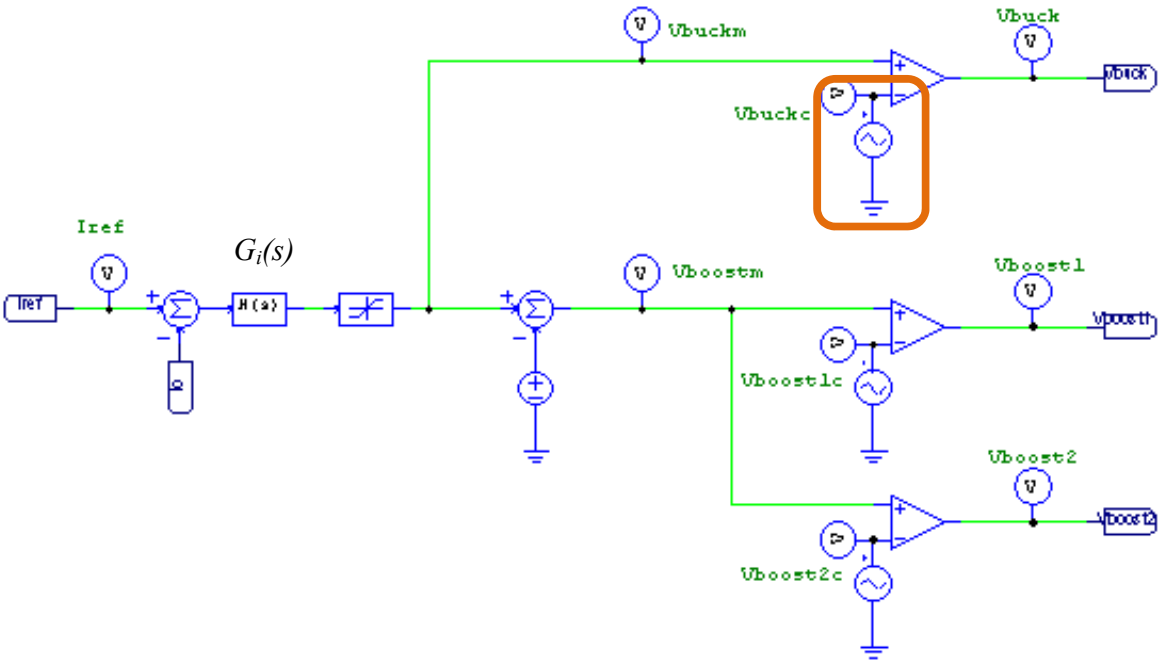
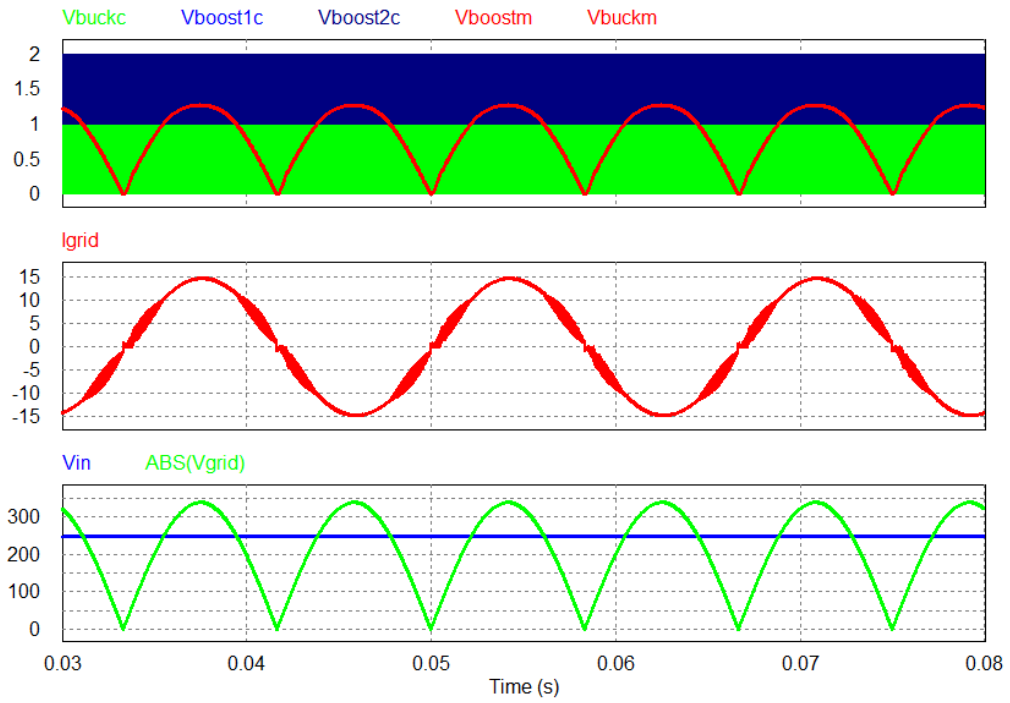
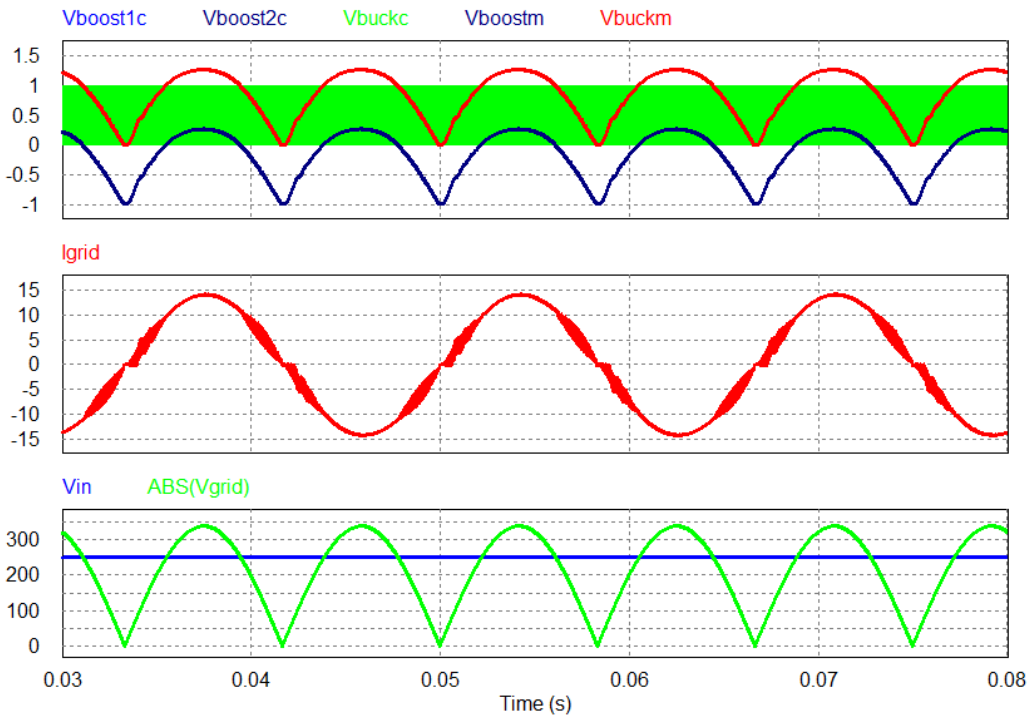


Figure 4.5 Digital control for smooth transition between modes.


Vbuckc
Vboost1c
Vboost2c
Vboostm
Vbuckm
2
1.5
1
0.5
0
Igrid
15
10
5
0
-5
-10
-15
Vin
ABS(Vgrid)
300
200
100
0
0.03
0.04
0.05
0.06
0.07
0.08
Time (s)

(a)


Vboost1c
Vboost2c
Vbuckc
Vboostm
Vbuckm
1.5
1
0.5
0
-0.5
-1
Igrid
15
10
5
0
-5
-10
-15
Vin
ABS(Vgrid)
300
200
100
0
0.03
0.04
0.05
0.06
0.07
0.08
Time (s)

(b)

Figure 4.6 Simulation results of double-carrier with different frequencies: (a) analog control; (b) digital control.

4.2 Double-Carrier with Different Magnitudes

Also from Chapter 3.3, once the compensator works for boost mode, it will automatically work for buck mode because of buck converter's characteristics. This gives the possibility of implementing a universal controller for boost mode and buck mode, with the two modes sharing the same compensator as shown in Figure 3.18. However, for the rectified sinusoidal waveform, there are many harmonics at the zero crossing, which require wide control loop bandwidth and high gain to compensate. Thus an advanced double-carrier based SPWM with different carrier magnitudes is proposed, as shown in Figure 4.7. If the buck mode needs to have k times the gain of boost mode, the boost carrier's magnitude needs to be k times that of buck mode. The distortion of the compared rectified sinusoidal waveform is due to the different magnitude of these two modes. In order to have the correct duty cycle, this comparing signal will adaptively become distorted with the carrier magnitudes.

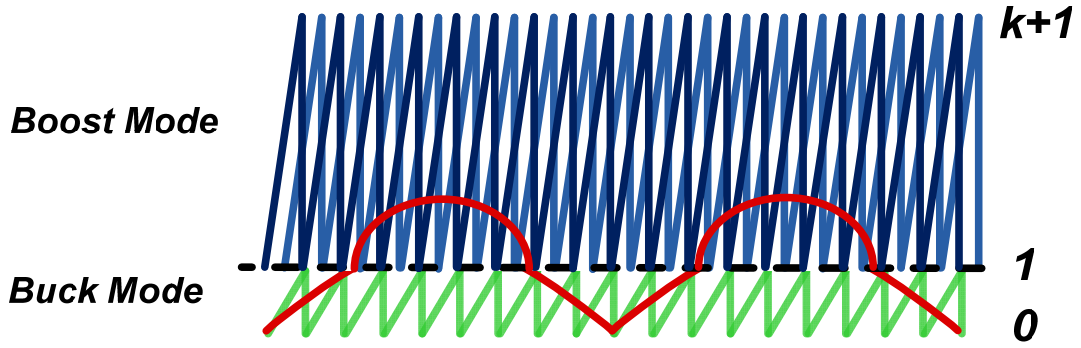


Figure 4.7 Double-carrier with different magnitudes.

In Figure 4.8, $G_i(s)$ is the compensator gain, FM is the PWM modulation gain, and $G_d(s)$ is the control-to-output transfer function. Thus, the loop gain can be expressed as (3.51).

$$T = G_d \cdot G_i \cdot FM \tag{3.1}$$

where

$$FM = \frac{1}{V_m} \tag{3.2}$$

V_m is the magnitude of the carrier.

Thus, for boost mode, its loop gain is

$$T_{boost} = G_d \cdot G_i \cdot \frac{1}{k} \tag{3.3}$$

For buck mode, its loop gain is

$$T_{buck} = G_d \cdot G_i \cdot 1 \tag{3.4}$$

Thus,

$$T_{buck} = T_{boost} \cdot k \tag{3.5}$$

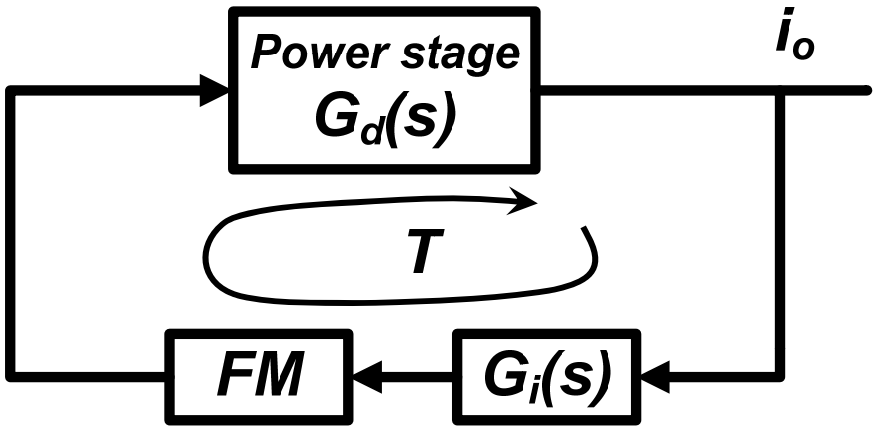


Figure 4.8 Control diagram of loop gain.

Thus, with different carrier magnitudes, the buck mode can obtain larger loop gain than the boost mode. In this method, the buck mode doesn't need to be constrained by the boost mode, and it can have wider bandwidth and higher gain. Figure 4.9 shows the loop gain of buck mode with the same carrier magnitude. Its bandwidth is around 2.5 kHz and its gain at 60 Hz is 65 dB. Figure 4.10 shows the loop gain of buck mode with five times smaller carrier magnitude than boost mode. Its bandwidth is around 6 kHz and its gain at 60 Hz is 78 dB. Table 4.1 shows a comparison.

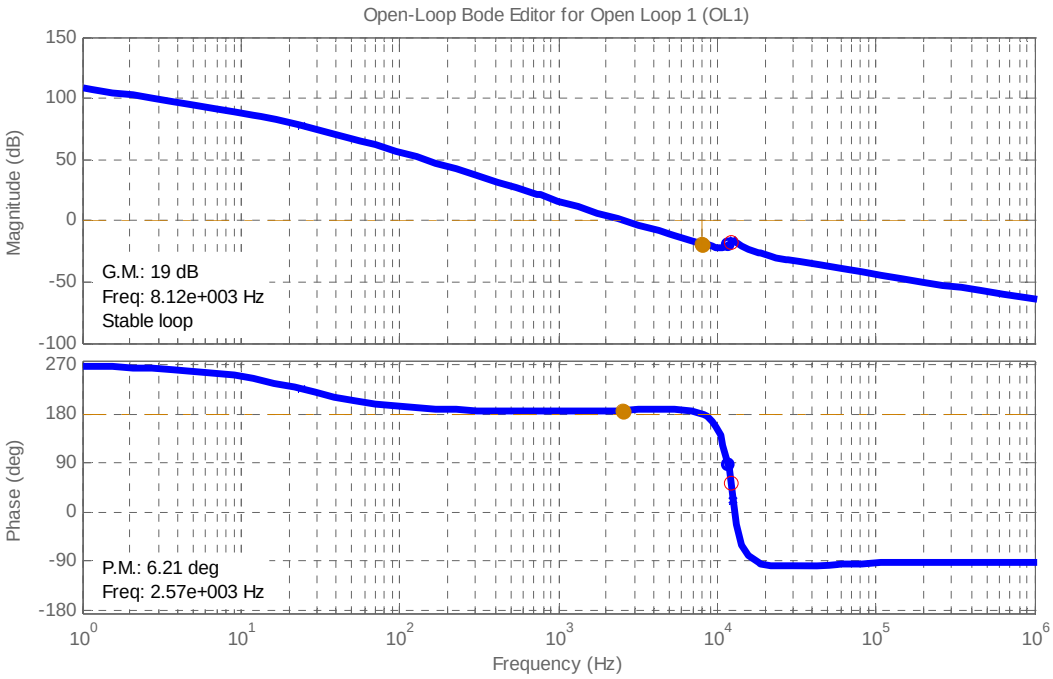


Figure 4.9 Loop gain of buck mode with the same carrier magnitude as boost mode.

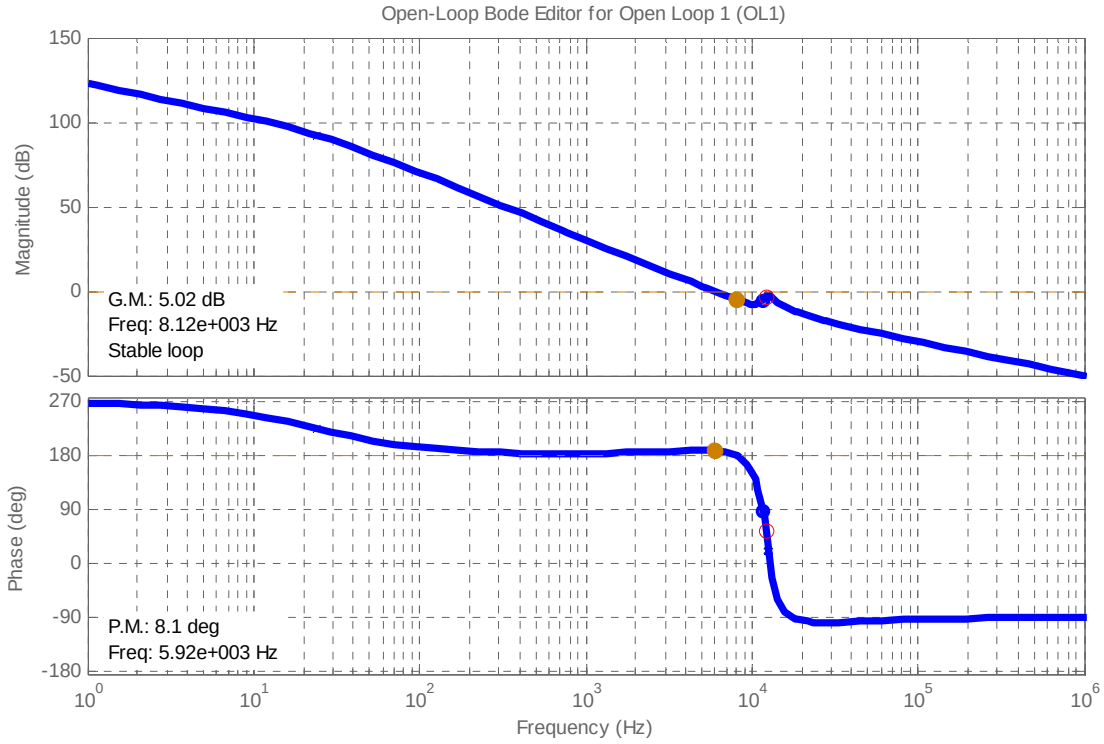


Figure 4.10 Loop gain of buck mode with five times smaller carrier magnitude than boost mode.

Table 4.1 Bandwidth and gain comparisons.

	Same carrier magnitude as boost mode	Five times smaller carrier magnitude than boost mode
Bandwidth	*2.5 kHz*	*6 kHz*
Gain @ 60 Hz	*65 dB*	*78dB*

Figure 4.11 and Figure 4.12 illustrate how to implement the method digitally. In digital control, the carriers for both modes are the same, and the compensated signal needs to deduct the carrier magnitude, which is 1 in a digital implementation, for the boost mode. The compensator increases by a factor of k to have a higher gain for the buck mode. As a result, the compensated signal needs to be reduced by a factor of k in order to have the same gain as analog control for this mode as shown in Figure 4.12.

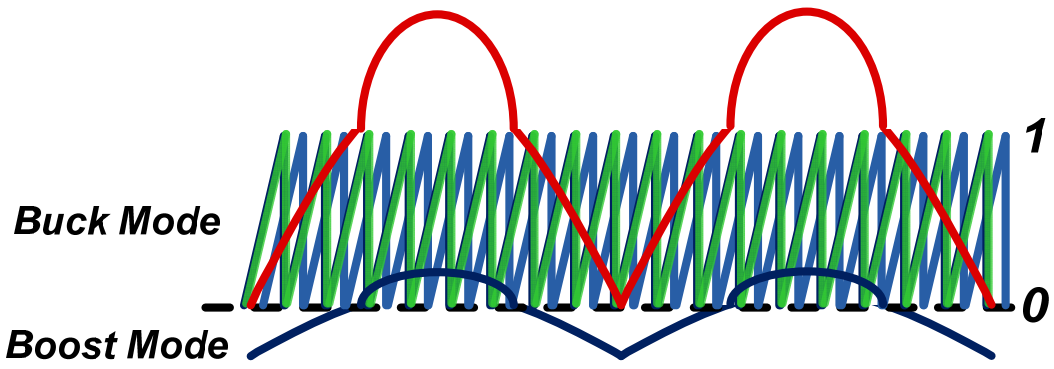


Figure 4.11 Double-carrier with different magnitudes in digital control.

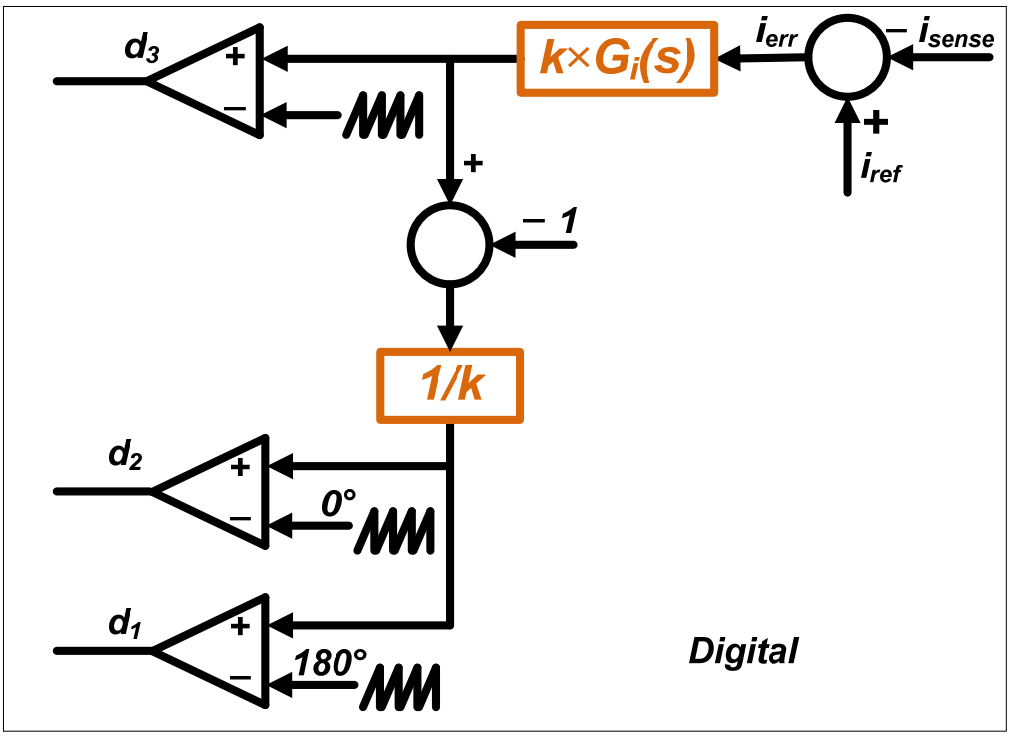


Figure 4.12 Digital control diagram for double-carrier with different magnitudes.

Figure 4.13 shows the analog control in PSIM. The only difference with Figure 3.21 is the carrier's magnitude for the boost switches S_1 *and* S_2 needs to be increased by k. Figure 4.14 shows the digital circuit in PSIM. The differences between this configuration with the one shown in Figure 3.22 are the compensator increases by a factor of k to have higher gain for the buck mode and the compensated signal needs to be reduced by a factor of k in order to have the same gain as analog control for the boost mode. In the simulation, k is chosen to be 5.

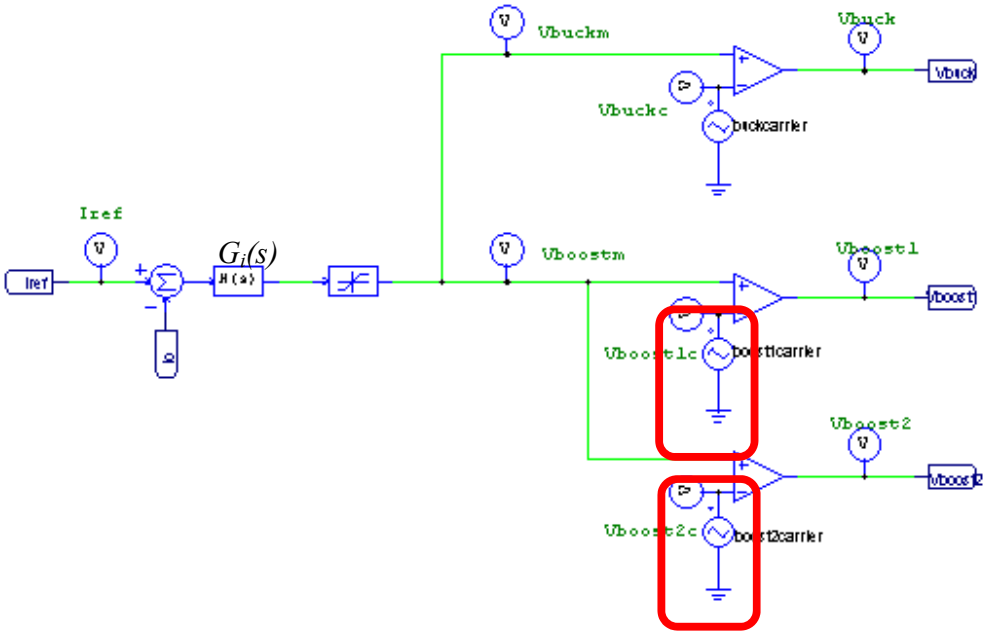


Figure 4.13 Analog control for smooth transition between modes.

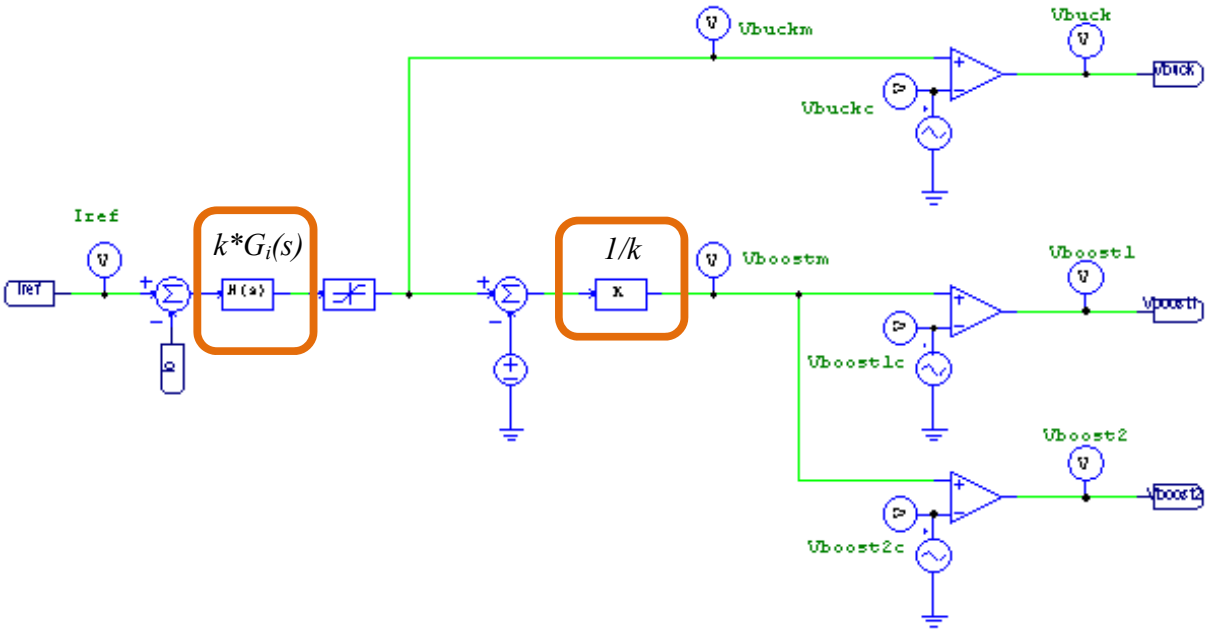
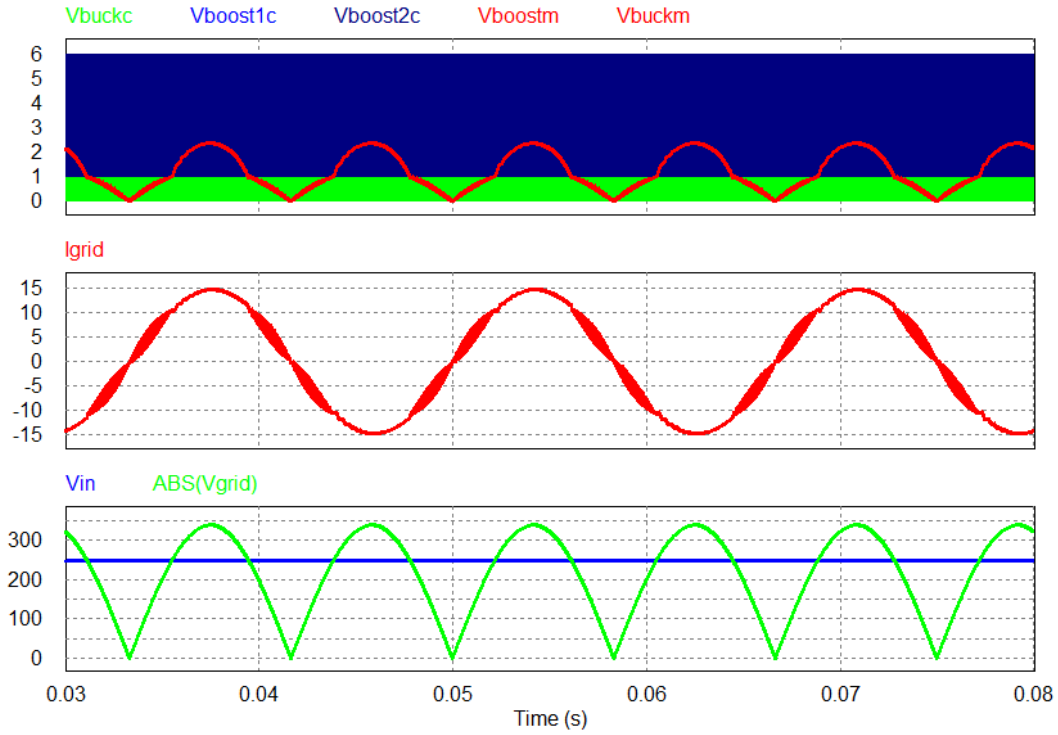
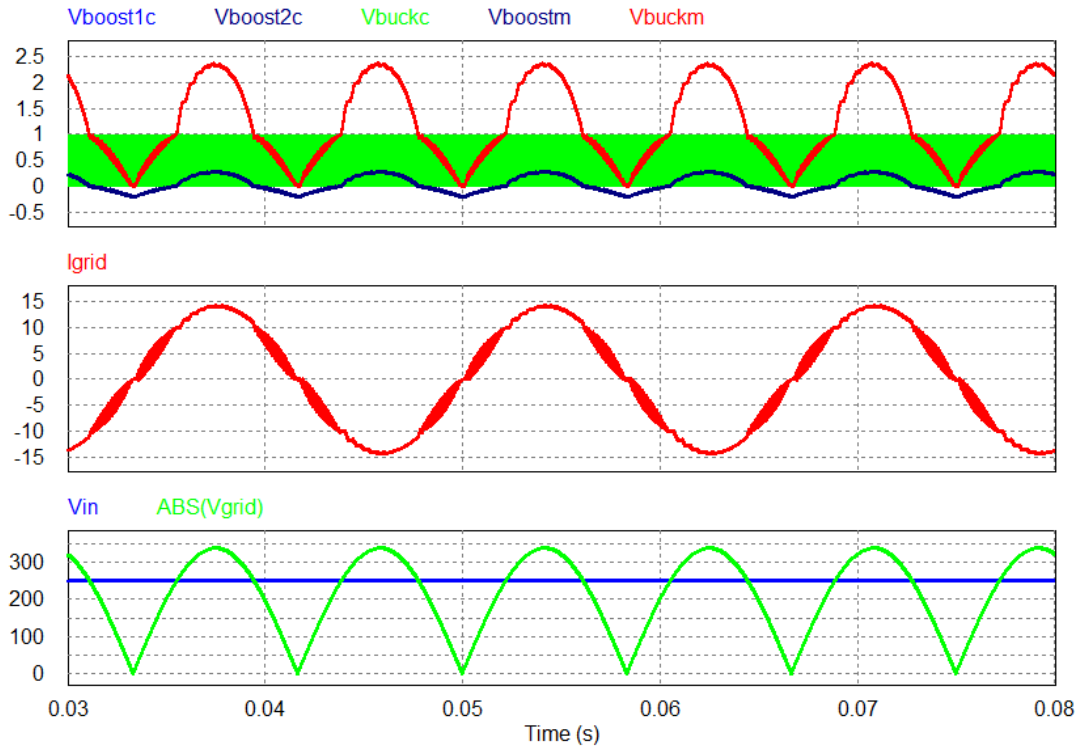


Figure 4.14 Digital control diagram for double-carrier with different magnitudes.

Figure 4.15 shows simulation results using analog control and digital control respectively. These simulation results verify that both control methods work for the proposed dual - mode inverter. Because of the higher compensator gain for the buck mode, the output current I_{grid} performs much better than in the previous control method, especially near zero - crossing point.



(a)



(b)

Figure 4.15 Simulation results of double-carrier with different magnitudes: (a) analog control; (b) digital control.

4.3 Double-Carrier with Different Frequencies and Magnitudes

Based on the previous two modulation methods, it is straightforward to combine these two modulation methods and take the advantages of both. Figure 4.16 illustrates this modulation method. The carrier for the boost mode is still on the top of the carrier for the buck mode. The carrier for buck mode has a different frequency and magnitude than that for the boost mode. As a result, the switching loss in the buck mode can be reduced and the buck mode obtains wide bandwidth and high gain.

Figure 4.17 and Figure 4.18 illustrate how to implement this method digitally.

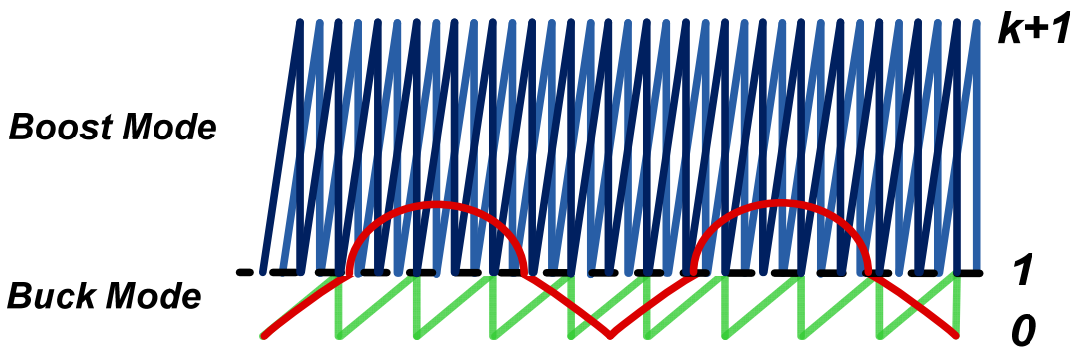


Figure 4.16 Double-carrier with different frequencies and magnitudes.

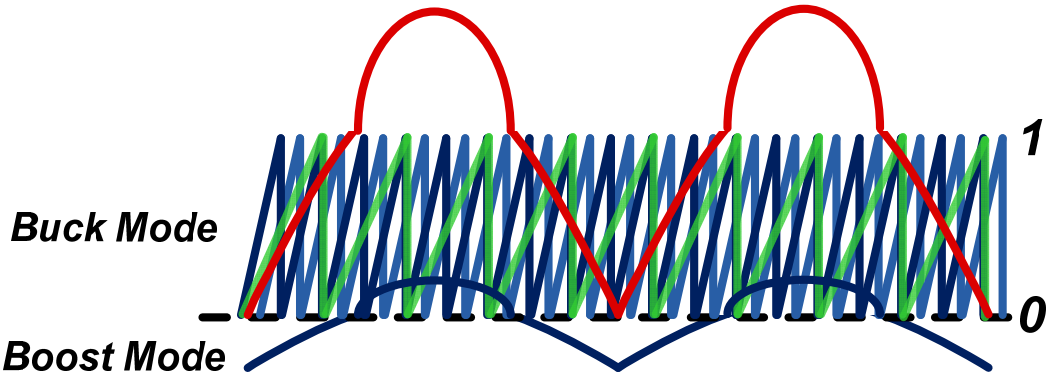


Figure 4.17 Double-carrier with different frequencies and magnitudes in digital control.

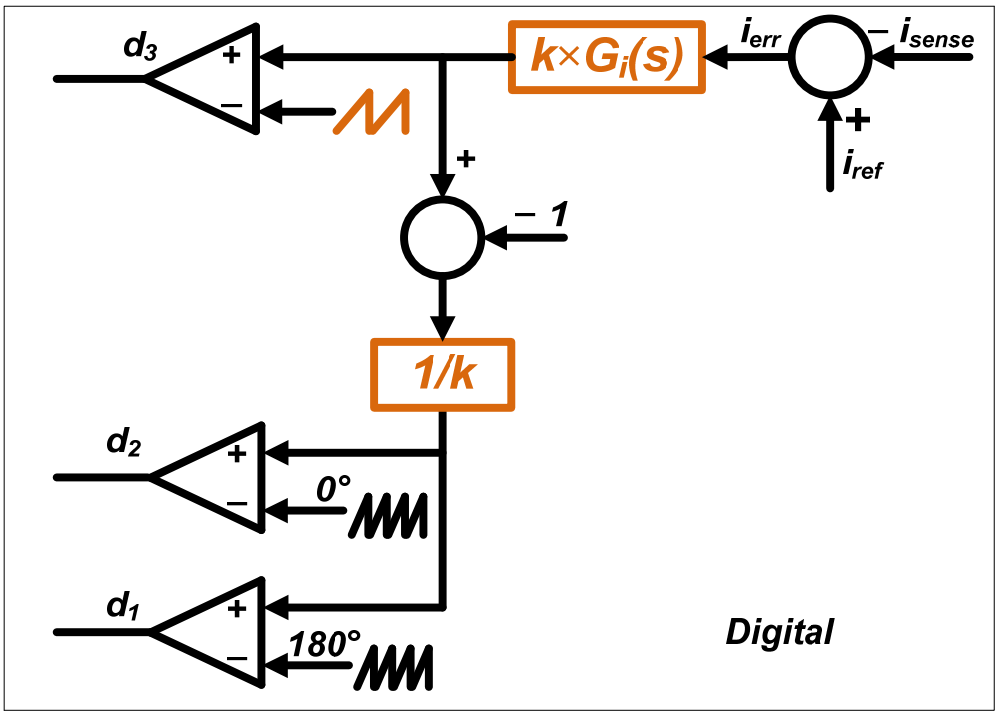


Figure 4.18 Digital control diagram for double-carrier with different frequencies and magnitudes.

Figure 4.19 and Figure 4.20, respectively show the analog control and digital circuit in PSIM. The only difference with Figure 4.13 and Figure 4.14 is that the carrier frequency for buck switch S_3 needs to be reduced. Figure 4.21 show the simulation results using analog control and digital control respectively. In order to have the same current ripple, the inductance needs to be increased properly. Hence, these simulation results are the same as the ones shown in Figure 4.15. These simulation results verify that both control methods work for the proposed dual - mode inverter.

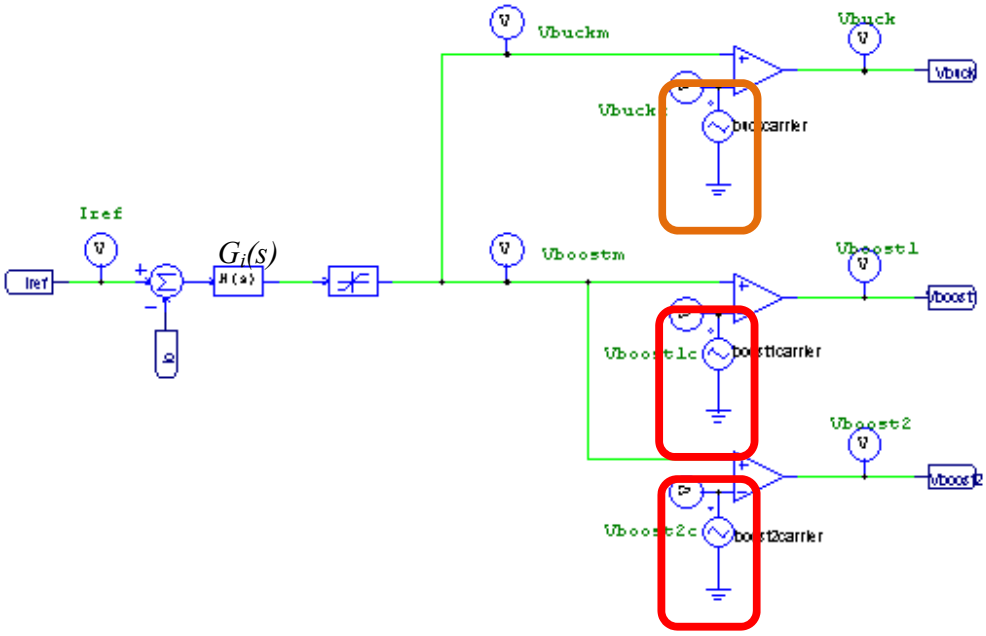


Figure 4.19 Analog control for smooth transition between modes.

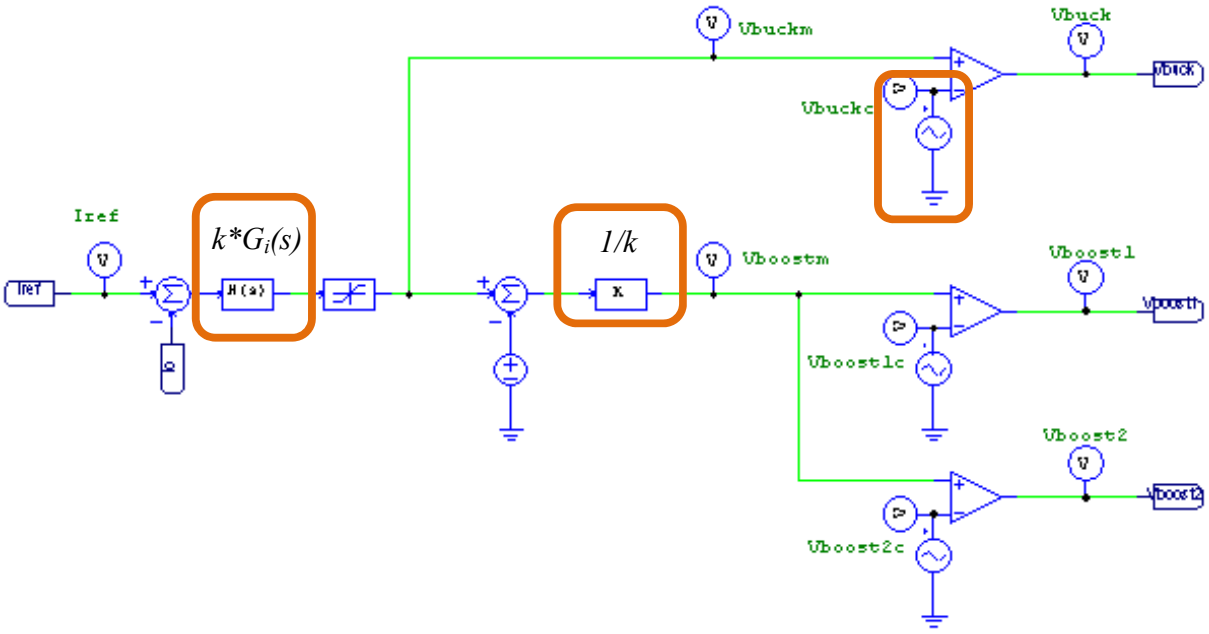
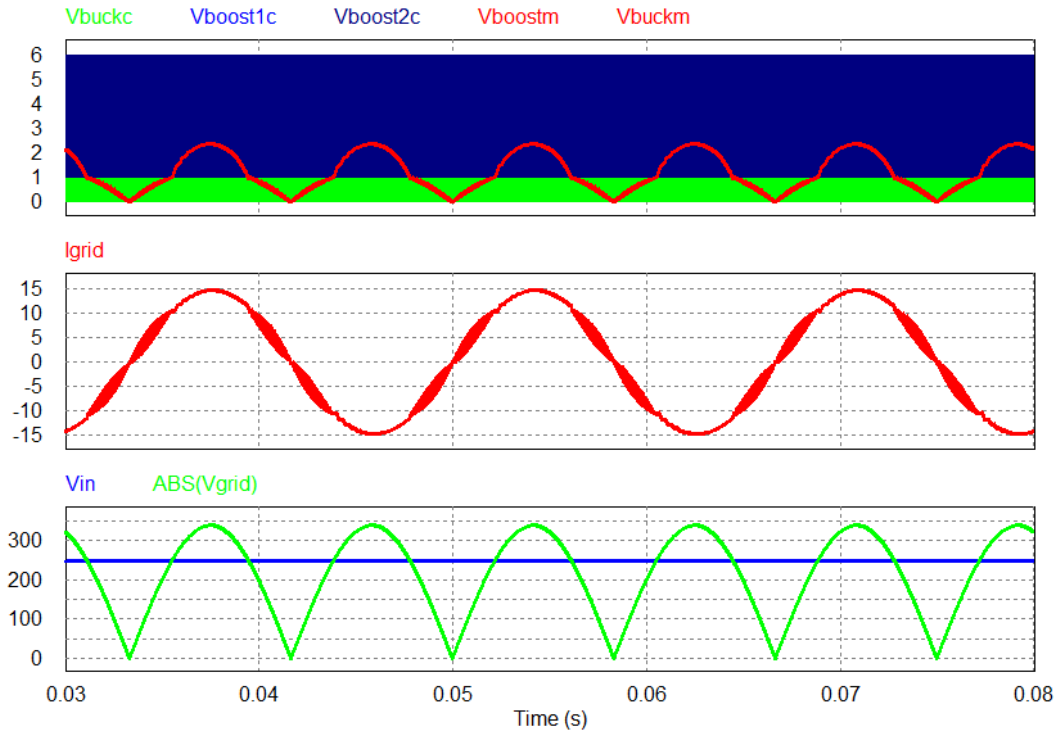
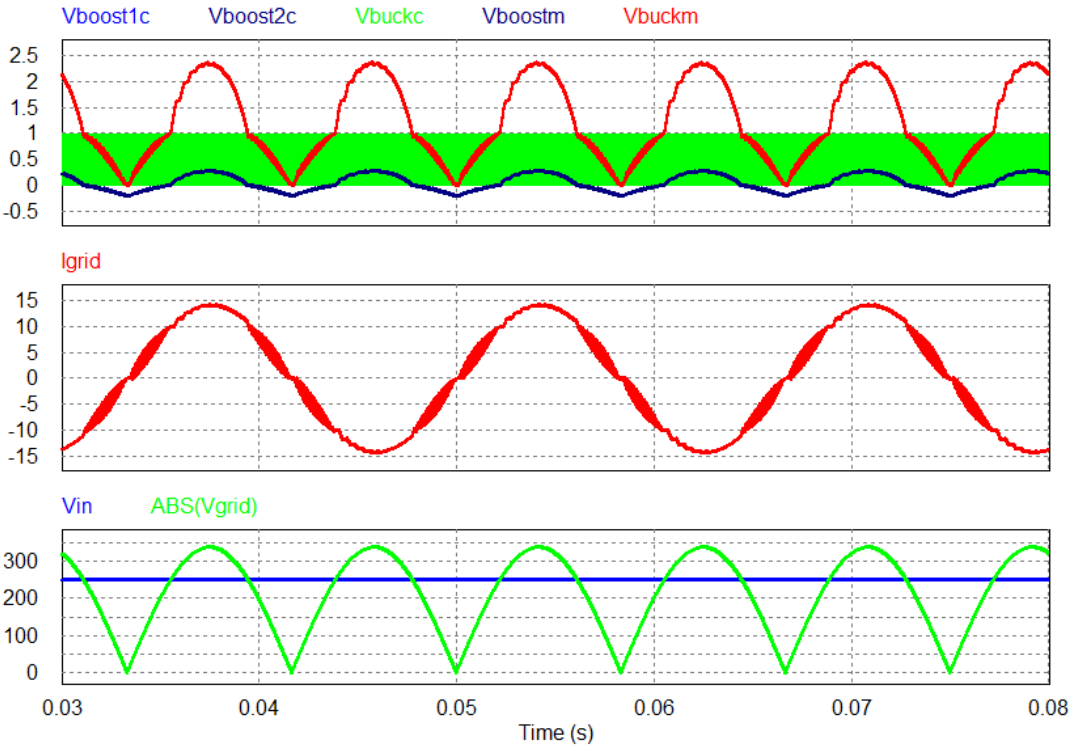


Figure 4.20 Digital control diagram for double-carrier with different magnitudes.


Vbuckc
Vboost1c
Vboost2c
Vboostm
Vbuckm
6
5
4
3
2
1
0
Igrid
15
10
5
0
-5
-10
-15
Vin
ABS(Vgrid)
300
200
100
0
0.03
0.04
0.05
0.06
0.07
0.08
Time (s)

(a)


Vboost1c
Vboost2c
Vbuckc
Vboostm
Vbuckm
2.5
2
1.5
1
0.5
0
-0.5
Igrid
15
10
5
0
-5
-10
-15
Vin
ABS(Vgrid)
300
200
100
0
0.03
0.04
0.05
0.06
0.07
0.08
Time (s)

(b)

Figure 4.21 Simulation results of double-carrier different frequencies and magnitudes: (a) analogy control; (b) digital control.

4.4 Summary

Based on the modulation method proposed in previous chapter, three advanced modulation methods are proposed. Double-carrier with different frequencies can help further improve the efficiency. Double-carrier with different magnitudes can help increase the bandwidth and gain. Double-carrier with different frequencies and magnitudes takes the advantages of both. Simulation verifies their function very well.

Chapter 5:
Proposed Other Dual - Mode Double - Carrier PV Inverters

In the previous chapters, a dual mode boost – buck converter based PV inverter was proposed, with a boost-buck type dc-dc converter as the first stage with regulated output inductor current. A full-bridge unfolding circuit with 50- or 60-Hz line frequency is applied to the dc-ac stage, unfolding the rectified sinusoidal current into a pure sinusoidal current. An interleaved boost is chosen for better performance and lower input current ripple. Since the circuit runs either in boost or buck mode, its first stage can be very efficient. For the second stage, because the unfolding circuit only operates at the line frequency and switches at zero voltage and current, switching loss can be omitted. It is observed that, for buck mode, there are many topologies can meet the same criteria, such as full bridge (FB), H5 inverter and dual buck (DB) inverter. In this chapter, three new dual - mode inverters are proposed. These proposed topologies either reduce the number of components or further improve the efficiency. The efficiencies and leakage currents of these inverters are compared.

5.1 Boost Cascaded with Full Bridge Inverter

The proposed boost - full bridge (FB) inverter is shown in Figure 5.1, in which the IGBTs covered by blue are operating in line frequency for selecting grid polarity as the same function of S_A - S_D in unfolding circuit in Figure 3.18. The MOSFETs covered

by yellow are operating at high switching frequency as the same function of S_3 in Figure 3.18.

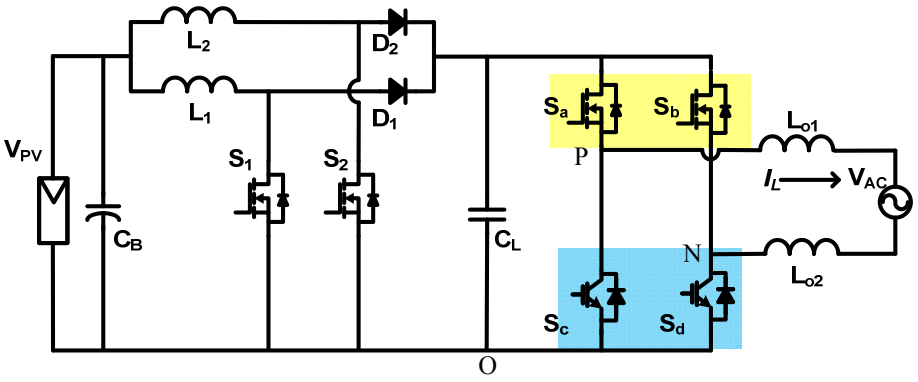


Figure 5.1 Boost-full bridge (FB) inverter.

Similar to the operation modes discussed 2.2.2, if the input voltage is lower than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are operating, and the MOSFETs covered by yellow are always on or off depends on the polarity of the grid.

If the input voltage is larger than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are off, and the MOSFETs covered by yellow are operating in high frequency as a normal unipolar full bridge inverter. Its PWM generation is shown in Figure 5.2.

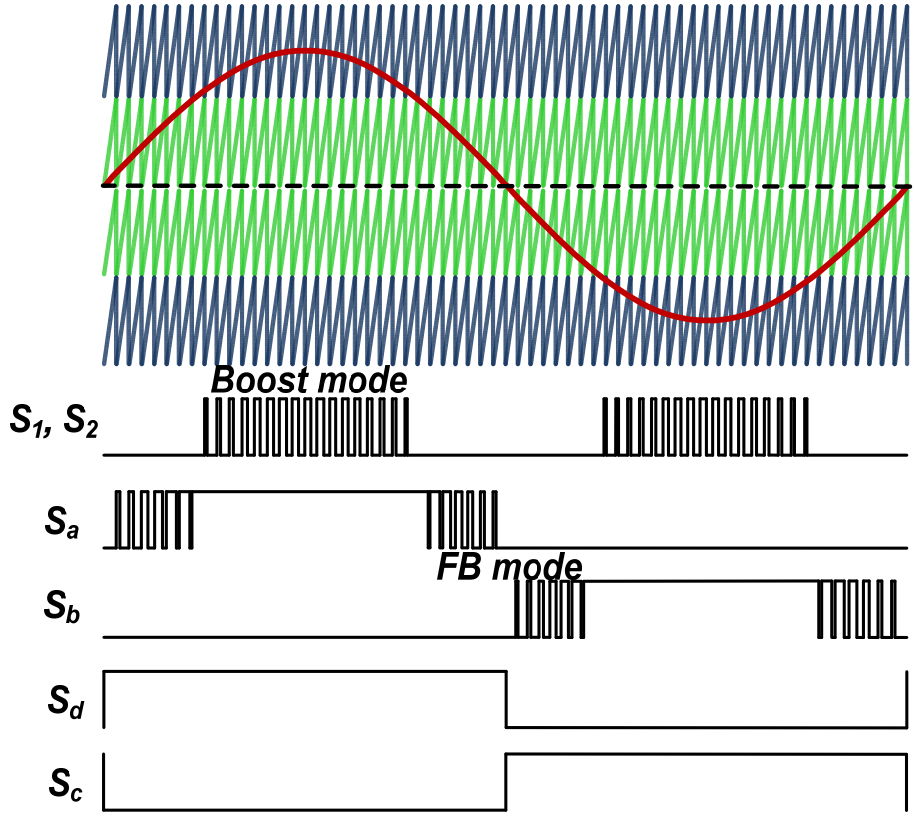


Figure 5.2 PWM generation of boost-full bridge (FB) inverter.

In Chapter 3.3, four switches are used in unfolding circuit for selecting the polarity of the grid. This boost - full bridge inverter saves two switches for polarity selection, which help save half of the conduction loss introduced by polarity selection switches. Also, the number of components can be reduced, which can help save the cost. However, since the free-wheeling diodes are the diodes in the same package with IGBTs, their reverse recovery may hurt the whole circuit's efficiency.

The two different operating modes and the non-constant middle link capacitor voltage as shown in Figure 2.16 and Figure 2.17 give the complication of calculating the loss in this type of inverters. Some details about calculations of loss are provided below.

If the input voltage range is set from *200 V* to *500 V*, under different input voltage condition, the angle and the voltage across the middle link capacitor can be found in (4.1) and (4.2) respectively.

$$\theta = \begin{cases} a\sin\left(\frac{V_{in}}{V_{opk}}\right) & if\ 200 \le V_{in} < 340 \\ \frac{\pi}{2} & if\ 340 \le V_{in} \le 500 \end{cases} \tag{4.1}$$

$$V_{CL}(\omega t) = \begin{cases} V_{opk}\sin(\omega t) & if\ 200 \le V_{in} < 340 \\ V_{in} & if\ 340 \le V_{in} \le 500 \end{cases} \tag{4.2}$$

Based on Figure 5.2, the loss in this inverter includes the loss in boost part, full bridge part and unfolding part as shown in (4.3).

$$\begin{aligned} P_{Loss} = {} & (P_{S1con} + P_{S1sw})\cdot 2 + (P_{D1con} + P_{D1rr})\cdot 2 + (P_{Sccon} + P_{Scsw})\cdot 2 \\ & + (P_{Dacon} + P_{Darr})\cdot 2 + (P_{Sacon} + P_{Sasw})\cdot 2 + P_{Lin} + P_{Lo} \end{aligned} \tag{4.3}$$

The loss in boost part can be calculated by (4.4) to (4.8).

$$P_{con\_boostmos} = \frac{1}{\pi}\cdot\left[\int_0^{\theta} 0\, d\omega t + \int_{\theta}^{\pi-\theta} \frac{\frac{2P_o}{V_{in}}\sin^2(\omega t)}{2}\cdot R_{dson}\frac{\frac{2P_o}{V_{in}}\sin^2(\omega t)}{2}\left(1-\frac{V_{in}}{V_{opk}\left|\sin(\omega t)\right|}\right)d\omega t\right] \tag{4.4}$$

$$P_{sw\_booston} = \left[t_r\cdot\frac{1}{\pi}\cdot\int_{\theta}^{\pi-\theta}\frac{\frac{2P_o}{V_{in}}\sin^2(\omega t)}{2}\cdot\frac{V_{CL}(\omega t)}{2}d\omega t + \frac{2}{3}\cdot C_{oss}\cdot V_{in}^2\cdot\left(1-\frac{2\theta}{\pi}\right)\right]\cdot f_{swboost} \tag{4.5}$$

$$P_{sw\_boostoff} = \left[t_f\cdot\frac{1}{\pi}\cdot\int_{\theta}^{\pi-\theta}\frac{\frac{2P_o}{V_{in}}\sin^2(\omega t)}{2}\cdot\frac{V_{CL}(\omega t)}{2}d\omega t\right]\cdot f_{swboost} \tag{4.6}$$

$$P_{con\_boostD} = \frac{1}{\pi}\cdot[2\cdot\int_0^{\theta}\frac{\frac{2P_o}{V_{in}}\cdot\sin^2(\omega t)}{2}\cdot[R_{ak}\cdot\frac{\frac{2P_o}{V_{in}}\cdot\sin^2(\omega t)}{2}+V_f]d\omega t + \int_{\theta}^{\pi-\theta}\frac{\frac{2P_o}{V_{in}}\cdot\sin^2(\omega t)}{2}\cdot[R_{ak}\cdot\frac{\frac{2P_o}{V_{in}}\cdot\sin^2(\omega t)}{2}+V_f]\frac{V_{in}}{V_{opk}\cdot|\sin(\omega t)|}d\omega t] \quad (4.7)$$

$$P_{Lin} = 2\cdot\frac{1}{\pi}\cdot\int_0^{\pi}(\frac{\frac{2P_o}{V_{in}}\cdot\sin^2(\omega t)}{2})^2\cdot R_{L1}d\omega t \quad (4.8)$$

The loss in full bridge part can be calculated by (4.9) to (4.13).

$$P_{Con\_buckmos} = \frac{1}{\pi}[2\cdot\int_0^{\theta}\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\cdot R_{dson}\cdot\left(\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\right)\cdot M\sin(\omega t)d\omega t + \int_{\theta}^{\pi-\theta}\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\cdot R_{dson}\cdot\left(\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\right)d\omega t] \quad (4.9)$$

$$P_{sw\_buckon} = \left(t_r\cdot\frac{V_{in}}{2}\frac{1}{\pi}2\cdot\int_0^{\theta}\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)d\omega t + \frac{2}{3}\cdot C_{oss}\cdot V_{in}^2\cdot\frac{2\theta}{\pi}\right)\cdot f_{swbuck} \quad (4.10)$$

$$P_{sw\_buckoff} = t_f\cdot\frac{V_{in}}{2}\frac{1}{\pi}2\cdot\int_0^{\theta}\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)d\omega t\cdot f_{swbuck} \quad (4.11)$$

$$P_{con\_buckD} = \frac{2}{\pi}\cdot\int_0^{\theta}\frac{\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)}{2}\cdot[R_{ak}\cdot\frac{\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)}{2}+V_f]\cdot\left[1-M|\sin(\omega t)|\right]d\omega t \quad (4.12)$$

$$P_{Lo} = \frac{1}{\pi}\cdot\int_0^{\pi}\left[\frac{P_o}{V_{orms}}\sqrt{2}\sin^2(\omega t)\right]^2\cdot R_{Lo}d\omega t \quad (4.13)$$

IGBTs $S_{\backslash c}$ and S_d operate at line frequency; so, this part only includes conduction loss.

$$P_{con\_IGBT} = \frac{1}{2\pi}\int_0^{\pi}\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\left[R_{ce}\left(\frac{P_o}{V_{orms}}\cdot\sqrt{2}\sin(\omega t)\right)+V_t\right]d\omega t \quad (4.14)$$

Then the efficiency can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{4.15}$$

Figure 5.3 shows the simulation results of the proposed topology. I_{grid} is the current sent to the grid. V_{boost}, S_a, S_b, S_c and S_d represent the PWM signals for the corresponding switches. V_{boostc}, V_{buckc} *and* $ABS(V_m)$ represent boost carrier, buck carrier and the compensated signal respectively. Both the operation modes and modulation methods are well illustrated in the simulation results.

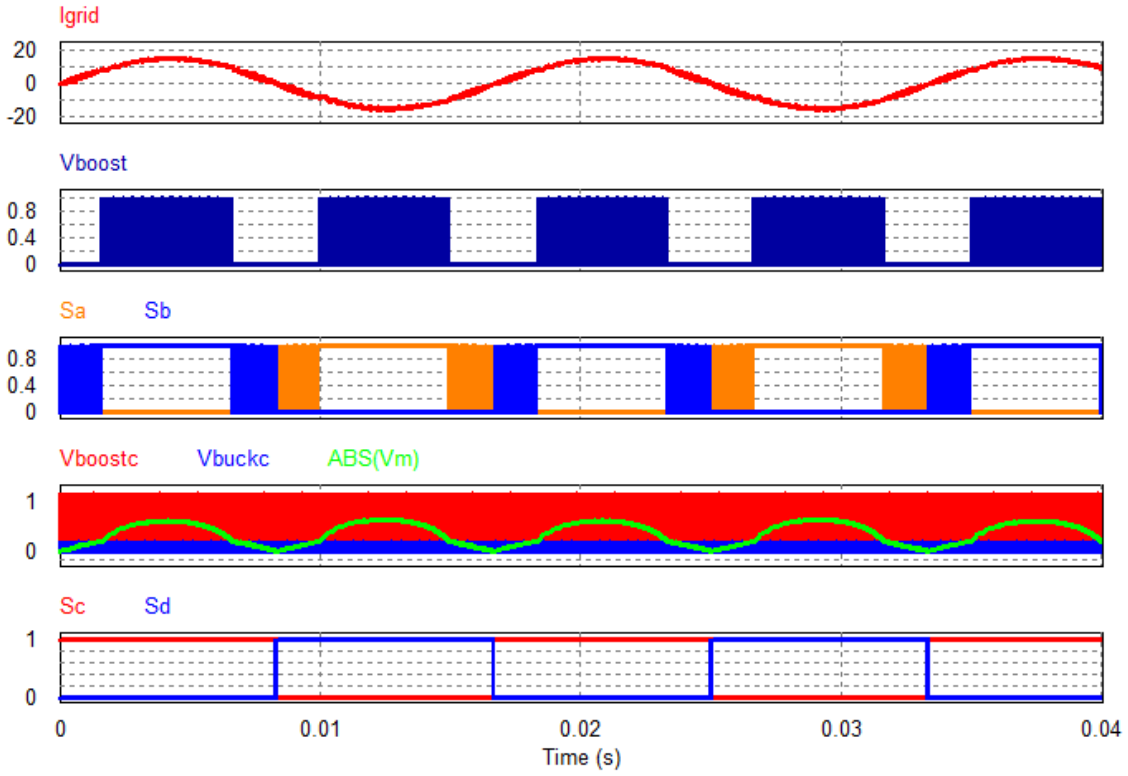


Figure 5.3 Simulation results of boost with full bridge.

5.2 Boost Cascaded with H5 Inverter

H5 is the inverter introduced in 2.1. Similarly to 5.1, the proposed boost - H5 inverter is shown in Figure 5.4, in which the IGBTs covered by blue are operating in line frequency for selecting grid polarity as the same function of S_A - S_D in unfolding circuit in Figure 3.18. The MOSFETs covered by yellow are operating at high switching frequency as the same function of S_3 in Figure 3.18.

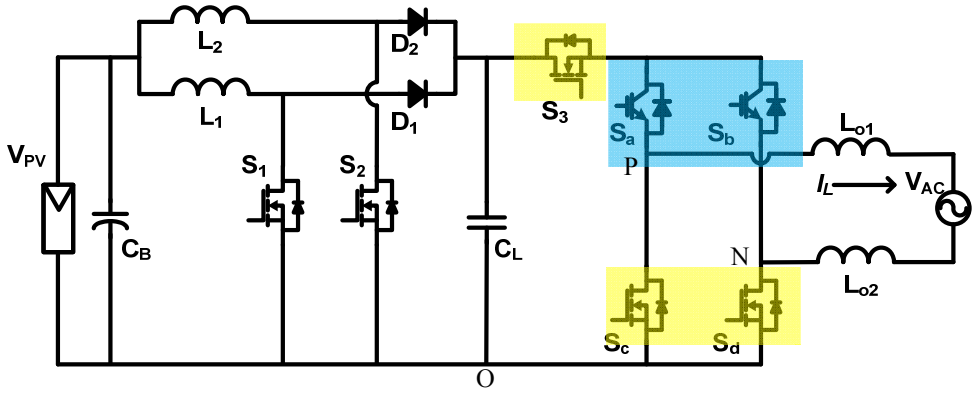


Figure 5.4 Boost-H5 inverter.

Similar to the operation modes discussed in Chapter 2.2.2, if the input voltage is lower than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are operating, and S_3 is always on. The other two MOSFETs covered by yellow S_c and S_d are on and off based on the polarity of the grid.

If the input voltage is larger than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are off, and the MOSFETs covered by yellow are operating in high frequency working as a H5 inverter. Its PWM generation is shown in Figure 5.5.

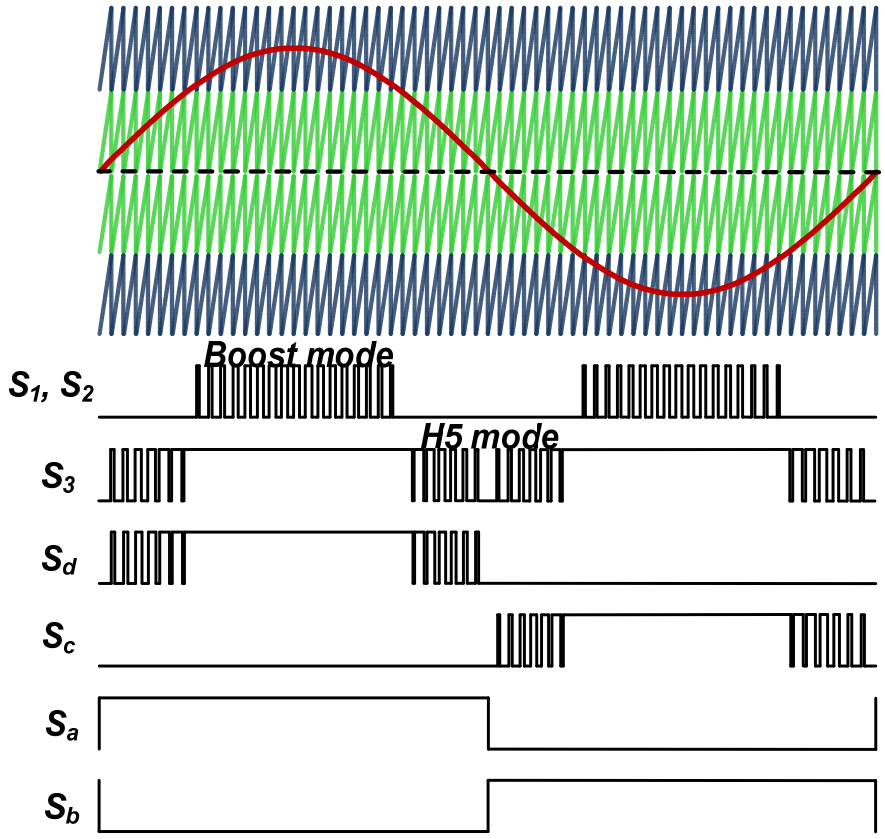


Figure 5.5 PWM generation of boost-H5 inverter.

In Chapter 3.3, four switches are used in unfolding circuit for selecting the polarity of the grid. In this boost - H5 inverter, one diode is saved and the diodes in the same package with IGBTs are also utilized. Because it can reduce the voltage stress for each component, its switching loss is greatly reduced and, thus, it still can achieve high efficiency.

Based on Figure 5.5, the loss in this inverter includes the loss in boost part, H5 part and unfolding part as shown in (4.16).

$$P_{Loss} = \left(P_{S1con} + P_{S1sw}\right)\cdot 2 + \left(P_{D1con} + P_{D1rr}\right)\cdot 2 + \left(P_{S3con} + P_{S3sw}\right) + \left(P_{Sccon} + P_{Scsw}\right)\cdot 2 + \left(P_{Dacon} + P_{Darr}\right)\cdot 2 + \left(P_{Sacon} + P_{Sasw}\right)\cdot 2 + P_{Lin} + P_{Lo} \quad (4.16)$$

Same as Chapter 5.1 , the loss in boost part can also be calculated by (4.4) to (4.8).

The conduction loss is the same as in full bridge part calculated as (4.9). The switching loss is slightly different since the voltage stress is half of that in full bridge inverter, and they can be calculated by (4.17) and (4.18).

$$P_{sw\_buckon} = \left(t_r \cdot \frac{V_{in}/2}{2} \frac{1}{\pi} 2 \cdot \int_0^{\theta} \frac{P_o}{V_{orms}} \cdot \sqrt{2} \sin(\omega t)\, d\omega t + \frac{2}{3} \cdot C_{oss} \cdot \frac{(V_{in}/2)^2}{2} \cdot \frac{2\theta}{\pi} \right) \cdot f_{swbuck} \tag{4.17}$$

$$P_{sw\_buckoff} = t_f \cdot \frac{V_{in}/2}{2} \frac{1}{\pi} 2 \cdot \int_0^{\theta} \frac{P_o}{V_{orms}} \cdot \sqrt{2} \sin(\omega t)\, d\omega t \cdot f_{swbuck} \tag{4.18}$$

The loss in IGBT which operates at line frequency can also be calculated as (4.14).

Then the efficiency can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{4.19}$$

Figure 5.6 shows the simulation results of the proposed topology. I_{grid} is the current sent to the grid. V_{boost}, S_3, S_a, S_b, S_c and S_d represent the PWM signals for the corresponding switches. V_{boostc}, V_{buckc} *and* $ABS(V_m)$ represent boost carrier, buck carrier and the compensated signal respectively. Both the operation modes and modulation methods are well illustrated in the simulation results.

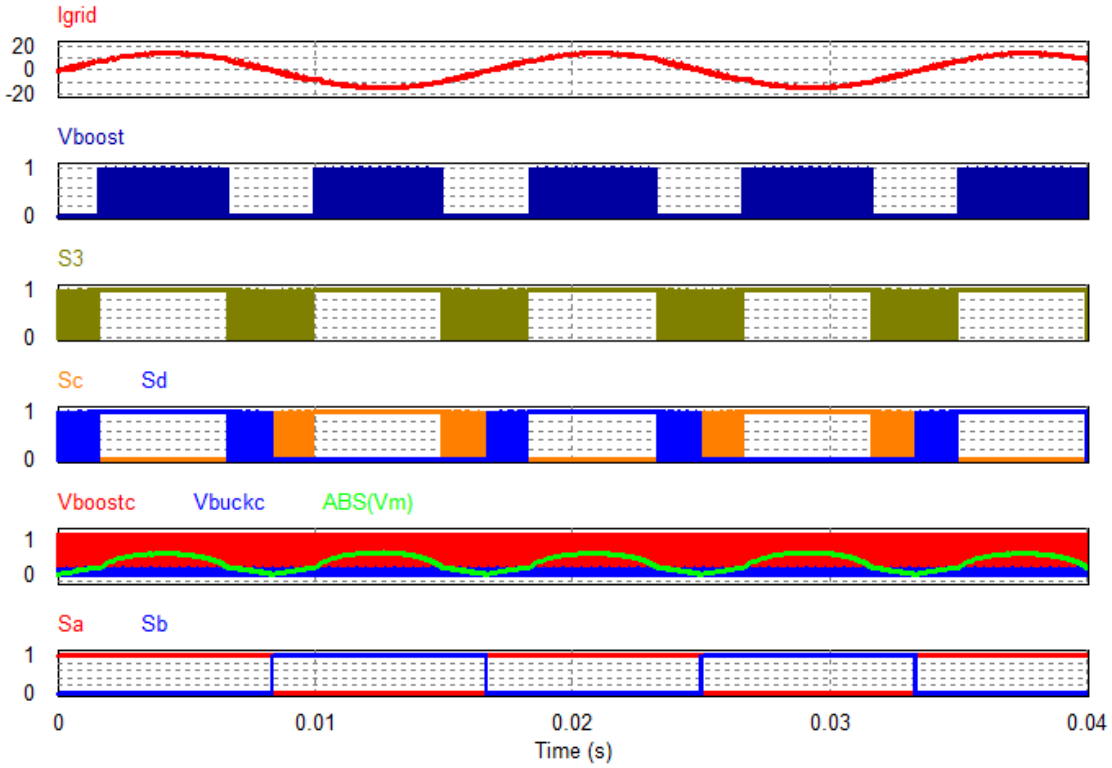


Figure 5.6 Simulation results of boost with H5.

5.3 Boost Cascaded with Dual Buck Inverter

Similarly to Chapter 5.1 and 5.2, the proposed boost - dual buck (DB) inverter is shown in Figure 5.7, in which the IGBTs covered by blue are operating in line frequency for selecting grid polarity as the same function of S_A - S_D in unfolding circuit in Figure 3.18. The MOSFETs covered by yellow are operating at high switching frequency as the same function of S_3 in Figure 3.18.

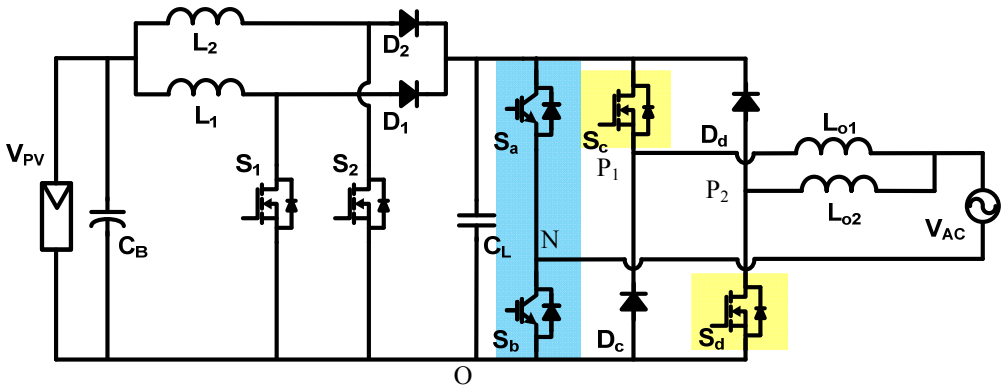


Figure 5.7 Boost-dual buck (DB) inverter.

Similar to the operation modes discussed in Chapter 2.2.2, if the input voltage is lower than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are operating, and the MOSFETs covered by yellow are on and off based on the polarity of the grid.

If the input voltage is larger than the rectified instantaneous grid voltage, the switches in the interleaved boost part S_1 and S_2 are off, and the MOSFETs covered by yellow are operating in high frequency working as a dual buck inverter. Its PWM generation is shown in Figure 5.8.

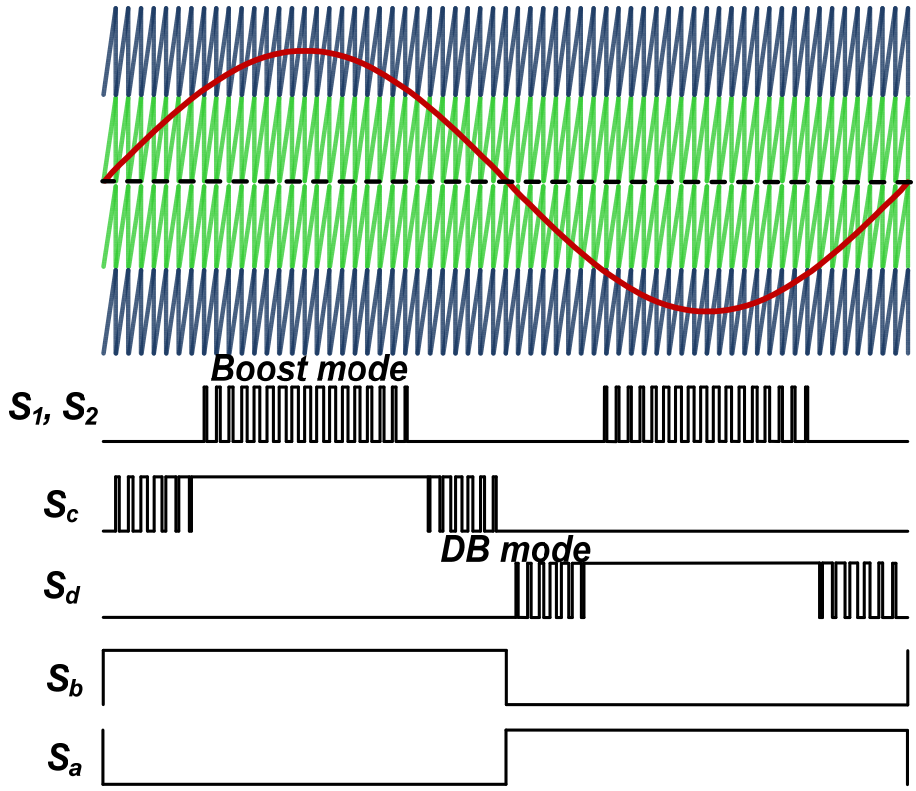


Figure 5.8 PWM generation of boost-dual buck (DB) inverter.

In Chapter 3.3, four switches are used in unfolding circuit for selecting the polarity of the grid. This boost-dual buck inverter keeps the same component number. Since a SiC diode with no reverse recovery loss can be used, it can reach higher efficiencies.

Based on Figure 5.8, the loss in this inverter includes the loss in boost part, H5 part and unfolding part as shown in (4.20).

$$\begin{aligned} P_{Loss} = &\left(P_{S1con} + P_{S1sw}\right)\cdot 2 + \left(P_{D1con} + P_{D1rr}\right)\cdot 2 + \left(P_{Sacon} + P_{Sasw}\right)\cdot 2 \\ &+ \left(P_{Sccon} + P_{Scsw}\right)\cdot 2 + \left(P_{Dccon} + P_{Dcrr}\right)\cdot 2 + P_{Lin} + P_{Lo} \end{aligned} \tag{4.20}$$

As with the discussion in Chapter 5.1 , the loss in boost part can also be calculated by (4.4) to (4.8). The loss in dual buck part can also be calculated by (4.9) to (4.13).

Then the efficiency can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{4.21}$$

Figure 5.9 shows the simulation results of the proposed topology. I_{grid} is the current sent to the grid. V_{boost}, S_a, S_b, S_c and S_d represent the PWM signals for the corresponding switches. V_{boostc}, V_{buckc} *and* $ABS(V_m)$ represent boost carrier, buck carrier and the compensated signal respectively. Both the operation modes and modulation methods are well illustrated in the simulation results.

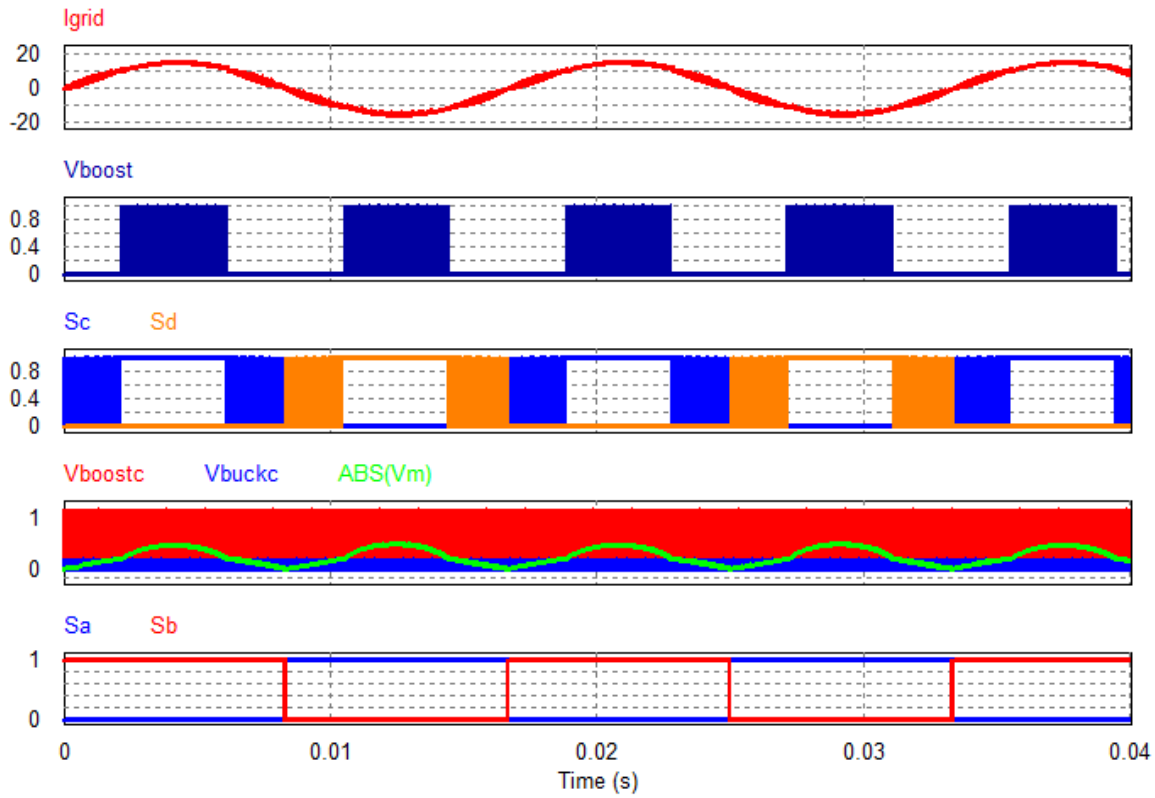


Figure 5.9 Simulation results of boost with dual buck.

5.4 Comparisons of the Proposed Inverters

5.4.1 Efficiency Comparison

The parameters of these inverters are listed in Table 5.1. All of the MOSFETs are CoolMos SPW47N60C3, and diodes are a SiC diode C3D20060D, and FGH30N60LSD are selected for IGBTs. Figure 5.10 and Figure 5.11 show the loss distribution with rated power *2.5 kW* under different input voltage conditions, where diode loss includes its conduction loss and the reverse recovery loss.

Table 5.1: Parameters of all the inverters

Rated Power	Grid Voltage	Grid Frequency	Input Voltage	Switching Frequency
2.5 kW	*240* V_{ac}	*60 Hz*	*200 – 500 V*	*50 kHz*

When $V_{in} = 400\ V$, only buck mode operates; thus, all the boost related losses are zero. In FB and H5, the loss due to diodes is dominant because of the bad performance of the paralleled diodes with their IGBTs. Because the MOSFETs in H5 have lower voltage stress than those used in the buck, FB and DB, the switching loss of MOSFETs in the H5 is smaller than the other three circuits. However, the conduction loss is larger because there are two MOSFETs in series. The loss due to the IGBTs is higher in buck than the other three, because there are always two IGBTs operating together. This can give the idea that if buck type inverter can change the IGBTs in unfolding circuit to MOSFETs, the efficiency in this buck type would be even higher.

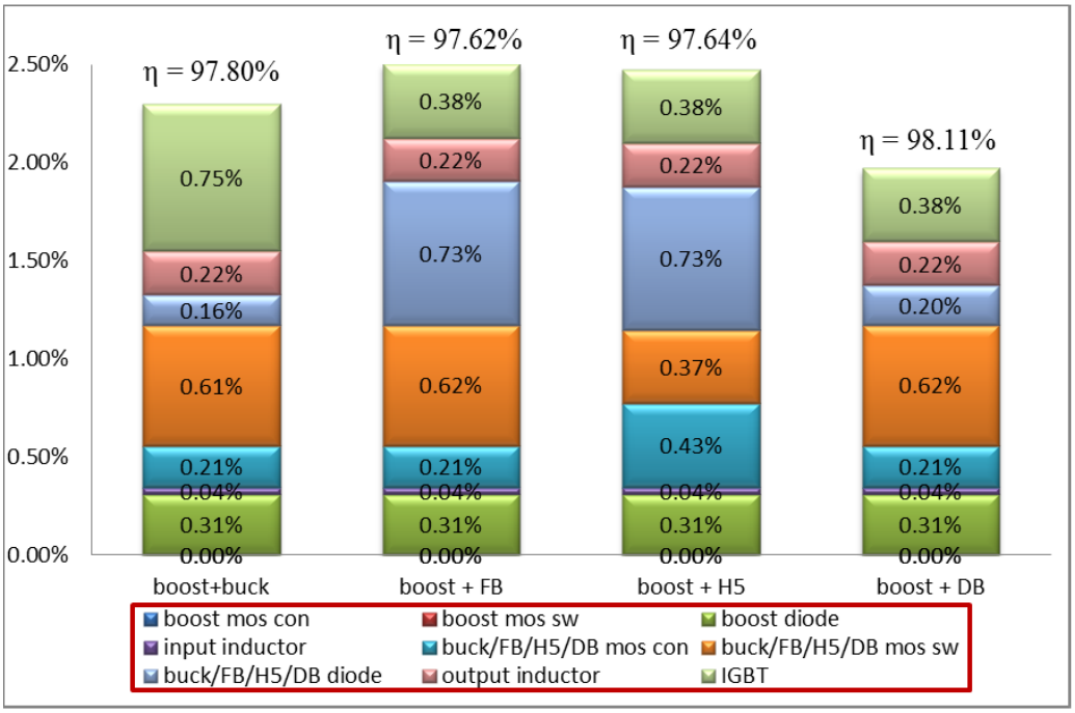


Figure 5.10 Loss distribution in three inverters when V_{in} = *400 V*

When V_{in} = *200 V*, both buck mode and boost mode operate. Because of the uniformity, all the boost related losses are the same. Due to high input current, the boost diode's conduction loss is high. The different is with high input voltage case, the switching loss in buck/FB/H5/DB becomes less on account of lower voltage stress.

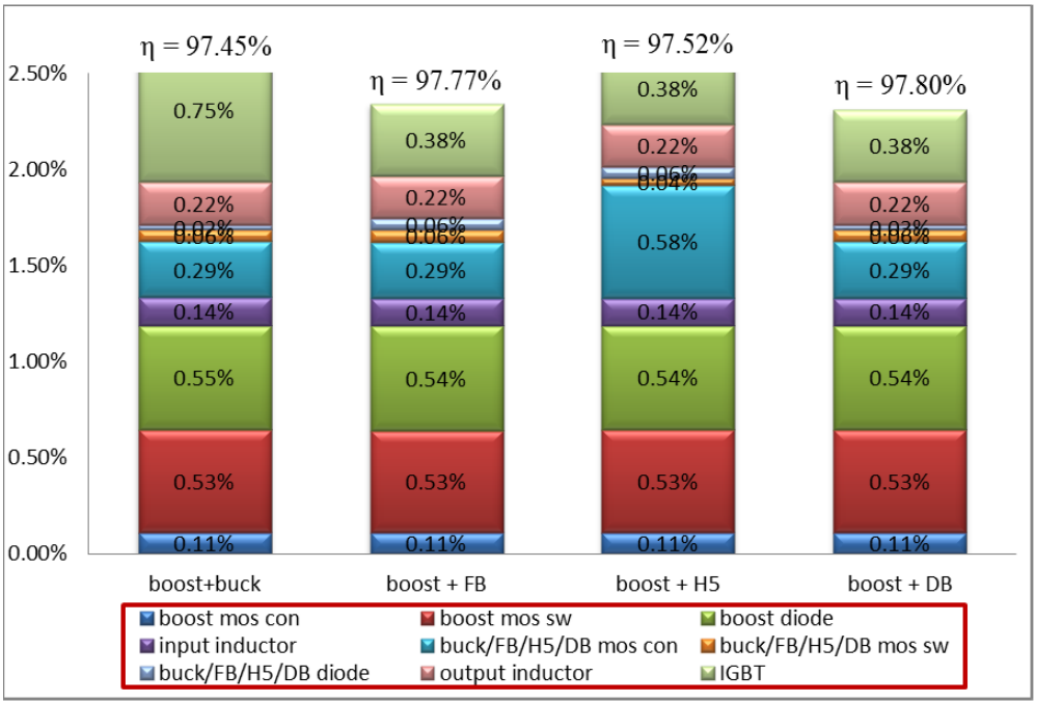


Figure 5.11 Loss distribution in three inverters when V_{in} = *200 V*

It can be observed that the switching loss in buck/FB/H5/DB mode is dominant if the input voltage is larger than the peak of the grid voltage because of the high voltage stress when the switches are off. In this case, first advanced double - carrier based SPWM control described in Chapter 4.1 – reducing the carrier frequency for buck/FB/H5/DB mode will help improve the efficiency. However, the switching loss in in buck/FB/H5/DB mode will not be dominant when the input voltage is smaller than the peak of the grid voltage because of the small voltage stress when the switches are off. In this case, the control described in Chapter 4.1 won't help improve the efficiency significantly. Thus, a more complicated advanced double - carrier based SPWM control - changing the carrier frequency based on the input voltage can be proposed which will be discussed in the future work. Currently, the second advanced double - carrier based

SPWM control in 4.2 – reducing the carrier magnitude for buck/FB/H5/DB mode but keeping the same frequency is implemented.

Figure 5.12 shows the calculated CEC efficiency of these four inverters. It is easy to observe that boost with H5 type inverter gives the highest CEC efficiency in most of the conditions, because H5 type will give the advantages of lower switching loss due to lower voltage stress. The conduction loss is no longer dominant, especially in light load condition, and H5's superiority gives higher efficiency.

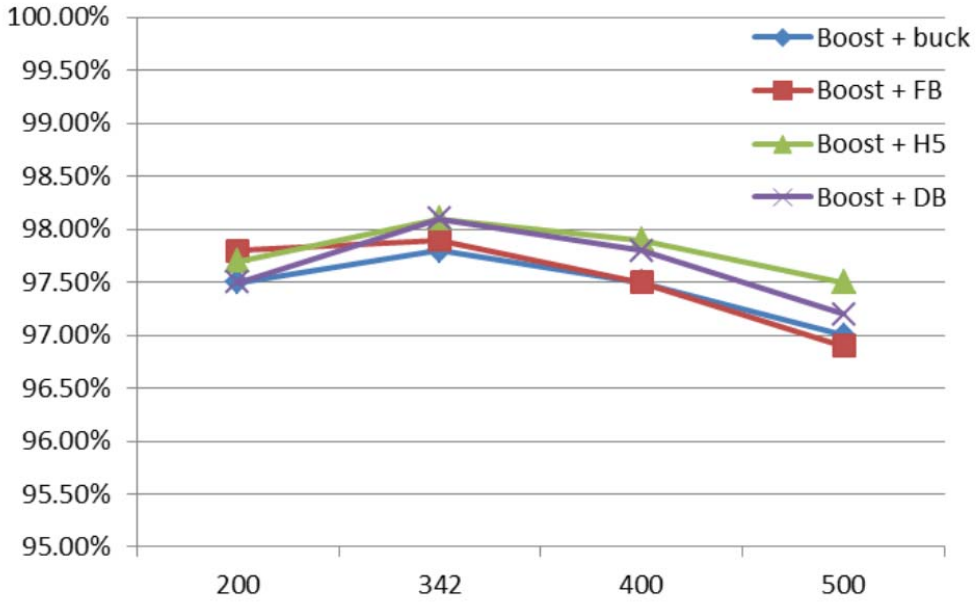


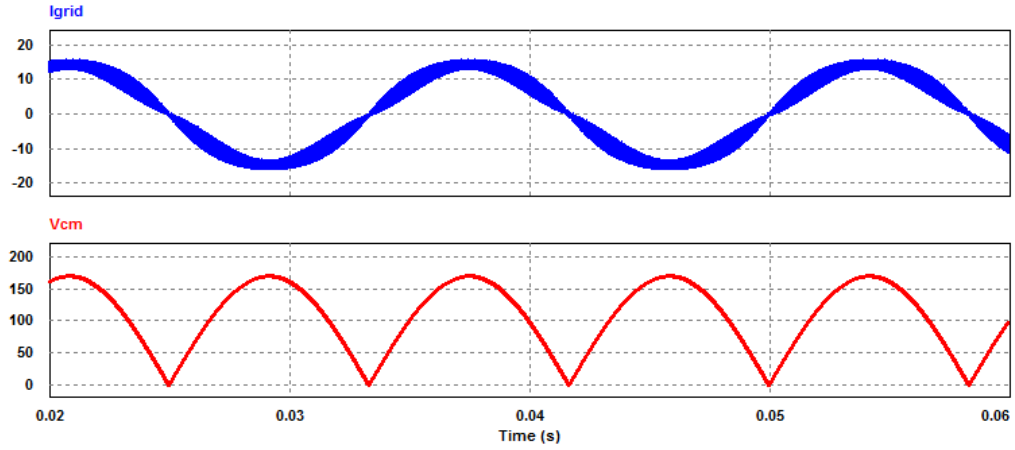
Figure 5.12 CEC efficiency of four inverters under different input voltage condition

5.4.2 Leakage Current Comparison

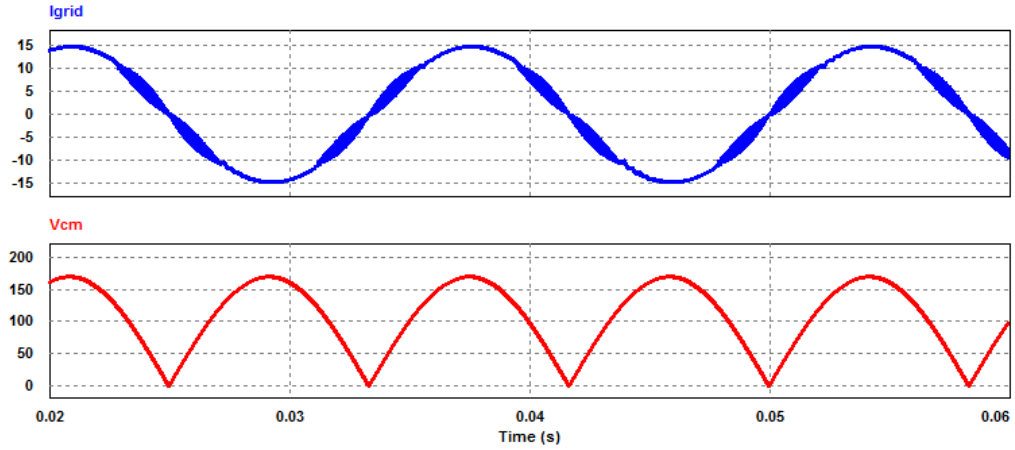
Similar to the analysis used in Chapter 2.2.5, for all the three proposed topologies, the negative terminal "*O*" of solar modules is set as the reference point, and the middle points of the bridge legs are set as "*P*" and "*N*" for the output terminals. Then the instantaneous common-mode voltage v_{cm} can be calculated as

$$v_{cm} = \frac{(v_{PO} + v_{NO})}{2} \tag{5.22}$$

Based on the discussion in Chapter 2.2.5, the common mode voltage V_{cm} for the boost-buck PV inverter proposed in Chapter 2 can be simulated, as shown in Figure 5.13. It could be noticed that V_{cm} changes at line frequency, which will lead to very small leakage current.



(a)



(b)

Figure 5.13 Common mode voltage V_{cm} of boost-buck: (a) V_{in}>V_{gridpk}; (b) V_{in}<V_{gridpk}.

For boost - FB inverter, equations (5.23) and (5.24) can be obtained.

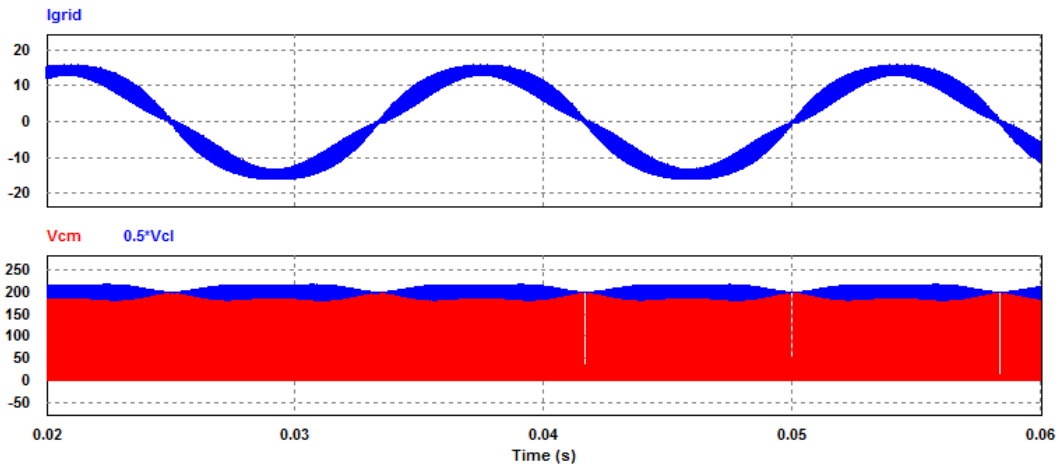
If $v_{grid} > 0$,

$$\begin{cases} v_{PO} = v_{CL} \quad v_{NO} = 0 \quad if\ S_a\ is\ on \\ v_{PO} = 0 \quad v_{NO} = 0 \quad if\ S_a\ is\ off \end{cases} \tag{5.23}$$

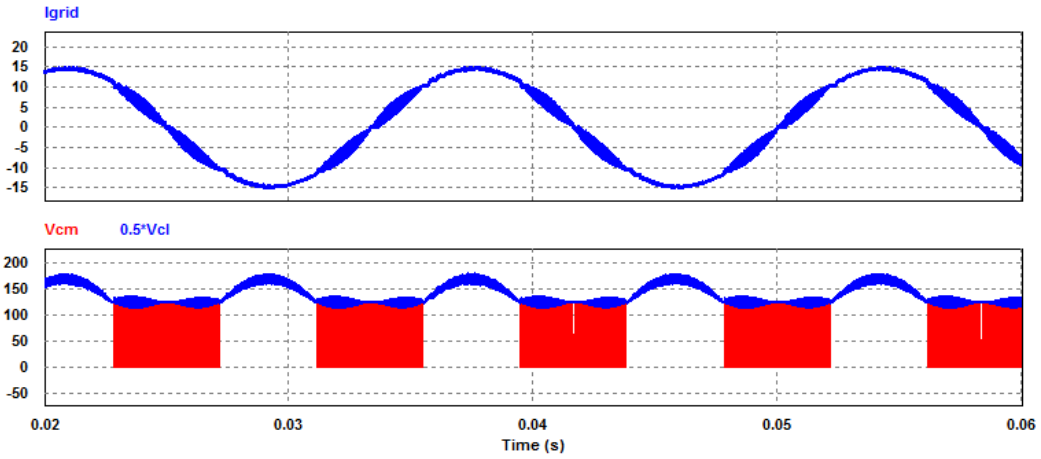
If $v_{grid} < 0$,

$$\begin{cases} v_{PO} = 0 \quad v_{NO} = v_{CL} \quad if\ S_b\ is\ on \\ v_{PO} = 0 \quad v_{NO} = 0 \quad if\ S_b\ is\ off \end{cases} \tag{5.24}$$

where v_{CL} is the middle capacitor's voltage, which is equal to v_{in} when it runs in buck mode and is v_{grid} when it runs in boost mode, as shown in Figure 2.17. Then, v_{cm} changes between 0 and $v_{CL}/2$ with high switching frequency as shown in Figure 5.14. Thus, there will be a high leakage current in this inverter.



(a)



(b)

Figure 5.14 Common mode voltage V_{cm} of boost-FB: (a) V_{in}>V_{gridpk}; (b) V_{in}<V_{gridpk}.

For boost – H5 inverter, equations (5.25) and (5.26) can be obtained.

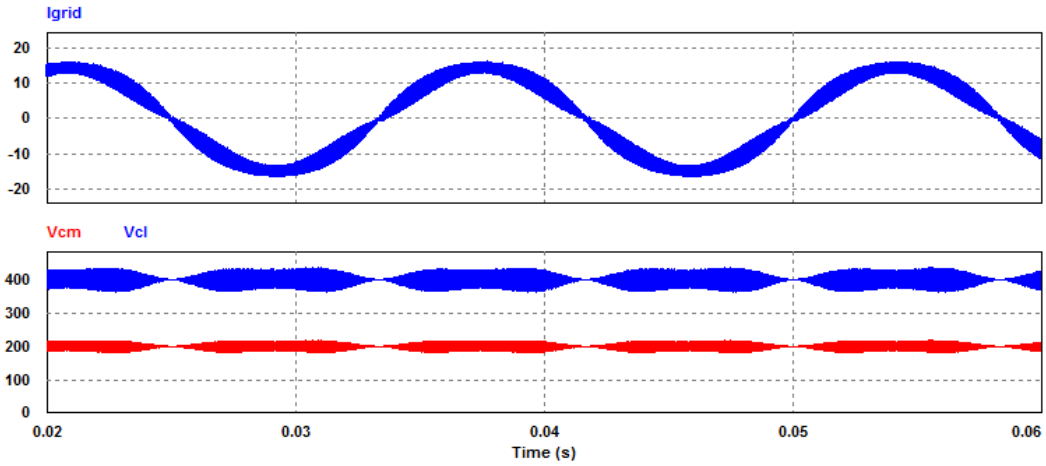
If $v_{grid} > 0$,

$$\begin{cases} v_{PO} = v_{CL} \quad v_{NO} = 0 \quad if\ S_3\ is\ on \\ v_{PO} = \dfrac{v_{CL}}{2} \quad v_{NO} = \dfrac{v_{CL}}{2} \quad if\ S_3\ is\ off \end{cases} \tag{5.25}$$

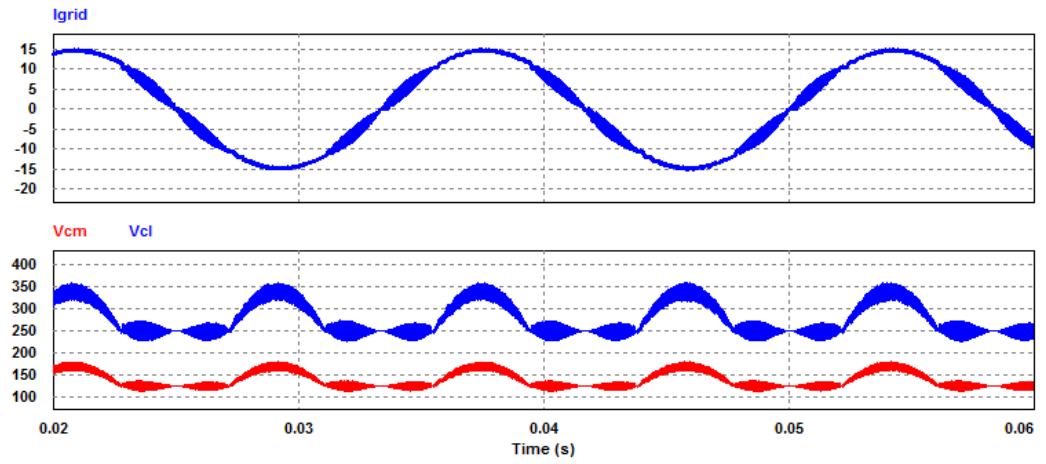
If $v_{grid} < 0$,

$$\begin{cases} v_{PO} = 0 \quad v_{NO} = v_{CL} \quad if\ S_3\ is\ on \\ v_{PO} = \dfrac{v_{CL}}{2} \quad v_{NO} = \dfrac{v_{CL}}{2} \quad if\ S_3\ is\ off \end{cases} \tag{5.26}$$

Then, v_{cm} always equals to $v_{CL}/2$ as shown in Figure 5.15. Thus, there will be no leakage current if the inverter runs in buck mode, but there will be small leakage current if it runs in boost mode.



(a)



(b)

Figure 5.15 Common mode voltage V_{cm} of boost-H5: (a) $V_{in}>V_{gridpk}$; (b) $V_{in}<V_{gridpk}$.

For boost - DB inverter, equations (5.27) and (5.28) can be obtained.

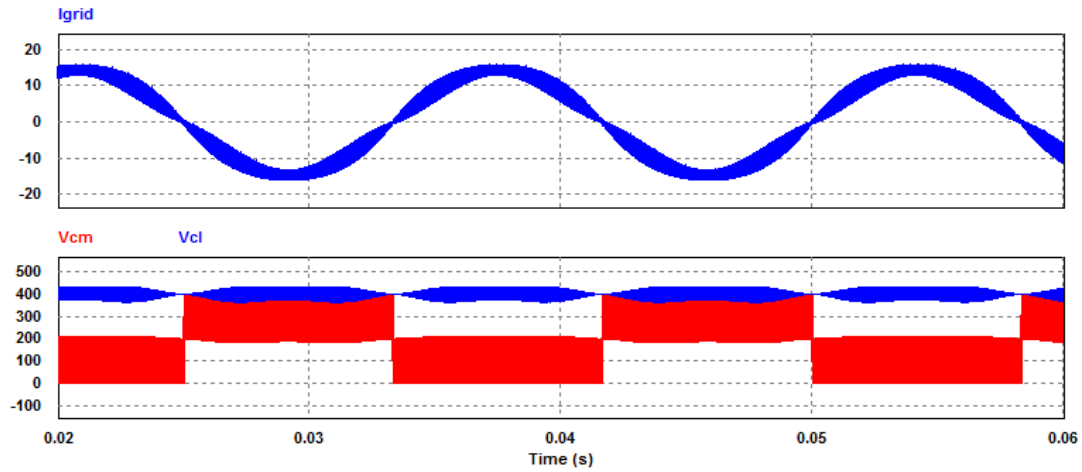
If $v_{grid} > 0$,

$$\begin{cases} v_{P_1O} = v_{CL} \quad v_{NO} = 0 \quad if\ S_c\ is\ on \\ v_{P_1O} = 0 \quad v_{NO} = 0 \quad if\ S_c\ is\ off \\ v_{P_2O} = v_{grid} \end{cases} \tag{5.27}$$

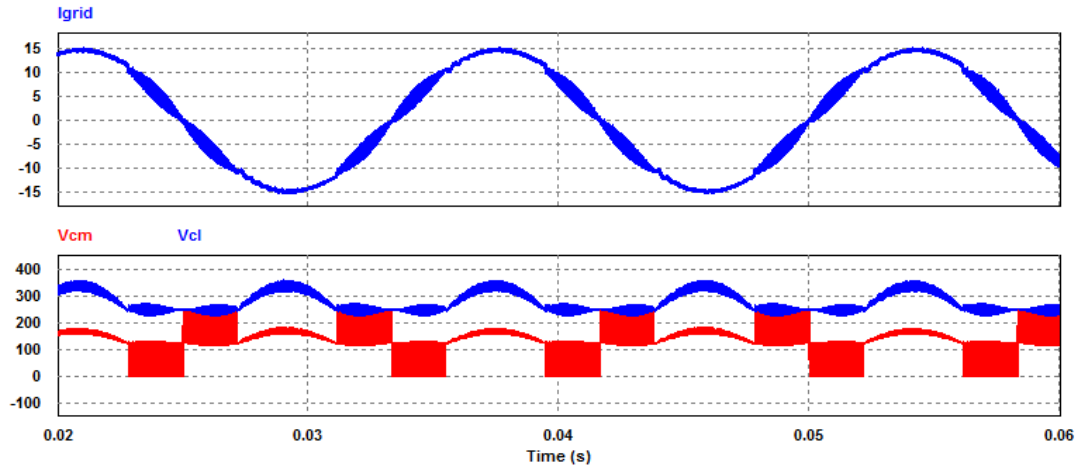
If $v_{grid} < 0$,

$$\begin{cases} v_{P_2O} = 0 \quad v_{NO} = v_{CL} \quad if\ S_d\ is\ on \\ v_{P_2O} = v_{CL} \quad v_{NO} = v_{CL} \quad if\ S_d\ is\ off \\ v_{P_1O} = v_{grid} \end{cases} \tag{5.28}$$

Then, v_{cm} changes among 0, $v_{CL}/2$ and v_{CL} with high switching frequency as shown in Figure 5.16. Thus, there will be a high leakage current in this inverter.



(a)



(b)

Figure 5.16 Common mode voltage V_{cm} of boost-DB: (a) V_{in}>V_{gridpk}; (b) V_{in}<V_{gridpk}.

Table 5.2 lists the summary of the inverters proposed in this chapter and the one in previous chapter – boost-buck converter based inverter. If both efficiency and leakage current are considered, boost-H5 should be the best choice.

Table 5.2: Comparisons of leakage current in different proposed inverters.

	Boost-buck	Boost-FB	Boost-H5	Boost-DB
Common mode voltage (v_{cm})	$\frac{\lvert v_{grid} \rvert}{2}$	$0 \ or \ \frac{v_{CL}}{2}$	$\frac{v_{CL}}{2}$	$0 \ or \ \frac{v_{CL}}{2} \ or \ v_{CL}$
v_{cm} changing frequency	Line frequency	High switching frequency	Constant in buck mode Line frequency in boost mode	High switching frequency
Leakage current	low	high	low	high

5.5 Summary

This chapter proposed another three dual-mode double-carrier based SPWM inverters based on the boost/buck operation mode concept. With both step-up and step-down functions, this type of inverter can achieve high efficiency in a wide range because only one switch operates at the PWM frequency at a time.

In fact, if any inverter is working based on buck converter's concept, it can be integrated with boost part and operate in either buck or boost mode. As a result, the new inverter won't have the limitation on its input voltage, which means the input voltage doesn't need to be higher than the peak of the output ac voltage. In this way, the input voltage range could be widened.

The efficiencies and the detailed loss distribution of these inverters with one of the advanced modulation method are compared. Based on the comparison, boost mode with H5 PV inverter gives highest CEC efficiency in most cases, because it has lowest switching loss.

The leakage current for the three inverters have been analyzed. From this point of view, boost-H5 performs the best. Thus, if both efficiency and leakage current are considered, boost-H5 should be the best choice.

Chapter 6:
Conclusions and Future Works

6.1 Summary

This dissertation proposed a single stage boost-buck converter based high-efficiency grid-tied PV inverter. Based on its unique operation mode, the proper control method is proposed for smooth mode transition. Based on the similar concept, three other inverters with both step-up and step-down functions are proposed. Along with that, three advanced control methods are also proposed

The following conclusions are drawn from the work.

1) A high efficiency boost-buck converter based single stage PV inverter is proposed. The first converter part operates in either boost or buck mode; thus, it has a wide input voltage range, which is good for PV application. The second inverter part is composed with unfolding circuit based on the direction of the grid. Therefore from power processing point of view, this inverter is a single stage inverter. Because it processes power either as a buck converter or a boost converter, high efficiency can be achieved.
2) After analyzing its model, it is known that if the input inductor L_1 can be reduced, the double-pole position, which is considered as the frequency wall of bandwidth, will be pushed to higher frequency. Moreover, the gain will increase as well. Also, the Q factor will be reduced accordingly, which benefits the high bandwidth design for the boost mode. However, decreasing the output inductor L_2 will keep

the same double-pole position and have higher Q factor, which won't help controller design. As a result, small L_1 and large L_2 are preferred from the design point of view.

3) Because small L_1 is preferred for easier controller design, an interleaved-boost-cascaded-with-buck (IBCB) converter is proposed to increase the resonant pole frequency by the use of smaller boost inductor value. As a result, the control loop bandwidth can be pushed further up to enhance the robustness of the complete system and helps the system be controlled easier.
4) The double-carrier modulation method is proposed based on the inverter's operation mode. The duty cycle for buck switch is always one if the inverter is running in boost mode. The duty cycle for boost switches are always zero if the inverter is running in buck mode. Because of this, the carrier for boost mode is stacked on the top of the carrier for buck mode. As a result, there is no need to compare the input and output voltage to decide which mode the inverter should operate in and the inverter operates smoothly between these two modes.
5) Three advanced modulation methods are proposed. The first one - Double-carrier with different frequencies can help further improve the efficiency. The second one - Double-carrier with different magnitudes can help increase the bandwidth and gain. The last one - Double-carrier with different frequencies and magnitudes takes the advantage of both.
6) Based on the operation mode concept, many topologies can be proposed. If any inverter is working based on buck converter's concept, it can be integrated with boost part. As a result, the new inverter won't have the limitation on its input

voltage, which means the input voltage doesn't need to be higher than the peak of the output ac voltage. In this way, the input voltage range could be widened. In this dissertation another three dual-mode double-carrier based SPWM inverters are proposed for example. With both step-up and step-down functions, this type of inverter can achieve high efficiency in a wide range because only one switch operates at the PWM frequency at a time.

7) The lifetime issue of the electrolytic capacitors has been investigated and analyzed. Although the electrolytic capacitors have limited lifetime, it can still be used by applying smaller voltage and current ripple to prolong its lifetime. Because the end of its life doesn't mean its failure, the electrolytic capacitor can work much longer than its estimated lifetime. As time goes on, the capacitance of electrolytic capacitor will be reduced. The smaller capacitance leads to lower Maximum Power Point Tracking (MPPT) efficiency. Thus, at the end of the electrolytic capacitors' lifetime, the capacitors won't fail to work but the change in capacitance will reduce the MPPT efficiency and will reduce the whole system's efficiency as well.

6.2 Future Works

1) When the grid is abnormal, the PV inverter needs to disconnect from the grid. A control scheme needs to be developed and further investigated to make the inverter to operate between grid-tied mode and islanding mode.

2) Although the three dual-mode double-carrier based SPWM inverters are proposed and their efficiency analysis has been provided, some more experiments should be conducted and their actual efficiency should be compared.

3) Other types of dual-mode double-carrier based SPWM inverters can be investigated, such as boost along with HERIC (Highly Efficiency and Reliable Inverter Concept) [73] inverter.

4) For boost-FB (Full Bridge) and boost-DB (Dual Buck) inverter, other modulation methods could be considered to eliminating their leakage currents, such as bipolar PWM modulation method.

Bibliography

[1] German Advisory Council on Global Change WBGU Berlin 2003 www.wbgu.de; Renewable Energy Policy Network for the 21st Century, Renewables, Global Status Report 2006

[2] J.-S. Lai, "Power conditioning systems for renewable energies," in *International Conference on Electrical Machines and Systems, ICEMS 07*, pp. 209-218, Oct. 2007.

[3] Y.T. Tan, D.S. Kirschen, and N. Jenkins, "A model of PV generation suitable for stability analysis," *IEEE Trans. Energy Convers.*, vol. 19, no. 4, pp. 748-755, Dec 2004.

[4] S. Duryea, S. Islam, and W. Lawrance, "A battery management system for stand-alone photovoltaic energy systems," *IEEE Industry Applications Magazine*, vol. 7, no. 3, pp. 67–72, Jun. 2001.

[5] Strong, Steven (June 9, 2010 (last update)). "Building Integrated Photovoltaics (BIPV)". Whole Building Design Guide. Retrieved 2011-07-26.

[6] Bangyin Liu, Shanxu Duan, Tao Cai, "Photovoltaic DC-Building-Module-Based BIPV System-Concept and Design Considerations," *IEEE Trans. Power Electron*, Vol. 26, No. 5, pp. 1418 – 1429, 2011.

[7] H Chiu; Y Lo; C Yao; S Cheng, "Design and Implementation of a Photovoltaic High-Intensity-Discharge Street Lighting System, " *IEEE Transactions on Power Electronics,* vol.26, no.12, pp.3464-3471, Dec. 2011

[8] J. P. Benner and L. Kazmerski, "Photovoltaics gaining greater visibility," *IEEE Spectr.*, vol. 29, no. 9, pp. 34–42, Sep. 1999.

[9] R. Billinton, and R. Karki, "Capacity expansion of small isolated power systems using PV and wind energy," *IEEE Trans. Power Syst*., vol. 16, no. 4, pp. 892-897, Nov 2001.

[10] J. T. Bialasiewicz, “Renewable Energy Systems with Photovoltaic Power Generators: Operation and Modeling,” *IEEE Trans. Ind. Electron*., vol. 55, no. 7, pp. 2752-2758, July. 2008.

[11] X Guan, Z Xu, and Q. S. Jia, “Energy-Efficient Buildings Facilitated by Microgrid,” *IEEE Trans. on Smart Grid*, vol. 1, no. 3, pp. 243-252, Dec. 2010.

[12] Koran, A.; Sano, K.; Rae-Young Kim; Jih-Sheng Lai; , "Design of a Photovoltaic Simulator With a Novel Reference Signal Generator and Two-Stage LC Output Filter," *IEEE Transactions on Power Electronics,* vol.25, no.5, pp.1331-1338, May 2010

[13] Yaow-Ming Chen; Hsu-Chin Wu; Yung-Chu Chen; Kung-Yen Lee; Shian-Shing Shyu; , "The AC Line Current Regulation Strategy for the Grid-Connected PV System," *Power Electronics, IEEE Transactions on* , vol.25, no.1, pp.209-218, Jan. 2010

[14] *IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, IEEE Std. 1547, 2003.

[15] Fumihiro Shinjo, Keiji Wada, Toshihisa Shimizu, "A Single-Phase Grid-Connected Inverter with a Power Decoupling Function," *Power Electronics Specialists Conference, 2007,* IEEE 17-21, pp. 1245–1249.

[16] Casadei, D.; Grandi, G.; Rossi, C.; “Single-phase single-stage photovoltaic generation system based on a ripple correlation control maximum power point tracking”, *IEEE Transaction on Energy Conversion,* Volume 21, Issue 2, pp. 562–568, June 2006.

[17] Yi Huang; Miaosen Shen; Peng, F.Z.; Jin Wang; “Z-Source Inverter for Residential Photovoltaic Systems”, IEEE Transactions on Power Electronics, Volume 21, Issue 6, pp. 1776 – 1782, Nov. 2006.

[18] Kjaer, S.B.; Pedersen, J.K.; Blaabjerg, F.; “A review of single-phase grid-connected inverters for photovoltaic modules”, *IEEE Transactions on Industry Applications,* Volume 41, Issue 5, pp. 1292 – 1306, Sept.-Oct. 2005.

[19] M. Calais, J. Myrzik, T. Spooner, V. G. Agelidis, “Inverter for Single-Phase Grid Connected Photovoltaic Systems – An Overview,” *Power Electron. Spec.* Conf., Vol. 4, pp. 1995-2000, Feb. 2002.

[20] Salas, V.; Olias, E.; “Maximum power point tracking in the PV grid-connect inverters of 5 kW”, Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE, pp. 193 – 196.

[21] J.M. Kwon, K.H. Nam, and B.H. Kwon, “Photovoltaic power conditioning system with line connection,” *IEEE Trans. Ind. Electron*., vol. 53, no. 4, pp. 1048-1054, Aug. 2006.

[22] P. G. Barbosa, H. A. C. Braga, M. do Carmo Barbosa Rodrigues, and E. C. Teixeira, “Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems,” *IEEE Trans. Power Electron*., vol. 21, no. 4, pp. 1116–1124, Jul. 2006.

[23] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, “Auto-calibrating dc link current sensing technique for transformerless, grid connected, H-bridge inverter systems,” *IEEE Trans. Power Electron*., vol. 21, no. 5, pp. 1385–1396, Sep. 2006.

[24] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup, “Implementation and test of an online embedded grid impedance estimation technique for PV inverters,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1136–1144, Aug. 2005.

[25] Bo Yang; Wuhua Li; Yi Zhao; Xiangning He; , "Design and Analysis of a Grid-Connected Photovoltaic Power System," *Power Electronics, IEEE Transactions on* , vol.25, no.4, pp.992-1000, April 2010

[26] B. K. Bose, P. M. Szczesny, and R. L. Steigerwald, “Microcomputer control of a residential photovoltaic power conditioning system,” *IEEE Trans. Ind. Applicat*., vol. IA-21, pp. 1182–1191, Sept./Oct. 1985.

[27] S. Saha and V. P. Sundarsingh, “Grid connected photovoltaic inverter as an industrial product,” Eur. *Polymer Fed*., pp. 46–51, Oct. 1996.

[28] S. Saha and V. P. Sundarsingh, “Novel grid-connected photovoltaic inverter,” *Proc. Inst. Elect. Eng*., vol. 143, pp. 219–224, Mar. 1996.

[29] Martins, D.C.; Demonti, R.; “Interconnection of a photovoltaic panels array to a single-phase utility line from a static conversion system”, *Power Electronics Specialists Conference*, 2000, pp. 1207-1211.

[30] R. O. Cáceres and I. Barbi, "A boost dc-ac converter: analysis, design, and experimentation," *IEEE Trans. Power Electron*., vol. 14, pp. 134–141, Jan. 1999.

[31] N. Vázquez, J. Almazan, J. Álvarez, C. Aguilar, and J. Arau, "Analysis and experimental study of the buck, boost and buck-boost inverters," in *Proc. IEEE PESC'99*, Charleston, SC, June 27–July 1 1999, pp. 801–806.

[32] N. Kasa, T. Iida, and H. Iwamoto, "An inverter using buck-boost type chopper circuits for popular small-scale photovoltaic power system," in *Proc. IEEE IECON'99,* San Jose, CA, Nov./Dec. 1999, pp. 185–190.

[33] W. Chien-Ming, "Anovel single-stage full-bridge buck-boost inverter," IEEE Trans. Power Electron., vol. 19, no. 1, pp. 150–159, Jan. 2004.

[34] S. Jain, and V. Agarwal, "A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking," *IEEE Trans. Power Electron*., vol. 22, no. 5, pp. 1928-1940, Sep. 2007.

[35] Y. Xue, L. Chang, S. B. Kjær, J. Bordonau, and T. Shimizu, "Topologies of single phase inverters for small distributed power generators: An overview," *IEEE Trans. Power Electron*., vol. 19, no. 5, pp. 1305–1314, Sep. 2004.

[36] Xiaoming Yuan; Yingqi Zhang; "Status and Opportunities of Photovoltaic Inverters in Grid-Tied and Micro-Grid Systems", *Power Electronics and Motion Control Conference*, 2006, pp. 1-4.

[37] Kerekes, T.; Liserre, M.; Teodorescu, R.; Klumpner, C.; Sumner, M.; , "Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies," *Power Electronics, IEEE Transactions on* , vol.24, no.9, pp.2202-2211, Sept. 2009

[38] German Patent H5-Topology: DE 10 2004 030 912 B3, issued 19.01.2006.

[39] "PRECAUTIONS AND GUIDELINES" from http://www.chemi-con.co.jp/Welcome_e.html.

[40] "General Descriptions of Aluminum Electrolytic Capacitors" from http://www.nichicon-us.com/english/products/index.html.

[41] "Application Guide Aluminum Electrolytic Capacitors" from http://www.cde.com/.

[42] "Aluminum Capacitors" from http://www.vishay.com/capacitors/aluminum/

[43] Department of Energy Roadmap

[44] “Life-Limiting Factors in Electrolytic Capacitors” from http://www.evoxrifa.fi/technote_pdf/electrolytic_life_factors.pdf.

[45] T. Shimizu, K. Wada and N. Nakamura, “Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system,” *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264-1272, Sep. 2006.

[46] C. Rodriguez, G.A.J. Amaratunga, "Long-Lifetime Power Inverter for Photovoltaic AC Modules," *IEEE Transactions on Industrial Electronics,* vol.55, no.7, pp.2593-2601, July 2008

[47] P.T. Krein, R.S. Balog, "Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port," in *Applied Power Electronics Conference and Exposition, 2009,* vol., no., pp.620-625, 15-19 Feb. 2009

[48] Duo Li, Zhe Zhang, Biwen Xu, Min Chen, Zhaoming Qian, "A method of power decoupling for long life micro-inverter", *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society,* pp. 802 - 807, 2011

[49] Schimpf, F., Norum, L., "Effective use of film capacitors in single-phase PV-inverters by active power decoupling", *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society,* pp. 2784 - 2789, 2010

[50] Valentini, M.; Raducu, A.; Sera, D.; Teodorescu, R.; “PV Inverter Test Setup for European Efficiency, Static and Dynamic MPPT Efficiency Evaluation,” *11th International Conference on Optimization of Electrical and Electronic Equipment,* pp. 433-438, 2008.

[51] Ogura, K.; Nishida, T.; Hiraki, E.; Nakaoka, M.; Nagai, S.;, “Time-sharing boost chopper cascaded dual mode single-phase sinewave inverter for solar photovoltaic power generation system ,” *Power Electronics Specialists Conference, 2004*, pp. 4763 - 4767 Vol.6

[52] Feng Tian; Al-Atrash, H.; Kersten, R.; Scholl, C.; Siri, K.; Batarseh, I.; “A Single-Staged PV Array-Based High-Frequency Link Inverter Design with Grid

Connection", *Applied Power Electronics Conference and Exposition, 2006*, pp. 19-23.

[53] Zheng Zhao, Kuan-Hung Wu and Jih-Sheng Lai;, "Utility Grid Impact with High Penetration PV Micro-Inverters Operating under Burst Mode Using Simplified Simulation Model," *Energy Conversion Congress and Exposition*, pp. 3928—3932, September 2011.

[54] J. M. A. Myrzik and M. Calais, "String and module integrated inverters for single-phase grid connected photovoltaic systems—A review," in *Proc. IEEE Power Tech. Conf.*, Bologna, Italy, Jun. 23–26, 2003, vol. 2, pp. 1–8.

[55] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—An overview," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1998, vol. 1, pp. 224–229.

[56] German Standard DIN VDE 0126- 1-1.

[57] R. Gonzales, J. L`opez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.

[58] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.

[59] H. F. Xiao and S. J. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010.

[60] V. Vorpérian, "Simplified analysis of PWM converters using model of PWM switch—I: Continuous conduction mode," *IEEE Trans. Aerosp.Electron. Syst.*, vol. 26, no. 3, pp. 490–496, May 1990.

[61] D. Czarkowski and M. K. Kazimierczuk, "Energy-conservation approach to modeling PWM dc–dc converters," *IEEE Trans. Aerosp.Electron. Syst.*, vol. AES-29, no. 3, pp. 1059–1063, Jul. 1993.

[62] R. Giral, L. S. Martinez, and S. Singer, "Interleaved converters operation based on CMC," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 643–652, Jul. 1999.

[63] İbrahim SEFA, Şaban ÖZDEMİR "Multifunctional Interleaved Boost Converter for PV Systems", *IEEE International Symposium on Industrial Electronics (ISIE), 2010*, pp. 951 – 956

[64] Patel, H.; Agarwal, V.; , "MPPT Scheme for a PV-Fed Single-Phase Single-Stage Grid-Connected Inverter Operating in CCM With Only One Current Sensor ," *Energy Conversion, IEEE Transactions on* , Vol. 24 , Issue: 1 , pp. 256 – 263, 2009

[65] Ribeiro, H.; Silva, F.; Pinto, S.; Borges, B., "Single stage inverter for PV applications with One Cycle Sampling technique in the MPPT algorithm," 35th Annual Conference of IEEE *Industrial Electronics (IECON)*, pp. 842 – 849, November 2009.

[66] Ding Li; Feng Gao; Poh Chiang Loh; Peng Wang; Yi Tang; , "Transient maximum power point tracking for single-stage grid-tied inverter ," *Energy Conversion Congress and Exposition*, pp. 313 – 318, September 2009

[67] T. Esram and P. L.Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Conv.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.

[68] S. Jain and V. Agarwal, "Comparison of the performance of maximum power point tracking schemes applied to single-stage grid-connected photovoltaic systems," *IET Electr. Power Appl.*, vol. 1, no. 5, pp. 753–762, Sep. 2007.

[69] H. P. Desai and H. K. Patel, "Maximum power point algorithm in PV generation: An overview," in *Proc. 7th Int. Conf. Power Electron. Drive Syst.*, Nov. 27–30, 2007, pp. 624–630.

[70] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "A technique for improving P&O MPPT performances of double-stage grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4473–4482, Nov. 2009.

[71] Sera D., Kerekes T., Teodorescu R., Blaabjerg F., "Improved MPPT Algorithms for Rapidly Changing Environmental Conditions", *Power Electronics and Motion Control Conference*, pp.1614-1619, 2006.

[72] Abdelsalam, A.K.; Massoud, A.M.; Ahmed, S.; Enjeti, P.N.; "High-Performance Adaptive Perturb and Observe MPPT Technique for Photovoltaic-Based

Microgrids", *IEEE Transactions on Power Electronics,* vol. 26, pp. 1010 – 1021, 2011.

[73] H. Schmidt, S. Christoph, and J. Ketterer, "Current inverter for direct/alternating currents, has direct and alternating connections with an intermediate power store, a bridge circuit, rectifier diodes and a inductive choke," German Patent DE10 221 592 A1, Dec. 4, 2003.