

## LD-2 PENCILBOX LOGIC DESIGN TRAINER

THE LD-2 PENCILBOX LOGIC DESIGNER/TRAINER PERMITS STUDENTS TO AVOID THE REPETITIVE BUILDING OF FREQUENTLY USED CIRCUITS.

ALL FUNCTIONS ARE INTERNALLY CONNECTED TO THREE SOLDERLESS INTERCONNECT SOCKETS WITH TWO TIE POINTS FOR EACH SIGNAL.

### DC POWER SUPPLIES

+12V +/- 5% 500MA MAX, -12V +/- 5% 200MA MAX,  
+5V +/- 5% 1A MAX.

### TTL/CMOS OPERATION

SELECTABLE OUTPUT VOLTAGE OF CLOCK, PULSER, LOGIC SWITCHES. INPUT VOLTAGE THRESHOLDS OF SEVEN SEGMENT DISPLAYS, LOGIC INDICATORS AND VCC TIE POINT BETWEEN 5V, TTL AND 12V CMOS.

### CLOCK

1HZ +/- 20%; 1KHZ +/- 20%, 100KHZ +/- 20%. ALSO USER VARIABLE WITH EXTERNAL CAPACITOR.

LOGIC "1" OUTPUT CURRENT 2MA @ 4.0V MIN. (5V/TTL), 4MA @ 11.0V MIN. (12V/CMOS).

LOGIC "0" OUTPUT CURRENT 2MA @ 0.1V MAX. (5V/TTL), 5MA @ 0.1V MAX. (12V/CMOS).

### PULSERS

TWO FULLY DEBOUNCED PUSHBUTTONS WITH TRUE LOGIC AND COMPLEMENTARY OUTPUTS.

LOGIC "1" OUTPUT CURRENT 2MA @ 2.5V MIN. (5V/TTL), 2 MA @ 11.0 V MIN. (12 V/CMOS).

LOGIC "0" OUTPUT CURRENT 2MA @ 0.4V MAX. (5V/TTL), 5MA @ 0.4V MAX. (12 V/CMOS).

### LOGIC SWITCHES

EIGHT SPDT SWITCHES SELECT OUTPUT VCC OR GROUND. OUTPUT CURRENT, ALL CASES: 200MA MAX.

### LOGIC INDICATORS

EIGHT LEDs BUFFERED BY TWO FOUR-BIT LATCHES WITH SEPARATE ENABLES. INPUT IMPEDANCE, ALL INPUTS: 100K OHMS.

### CONNECTORS

ALL FUNCTIONS ARE PERMANENTLY TIED TO THREE SOLDERLESS TIE POINT CONNECTORS. EACH TIE POINT HAS TWO SOLDERLESS CONNECTION POINTS. GND (GROUND), +5V, VCC AND CLOCK OUT HAVE FOUR CONNECTION POINTS EACH.

### DIMENSIONS

25.4 x 19.0 x 6.5CM (W x D x H).

### WEIGHT

0.71KG.

