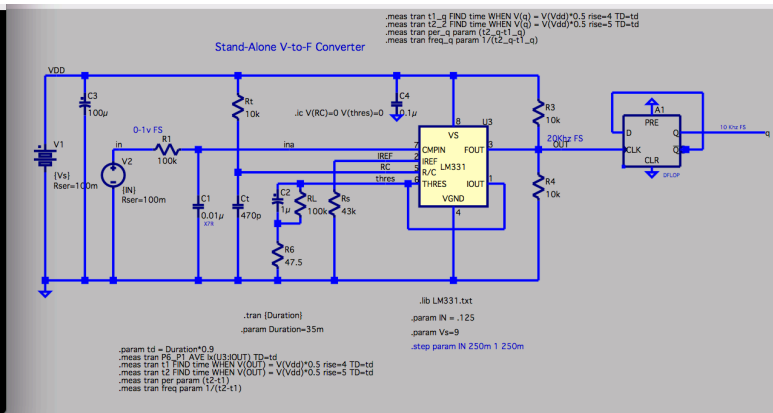
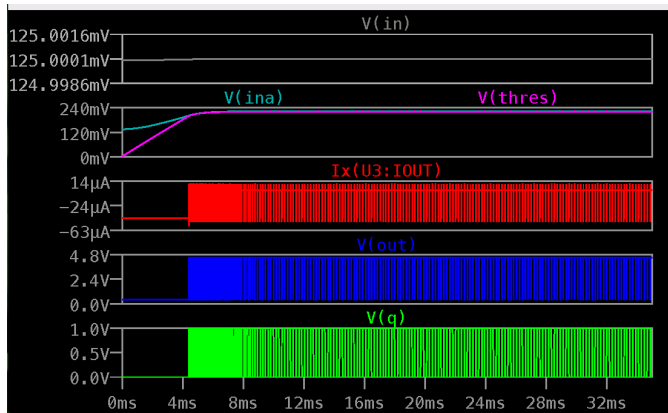


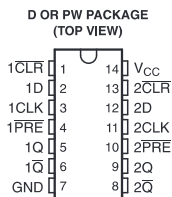
Attribute	Value	Vis.
Prefix	A	
InstName	A1	X
SpiceModel	DFLOP	
Value		X
Value2		
SpiceLine		
SpiceLine2		



FEATURES

- Controlled Baseline
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption, 80 μA Max I_{CC}
- Typical $t_{\text{pd}} = 15 \text{ ns}$
- $\pm 4 \text{ mA}$ Output Drive at 5 V
- Low Input Current of 1 mA Max

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



DESCRIPTION/ORDERING INFORMATION

The SN74HC74 device contains two independent D-type positive edge triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC – D	Reel of 2500	SN74HC74MDREP	HC74MEP
	TSSOP – PW	Reel of 2000	SN74HC74MPWREP	HC74MEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

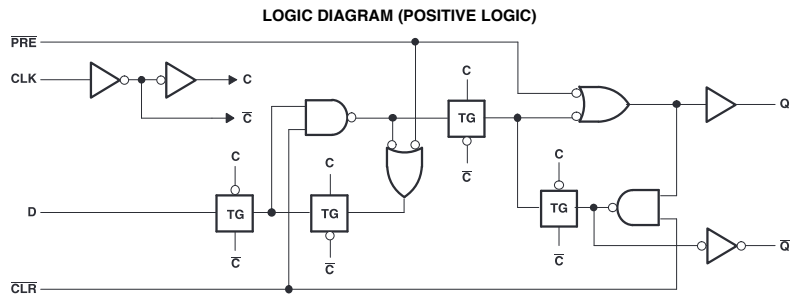


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SN74HC74-EP
DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP
WITH CLEAR AND PRESET
 SCLS710–MARCH 2008



Absolute Maximum Ratings⁽¹⁾
 over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
I _{IK}	Input clamp current	V _I < 0 or V _I = 0 to V _{CC} ⁽¹⁾		±20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O = 0 to V _{CC} ⁽¹⁾		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
θ _{JA}	Package thermal impedance ⁽²⁾	PW package		113	°C/W
T _{stg}	Storage temperature range		−60	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	V
		V _{CC} = 4.5 V		3.15	
		V _{CC} = 6 V		4.2	
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 6 V		1.8	
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
ΔtΔv	Input transition rise/fall time	V _{CC} = 2 V		1000	ns
		V _{CC} = 4.5 V		500	
		V _{CC} = 6 V		400	
T _A	Operating free-air temperature	−55	125		°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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WITH CLEAR AND PRESET

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		I _{OH} = –4 mA	4.5 V	3.98	4.3		3.7		
		I _{OH} = –5.2 mA	6 V	5.48	5.8		5.2		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V				4	80	µA
C _I			2 V to 6 V		3	10		10	pF

TIMING REQUIREMENTS

			V _{CC}	T _A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t _{clock}	Clock frequency		2 V		6		4.2	MHz
			4.5 V		31		21	
			6 V	0	36	0	25	
t _w	Pulse duration	PRE or CLR low	2 V	100		150	ns	
			4.5 V	20		30		
			6 V	17		25		
	CLK high or low	2 V	80		120			
		4.5 V	16		24			
		6 V	14		20			
t _{su}	Data	2 V	100		150	ns		
		4.5 V	20		30			
		6 V	17		25			
	PRE or CLR inactive	2 V	25		40			
		4.5 V	5		8			
		6 V	4		7			
t _h	Hold time, data after CLK↑		2 V	0		0	ns	
			4.5 V	0		0		
			6 V	0		0		

SN74HC74-EP
DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP
WITH CLEAR AND PRESET

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SWITCHING CHARACTERISTICS

over operating free-air temperature range $C_L = 50$ pF, (unless otherwise noted)

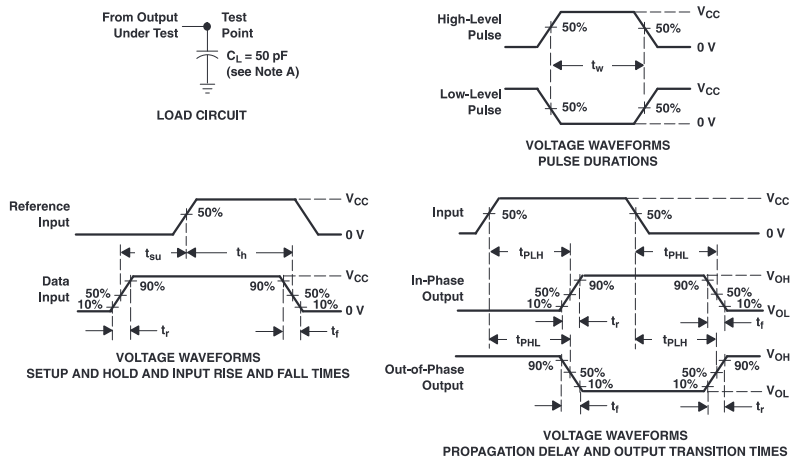
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			2 V	6	10		4.2		MHz
			4.5 V	31	50		21		
			6 V	36	60		25		
t_{pd}	PRE or CLR	Q or \bar{Q}	2 V		70	230		345	ns
			4.5 V		20	46		69	
			6 V		15	39		59	
	CLK	Q or \bar{Q}	2 V		70	175		250	
			4.5 V		20	35		50	
			6 V		15	30		42	
t_t		Q or \bar{Q}	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, t_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC74MPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74MEP	Samples
V62/08613-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74MEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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