MURDOCH
UNIVERSITY
PERTH, WESTERN AUSTRALIA

School of Engineering and Energy
ENG460 Engineering Thesis Final Report

Grid-connected Transformerless Single-phase Photovoltaic Inverters: An Evaluation on DC Current Injection and PV Array Voltage Fluctuation

---

"A report submitted to the School of Engineering and Energy, Murdoch University in partial fulfilment of the requirements for the degree of Bachelor of Engineering"

AUTHOR: Claude Morris, **ACADEMIC SUPERVISOR:** Dr Martina Calais, **ASSOCIATE SUPERVISOR:** Andrew Ruscoe, **UNIT COORDINATOR:** Professor Parisa Bahri

Abstract

A number of political, environmental and technical factors have resulted in the increase of implementation of renewable technology including grid connected photovoltaic inverters.

As a result, new topologies for grid connected inverters providing higher efficiencies and lower manufacturing costs have been developed. In particular, designs utilising transformerless topologies have steadily increased. While there are clear associated advantages of implementing these new transformerless topologies, new potential issues such as DC current injection and capacitive leakage currents are introduced.

Part A of this report presents a clearly defined test circuit setup and procedure for testing DC current injection for grid-connected single-phase photovoltaic inverters implementing both transformerless and high frequency transformer topologies. The results demonstrated that the test circuit setup and testing procedure is suitable for inclusion in a future amendment to AS4777.2. It is however proposed that before these amendments are recommended, further investigation is required to determine what power levels all inverters are required to be tested at and how many tests per inverter are required.

Part B of this report defines and models a variety of transformerless inverter topologies, switching schemes and output filter configurations and clearly defines their operation. All of these various models have been simulated to determine which designs are suitable for applications in regards to reducing capacitive leakage currents in an effort to eliminate potential risks to users and to ensure electromagnetic compatability. Two commercially available and one anonymous Grid-connected Transformerless Single-phase Photovoltaic Inverter models utilising a selection of the simulated topologies and switching schemes were experimentally tested to verify simulated results.

Disclaimer

I declare the following to be our own work, unless otherwise referenced, as defined by the University's policy on plagiarism.

Signed:

Date:

Academic Supervisor Endorsement Pro Forma

I am satisfied with the progress of this thesis project and that the attached report is an accurate reflection of the work undertaken.

Signed:

Date:

Acknowledgments

I would like to thank my academic supervisor Martina Calais for her ongoing assistance and support throughout the whole process of researching, formulating and writing this report. Without her assistance, the whole process would have seemed more daunting and confronting. In addition, Martina should be acknowledged for developing the initial thesis project topic.

Acknowledgement must also be given to all staff from the *Research Institute for Sustainable Energy* (RISE) for their assistance and supplying space and equipment to conduct all the necessary experiments and tests. Many thanks go to Colin Black, Wayne Clarke and Andrew Ruscoe for their assistance with setting up equipment and overseeing test procedures. In particular, I would like to thank Andrew Ruscoe for his continued supervision and support in performing tests and for helping shape the purpose and objective of certain procedures. Additionally, his countless hours of assistance with simulations were greatly appreciated and without them this work could not have been completed.

I would also like to thank coordinator Professor Parisa Bahri for her assistance throughout the last semester.

Contents

Grid-connected Transformerless Single-phase Photovoltaic Inverters: An Evaluation on DC Current Injection and PV Array Voltage Fluctuation i

Abstract ii

Disclaimer iii

Academic Supervisor Endorsement Pro Forma iv

Acknowledgments v

Contents vi

Figures x

Tables xv

Symbols xvi

Glossary xvii

1 Background Information 1

PART A: DC Current Injection 4

2 Introduction: 4

3 Review of International Standards 9

4 Test Circuit Setup 10

4.1 Modelled PV array (PV array simulator) 11

4.2 Selection of proposed inverters (IUT) 11

4.3 Circuit Breakers and High Speed Fuses 11

4.4 Power Meters 12

4.5 High precision shunt resistor 12

4.6 Digital Multimeter 12

4.7 Three Phase Variable Resistive Load Bank 13

4.8 Variable AC Power source 13
4.9 Environmental Testing Chamber 14
4.10 Temperature Probes 14
4.11 Data Logging Equipment 15
4.12 Testing Procedure 15
4.13 Start Up Procedure 15
4.14 Initial Temperature Set Points 16
4.15 Revised Temperature Set points 16
5 Experimental Results 18
6 Analysis of SMA SB500TL (Utilising a H5 Topology) Testing Results: 22
7 Analysis of Anonymous GCTSPPVI(Utilising a Fullbridge Topology) Testing Results: 24
8 Analysis of Sunways AT2700 (Utilising a HERIC Topology) Testing Results: 25
9 Discussion on Techniques Proposed to Minimise DC Current Injection 26
10 Recommendations and Future Work 27
PART B: PV Array Voltage Fluctuation 29
11 Introduction: PV Array Voltage Fluctuation 29
11.1 Literature Review 33
12 GCTSPPVI Topologies 35
12.1 Full Bridge topology 37
12.2 Bipolar Switching Scheme 37
12.3 Unipolar Switching Scheme 39
12.4 Half Bridge Topology 42
12.5 H5 Topology 43
12.6 HERIC Topology 45

13 Modes of Operation for GCTSPPVI 47

14 Simulating PV Array Voltage Fluctuation 51

14.1 Selection of Appropriate Modelling 52

14.2 Dead Time 53

14.3 Anti-paralleled Diodes 54

14.4 Switching States 54

14.5 PV Array 56

14.6 Switching Device Selection 57

14.7 Control Signal Generation 57

14.8 Diode Model Selection 60

14.9 Sizing of load 60

14.10 Sizing of LC Filter 60

15 Simulation Results 61

15.1 Simulations for a Fullbridge Converter Implementing a Bipolar Switching Scheme 61

15.2 Simulation of Fullbridge Converter Utilising a Standard Unipolar Switching Scheme 62

15.3 Simulations for a Fullbridge Converter Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter 64

15.4 Simulations for a Fullbridge Converter Utilising a One Phase Chopping Unipolar Switching Scheme (Type B) With Single Output Filter Inductor 65

15.5 Simulation of Halfbridge Converter with Single Inductor Output Filter 66

15.6 Simulation of Halfbridge Converter with Split Inductor Output Filter 67

15.7 Simulation of HERIC Topology 68

15.8 Simulation of H5 Topology 69

16 Test Circuit Setup 71

17 Experimental Results....72
18 Analysis of PV Array Voltage Fluctuations....74
19 Conclusions....77
20 Recommendations and Future Works....78
PART C: OVERVIEW OF REPORT....79
21 Conclusions and Final Comments....79
References....81
Appendix A: Additional Tables....83
Appendix B: Additional Calculations....87
Appendix C: Additional Figures....89
Appendix D: Additional Simulation Results....95

Figures

Figure 1: Simplified Illustration of Typical Current Control Scheme for Grid Connected Inverters 6
Figure 2: Testing Circuit Used to Measure DC Current Injection at RESlab 10
Figure 3: Measurements while the IUT's Internal Temperature Stabilises Followed by a Step Change to 30 Degrees Celsius 14
Figure 4: Initial Temperature Testing Procedure on 16/09/09 16
Figure 5: Plot of DC Current Injection and Inverter Heat Sink Temperature Taken on 16/09/09 18
Figure 6: Plot of DC Current Injection and Internal Inverter Temperature Taken on 18/09/09 18
Figure 7: Plot of DC Current Injection and Internal Inverter Temperature Taken on 23/09/09 19
Figure 8: Plot of DC Current Injection and Internal Inverter Temperature Taken on 16/10/09 19
Figure 9: Plot of DC Current Injection and Internal Inverter Temperature Taken on 21/10/09 20
Figure 10: Plot of DC Current Injection and Internal Inverter Temperature Taken on 28/10/09 20
Figure 11: Plot of DC Current Injection and Internal Inverter Temperature Taken on 30/10/09 21
Figure 12: Plot of DC Current Injection with Two Minute Moving Averages and Internal Inverter Temperature Taken on 18/09/09 22
Figure 13: Labelled Junction Voltages of a Fullbridge Topology 29
Figure 14: Capacitive Leakage Current Travelling through a Person 30
Figure 15: Cross Section Model of Typical PV Array and Framing 31
Figure 16: **A-**Capacitance between Cells and Front Glass Panel, **B-** Capacitance between Cells and Back Plate, **C-**Capacitance between Cells and PV Frame, **D-**Combined

Capacitance between all Cells and Front Glass Panel in Addition to Capacitance between Cells and Frame when Array is exposed to Moisture 32
Figure 17: Full Bridge Converter Topology 35
Figure 18: Halfbridge Converter Topology 36
Figure 19:H5 Topology 36
Figure 20: HERIC topology 37
Figure 21: Bipolar (Two Level) Switching Scheme 38
Figure 22: **A-**Current Path for Fullbridge Converter implementing Bipolar Switching Scheme during Switching State 1, **B-**Current Path for Fullbridge Converter implementing Bipolar Switching Scheme during Switching State 2 38
Figure 23: Unipolar (Three Level) Switching Scheme 41
Figure 24: **A-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 1, **B-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 2, **C-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 3 **D-** Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 4 42
Figure 25:**A-** Current Path for Half Bridge Converter during Switching State 1, **B-**Current Path for Half Bridge Converter during Switching State 2 43
Figure 26: **A-**Current Path for H5 Topology during Switching State 1, **B-**Current Path for H5 Topology during Switching State 2, **C-** Current Path for H5 Topology during Switching State 3, **D-** Current Path for H5 Topology during Switching State 4 44
Figure 27: Current Path for HERIC Topology during Switching State 1 46
Figure 28: Output Voltage of Fullbridge Utilising Unipolar Switching Scheme with Selected Operation Point of 0.5× $VOUT - max$ 48
Figure 29: PWM Pulse Output (VJ)at Selected Operating Point 49
Figure 30: Split Inductor Current (IL) at Selected Operating Point 49
Figure 31: **1-**Current Path of GCTSPPVI implementing One Phase Chopping Unipolar Switching Scheme during Operating Mode 1, **2-**Free Wheeling Current path of

GCTSPPVI implementing One Phase Chopping Unipolar Switching Scheme during Operating Mode 2 50
Figure 32: Front End Boost Converter 53
Figure 33: RC Filter used to Implement Dead Time 54
Figure 34: Scenario of Operating with One Closed Switch Resulting in a Fault 56
Figure 35: Comparator inputs for generating high frequency PWM control signal for GCTSPPVI Implementing a Bipolar Switching Scheme 58
Figure 36: Comparator inputs for generating high frequency PWM control signal for GCTSPPVI Implementing a Unipolar Switching Scheme 59
Figure 37: ICAP Simulation of PV Array Voltage Fluctuation for Fullbridge Topology Implementing a Bipolar Switching Scheme with a Split Inductor Output Filter 61
Figure 38: Output Voltage Generated by a Fullbridge Topology Implementing a Bipolar Switching Scheme with a Split Inductor Output Filter 62
Figure 39: PV Array Voltage Fluctuation for Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter 62
Figure 40: High Resolution of PV Array Voltage Fluctuation at Zero Crossing for a Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter 63
Figure 41: Output Voltage Generated by a Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter 63
Figure 42: PV Array Voltage Fluctuation for Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme(Type B) with a Split Filter Inductor Output Filter 64
Figure 43: High resolution of PV array voltage fluctuation at Zero Crossing of Output Voltage for a Fullbridge Topology implementing One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter 64
Figure 44: Output Voltage Generated by a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter 65

Figure 45: PV Array Voltage Fluctuation of Fullbridge Topology Implementing a One Phase Chopping Switching Scheme (Type B) with a Single Output Filter Inductor 65
Figure 46: Output Voltage Generated by a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Single Inductor Output Filter 66
Figure 47: PV Array Voltage Fluctuation for Halfbridge Topology with Single Inductor Output Filter 66
Figure 48: Output Voltage Generated by a Halfbridge Topology with a Single Inductor Output Filter 67
Figure 49: PV Array Voltage Fluctuation for Halfbridge Topology with Split Inductor Output Filter 67
Figure 50: High resolution of PV array voltage fluctuation at Zero Crossing of Output Voltage for a Halfbridge Topology Implementing a Split Inductor Output Filter 68
Figure 51: PV Array Voltage Fluctuation for a HERIC Topology with a Split Inductor Output Filter 68
Figure 52: Output Voltage Generated by a HERIC Topology with a Split Inductor Output Filter 69
Figure 53: PV Array Voltage Fluctuation for a H5 Topology (with Total Array to Earth Capacitance of 21nF) with a Split Inductor Output Filter 69
Figure 54: Output Voltage Generated by a H5 Topology with a Split Inductor Output Filter 70
Figure 55: PV Array Voltage Fluctuation for Fullbridge Topology Implementing Bipolar Switching Scheme with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV 72
Figure 56: PV Array Voltage Fluctuation for HERIC Topology with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV.....72

Figure 57: PV Array Voltage Fluctuation for H5 Topology with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV.....73
Figure 58: Comparator Output of H5 Topology.....76
Figure 59: Output of Comparator After two Schmitt Inverters.....76
Figure 60: ICAP Model of Fullbridge Converter Implementing Bipolar Switching Scheme 89
Figure 61: ICAP Model of Fullbridge Converter Implementing One Phase Chopping Unipolar Switching Scheme (Type B).....90
Figure 62: ICAP Model of Fullbridge Converter Implementing Unipolar Switching Scheme [19].....91
Figure 63: ICAP Model of Halfbridge with Single Filter Inductance.....92
Figure 64: Halfbridge with Split Filter Inductance.....92
Figure 65: ICAP Model of HERIC Topology.....93
Figure 66: ICAP Model of H5 Topology.....94
Figure 67: PWM control Signal for Switches of Fullbridge Topology Implementing a Bipolar Switching Scheme at a Switching Frequency of 1kHz.....95
Figure 68: Control signals for a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) at a Switching Frequency of 1 kHz.....95
Figure 69: Control signals for a Fullbridge Topology Implementing a Unipolar Switching Scheme at a Switching Frequency of 1 kHz [19].....96
Figure 70: Control signals for a HERIC Topology Implementing at a Switching Frequency of 1 kHz.....97
Figure 71: signals for a H5 Topology Implementing at a Switching Frequency of 1 kHz 97

Tables

Table 1: Table of Symbols xvi
Table 2: Effect of DC Current Injection on Electrical Equipment [3] 4
Table 3: Summary on GCTSPPV Tested with Respect to DC Current Injection..... 11
Table 4: Switching States for Bipolar Switching Scheme for a Fullbridge Converter 38
Table 5: Switching States for Standard Unipolar Switching Scheme for a Full bridge Converter [19] 40
Table 6: Switching States for One Phase Chopping Unipolar Switching Scheme (Type A) for a Full bridge Converter [15]..... 40
Table 7: Switching States for One Phase Chopping Unipolar Switching Scheme for a Full bridge Converter(Type B) [9] 40
Table 8: Switching States of Bipolar Switching Scheme for Halfbridge Converter..... 43
Table 9: Switching States for Unipolar Switching Scheme for Inverter with a H5 Topology..... 44
Table 10: Switching States for Unipolar Switching Scheme for Inverter with a HERIC Topology..... 45
Table 11: Various Switching Schemes and Associated Voltage Fluctuations 74
Table 12: Summary of Comparison between Experimental Results and Simulations.... 75
Table 13: Standards Regarding DC Current Injection for GCTSPPVI 84
Table 14: Calculated Maximum DC Current Injection Levels..... 84
Table 15: ICAP Model Component selection and Sizing 86

Symbols

Symbol	Description
$V_j = V_{A-earth} - V_{B-earth}$	Junction Voltage
$i_{leakage}$	Capacitive Leakage Current
C_{array}	Accumulated Capacitance of the PV Array and Framing with Respect to Earth
$V_{A-earth}$	The Voltage at Point A with Respect to Earth
$V_{B-earth}$	The Voltage at Point B with Respect to Earth
$V_{common\ \ mode}$	Instantaneous Common Mode Voltage
$\frac{dV_{DC-earth}(t)}{dt}$	PV Array voltage Fluctuation with Respect to Earth
V_{OUT}	Output Voltage of GCTSPPVI
V_L	Output Filter Inductance Voltage
ΔV	Absolute DC Voltage Input
V_{grid}	Grid Voltage
$Z_{total\ L}$	Total Impedance of Inductance of Output Filter
R_{Load}	Resistive Load
P_{Rated}	Rated Power Output
ω_C	Angular Frequency of Capacitor
$f_{switching})$	Switching Frequency
$t_{switching}$	Switching Period

Table 1: Table of Symbols

Glossary

AC: Alternating Current

DC: Direct Current

DMM: Digital Multimeter

GCHFTSPPVI: Grid connected High Frequency Transformer Single-Phase Photovoltaic Inverter/s

GCTSPPVI: Grid Connected Transformerless Single-Phase Photovoltaic Inverter/s

GCSPPVI: Grid Connected Single-Phase Photovoltaic Inverter/s

EMC: Electromagnetic Compatibility

EMI: Electromagnetic Interference

Galvanic Isolation: Ensuring one section of an electrical system is not physically connected to another section.

Grid-connected: A system with its output connected to the mains utility grid

Half wave: The half cycle of a sine wave where the output is either positive negative

IGBT: Insulated-Gate Bipolar Transistor. A power electronics device which can be used as a switch

Inverter: An electronic device used to convert a DC input into an AC output

IUT: Inverter/s Under Testing

MOSFET: Metal oxide semiconductor field effect transistor. A power electronics device which can be used as a switch

MPPT: Maximum Power Point Tracking

NPLC: Number per Line Cycle

PWM: Pulse Width Modulation

PV: Photovoltaic

RCD: Residual Current Device

Single-phase: AC power where the direction of the current is in phase with its self and the direction of all the voltage is in phase with its self

SWIS: South West Interconnected System

THD: Total Harmonic Distortion

1 Background Information

Recent environmental and political factors have seen an increase in the demand for renewable energy technologies in both an international and Australian context. This steadily increasing demand has resulted in improvements of Photovoltaic (PV) technology in the past two decades. Grid connected inverters are no exception with the continued improvement in areas including power electronics resulting in higher efficiencies and lower manufacturing costs. Increased Australian Government incentives for grid connected PV systems and the general public's increased knowledge and awareness of environmental issues of power generation and a more positive attitude towards renewable energy have seen a steady increase in the demand for PV systems and hence grid connected inverters. As a result, new topologies for grid connected inverters providing higher efficiencies and lower manufacturing costs have been developed. In particular, designs utilising transformerless topologies have steadily increased.

The last few years have seen more and more Grid-connected Transformerless Single-phase Photovoltaic Inverters (GCTSPPVI) enter the Australian market [1]. While there have been no documented findings as to the current market share of GCSPPVI being transformerless in the Australian market, it is not unreasonable to expect the Australian PV market to follow the European trend which has shown a steady increase in the percentage of GCTSPPVI installed compared to the overall Grid-connected Single-phase Photovoltaic Inverter (GCSPPVI) market [1].

Transformerless topologies have several associated benefits against designs using topologies with line or high frequency transformers. From a practical perspective, transformerless topologies reduce the size and mass of inverters. The initial cost of the inverter is also typically reduced. Perhaps the most advantageous aspect of transformerless inverters is their increased efficiency at low and partial load. As no reactive power is required for the magnetising of the transformer windings, losses are

reduced and the power factor is also typically higher than that of inverters using transformers at low and partial load[2]. With the number of installed GCTSPPVI steadily increasing because of their benefits mentioned above, it is necessary to ensure that all transformerless inverter designs operate in a safe manner with no risk to users or installers and do not cause damage to existing appliances and the mains utility grid.

While the associated advantages of transformerless topologies are apparent, there has not been adequate investigation into potential safety, longevity and performance issues. The removal of a transformer inside the inverter introduces several potential issues. These issues include:

- No galvanic isolation between AC and DC sections of the inverter. This could be a potential safety issue in the case of a fault.
- The injection of DC current into the AC network. This is a potential concern in terms of the effect DC current may have on the performance of the utility grid and in particular, distribution transformers and electro mechanical power meters [1, 3].
- PV array voltage fluctuation. These voltage fluctuations are potentially hazardous due to induced capacitive leakage currents.
    - Capacitive leakage currents could be of a large enough magnitude to cause a reflex in a person [1].
    - Capacitive leakage currents can cause issues regarding EMC [3]
    - Capacitive leakage currents are believed to have non-reversible detrimental effects on the structure of the thin-film arrays[2]. As the associated high efficiency of thin film technologies as well as manufacturing costs becoming more and more competitive with mono and polycrystalline arrays, Australia will continue to see an increase in thin film arrays[4].

This report will investigate the final two points with part A investigating DC current injection and part B investigating PV array voltage fluctuation.

PART A: DC Current Injection

2 Introduction:

Inverter topologies which incorporate transformer at the output of the switching stage of an inverter ensure the DC input is isolated from the AC side. This is because after the input has been inverted through some form of switching scheme, the inverted current and resulting change in magnetic field on the primary coil induces a current and corresponding voltage on the secondary coil [5]. There is therefore no galvanic connection between the DC and AC sides. Without a transformer between the DC and AC sides, DC current can flow to the AC terminals. This can also be an issue in topologies implementing high frequency transformers (GCHFSPPVI) because there are stages between the high frequency transformer and the AC output which are capable of producing current with a DC offset. This is not a desirable outcome because in the case of a grid-connected inverter, the stray DC current could potentially flow through devices such as distribution transformers, current transformers, energy meters, RCDs or other sensitive devices [3]. Past literature has identified this issue resulting in research into determining what levels of DC current injection are acceptable [1] and [3]. The potential associated impact of this stray DC current is presented in Table 2.

Equipment	**Effect of DC Current Injection**	**Associated Risks**
Distribution Transformer	Saturation Lower Efficiency	Decreased Life Span Premature Failing
RCD	Modification of Tripping Characteristics	Reduction in Sensitivity
Current Transformers	Saturation	Error in Measurements- Potential Safety Issue
Electromechanical Energy Meters		Error in Measurement

Table 2: Effect of DC Current Injection on Electrical Equipment [3]

The issue of DC current injection due to GCTSPPVI has been recognised both internationally and from an Australian perspective with both Australian standards and most international standards stating some regulation in terms of inverters not exceeding a maximum level of DC injection. In order for GCTSPPVI to comply with these various standards, a sophisticated active method of controlling the output current and therefore limiting DC current injection is required. In a current controlled grid connected inverter, this is typically achieved by comparing a reference current waveform to the current output. In this report it is proposed that possible causes of DC current injection include:

- An inaccuracy from the device used in the feedback loop to measure the output current [6]
- A DC offset in the current reference waveform [3]
- Asymmetry in the switching of power semiconductors [6]

In regards to inaccuracies from the measuring device of DC injection, the measurement of a small DC component is exceedingly difficult when the AC current is rapidly fluctuating and is of a magnitude sometimes nearly a thousand times greater. Additionally, current measuring devices such as Hall Effect sensors are susceptible to nonlinearity and offsets. A recent study commented on this issue: *'It is impossible to limit, with any level of certainty, the dc component in the inverter output with better accuracy than that of the current measurement Device '* [6].While other current measuring devices such as resistive shunts and current transformers exist in the market, Hall Effect sensors are most widely used because of their relatively low costs and galvanic isolation [6]. As resistive shunts also drift with respect to temperature, it is not of great concern which current measuring device is implemented however it is assumed in this report that the majority of GCSPPVI implement Hall Effect sensors. Figure 1 demonstrates a highly simplified example of how a typical current control method can be implemented for a grid connected inverter. As can be seen, in a typical current controlled grid connected inverter, the output current is measured and compared to a reference waveform. Depending on whether the output current is

higher or lower than the reference signal and which halfwave the reference waveform is operating in, the controller will send a varying control signal to each switching device resulting in different switching states [7].

This comparison between the output and reference signal is continuously updated which results in the generation of a PWM signal. If the current measurement device has an inherent DC offset, the resulting control signals applied to all switching devices will result in an offset (DC component) at the output.

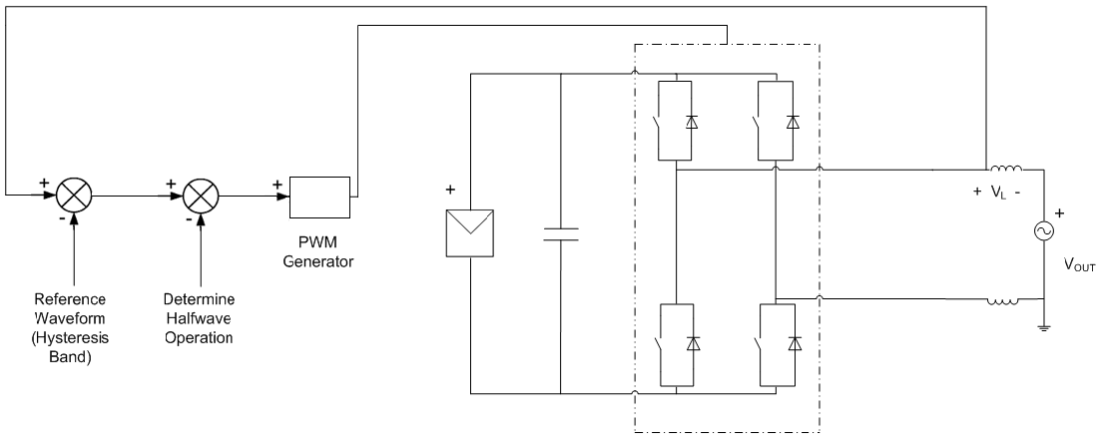

Figure 1: Simplified Illustration of Typical Current Control Scheme for Grid Connected Inverters

While there have been papers presenting prototype current control techniques to eradicate DC current injection incorporating concepts such as self calibrating current sensing devices [6] and virtual DC current blocking capacitors[8], it is not known if these concepts have been adopted by GCTSPPVI manufacturers as this level of detail on implemented control is not available.

In the case of the second point, an error in the reference signal may occur for several reasons. Firstly, the DC component or offset of a sinusoid can be described as the difference between the positive and negative half wave of the output. As even harmonics distort the difference between the positive and negative half wave, even

harmonic content of the reference signal can impact the magnitude of DC offset [3]. In the case of some current controlled GCTSPPVI, the actual grid is used as the reference signal. The grid is not a perfect sinusoid and has a certain even harmonic content which would influence the DC current content.

It should be noted however that reducing these harmonic components have been addressed by implementing a zero shift phase filter [9]. Based on conversations with former staff of an anonymous GCSPPVI manufacturer, it is the opinion of this report that most modern GCTSPPVI which are current controlled typically generate the reference signal by using a microprocessor. As this waveform would be produced from a modelled sinusoid, there would be no harmonics however this report proposes it is still possible to have a small DC offset in the reference signal as there may be issues with the zero crossing values.

The final cause is that semiconductor devices are not ideal switches and have delays with acting open or closed. There are also delays and inaccuracies and mismatches in the control signals determining the state of each switching element [6]. These factors can result in producing a DC offset.

It should be noted, that while this report has outlined three causes of DC current injection in GCTSPPVI, it is assumed that the primary cause of DC current injection is the error in implemented current measurement devices due to their temperature dependency. The current Australian standard AS4777.2 is quite vague and non specific in regards to DC current injection. The purpose of Part A of this thesis project was to investigate and attempt to verify a dependent relationship between DC current injection and internal inverter operating temperature and more specifically, the internal current measuring device.

If this dependency was successfully verified, the test circuit setup and procedure to verify the dependency could be used to recommend possible amendments to AS4777.2 to regarding test circuit setup and testing procedure. The associated advantage of this is that by having a more specific standard, testing will be consistent and it provides

manufacturers with a more strict procedure which in term should assist them to design GCTSPPVI that comply with AS4777.2.

3 Review of International Standards

The intended purpose of sourcing and reviewing various international standards with regards to DC current injection was to investigate how other countries limit and test DC current injection to assist in the design of a suitable DC current injection test circuit setup and procedure. Additionally, the proposed DC current injection testing procedure was also influenced by suggestions from several sources including views expressed by domestic inverter retailers following the distribution of the paper [1]. This indicates that the Australian market also believes amendments to the current AS4777.2 are required. Table 13 which can be found in Appendix A outlines the various requirements regarding DC current injection levels for grid connected single phase inverters imposed by various international standards. Possible amendments made to AS4777.2 would require information concerning:

- The method used to measure the DC current injection (test circuit)
- Clarification on whether the value of 5mA or 0.5% of the inverters rated current is a maximum value or averaged over a period of time
- How long each testing procedure should run for
- The number of required test per Inverter Under Testing (IUT)
- For what power levels of the inverter the DC current measurements should be taken at
- What external conditions (temperature) should the inverter be exposed during testing

All these issues were investigated and clarified in the test circuit setup and procedure outlined below.

4 Test Circuit Setup

As it was known that previous measurements of DC current injection had resulted in non-repeatable results [1], a major consideration in designing the test circuit setup was to produce results which could be reproduced at another time. The test circuit illustrated in Figure 2 was designed with this in mind by eliminating any undesired variation in any variables. All testing equipment was supplied by RISE and tests were conducted at the RESlab.

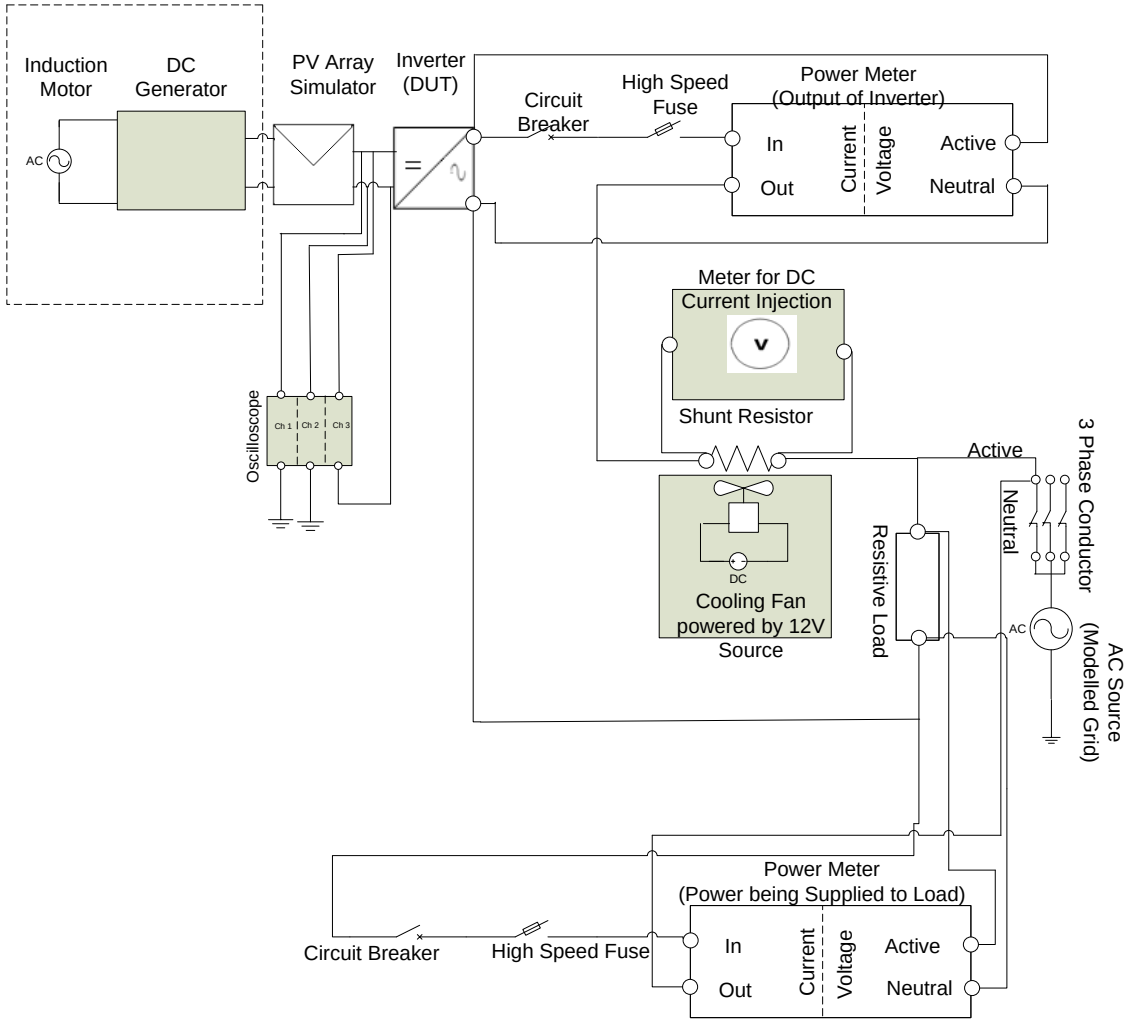

Figure 2: Testing Circuit Used to Measure DC Current Injection at RESlab

The testing circuit consisted of the following laboratory equipment:

4.1 Modelled PV array (PV array simulator)

A PV array simulator was used to model the I-V characteristics of a PV array under a constant solar radiation level. As Figure 2 demonstrates, the PV array simulator was supplied by a DC generator which was driven by an AC induction motor. This input was selected instead of rectifying a supply from the grid because it was desired for the PV simulator to produce a floating voltage output. As the grid is effectively grounded, a mains frequency transformer would be required to ensure the output of the PV simulator may not be floating if supplied by the grid. Additionally, as the PV array simulator can vary the input voltage, this method can achieve this simply by changing the field windings of the DC generator. Furthermore, this method is advantageous over a grid connected rectifier as there is very little harmonic content.

4.2 Selection of proposed inverters (IUT)

The following three GCTSPPVI were connected into the DC current injection test circuit as illustrated in Figure 2. A comprehensive analysis an explanation on the various implemented topologies is given in Chapter 12of this report.

Inverter Company and Model	**Topology**	**AC Rated Power**	**AS4777 Certified**
Anonymous GCTSPPVI (not commercially available)	Fullbridge converter	1.5 kW	No
Sunways AT2700	HERIC	2.7 kW	No
SMA SB5000TL	H5	4.6 kW	Yes

Table 3: Summary on GCTSPPV Tested with Respect to DC Current Injection

4.3 Circuit Breakers and High Speed Fuses

The circuit breakers and high speed fuses were used as primary and secondary sources of protection against the high precision power meters in the event of a fault condition. As power meters require the current to flow through the device, a current surge in the system as a result of a fault could potentially damage the meter.

4.4 Power Meters

Two separate power meters were used to measure the power supplied by both the GCTSPPVI being tested and the AC power source. The first power meter was connected in the manner illustrated in Figure 2 to measure the power being supplied by the CGTSPPVI to the load bank. The second power meter was connected to measure and display the total power supplied to the load bank. The power supplied to the load bank by the AC power source was measured on a second channel of one of the power meters.

4.5 High precision shunt resistor

The method used to measure DC current injection levels was by measuring the DC voltage drop across a high precision shunt resistor. While the use of resistive shunts is not a particularly popular method of DC measurement for GCTSPPVI manufacturers because of the voltage drop across the shunt and associated losses, the efficiency of the testing circuit will have no impact on the accuracy of the DC current injection measurements therefore making it an acceptable method to measured the DC current injection. The measured DC current injection is extremely accurate due to the low uncertainty of the value of the shunt resistor and the high precision of the digital multimeter used. The high precision shunt has been confirmed be 9.99799 mΩ for a current of 20A with an uncertainty of $\pm 3\frac{\mu\Omega}{\Omega}$. This value is maintained by encasing the shunt in a case with a high speed fan to maintain a constant temperature. As illustrated in Figure 2, the shunt was connected between the active terminal output of the inverter and the load bank ensuring that only the DC current injected by the inverter is being measured.

4.6 Digital Multimeter

The DMM used (Agilent 3458A) to measure the voltage drop across the shunt resistor was calibrated before every test and had an auto-zero function which makes internal corrections for internal offsets or drifts due to temperature [10]. As all connections made to the DMM were using the back terminals, the front terminals were used whilst the device was being calibrated so that there was no possibility of calibrating the device to a disturbance. The Numbers Per Line Cycle (NPLC) which is defined as the integration time or sampling rate of the device was set to 100. As the South West Interconnected System (SWIS) power lines cycle is 50 Hz, an NPLC corresponds with converting the analogue

average of every two seconds and converting it to a digital signal. This method removes the mains differential mode AC voltage leaving only the DC injection. As the DC current is a small measurement by comparison to the AC current, it is important that the logged value is not influenced by noise. To ensure that the DC current injection measurements were accurate and calibrated correctly and external noise was not influencing measurements, the measurements were verified by “piggy-backing” the terminals of the DMM to one lead and connecting the lead to one of the shunt terminals. As the DMM was measuring a short circuit, the DC voltage drop was measured to be in the order of micro volts. To ensure non repeatable disturbance such as harmonic distortion were not present, the THD of the system was measured before several tests using one of the power meters. As the AC source was the only device in the system capable of creating significant distortion, the measured THD was of a constant 0.4% every time it was measured.

4.7 Three Phase Variable Resistive Load Bank

As all tested inverters were single phase, only one phase of the load bank was connected. The load was oversized for each inverter by 15 to 20 percent for the inverter operating at its rated output with the power source supplying the rest of the load.

4.8 Variable AC Power source

It was decided that connecting the output of the inverter to the SWIS (utility grid) could potentially introduce uncontrolled variables by way of THD and voltage flicker which may impact DC current injection measurements. As a result, a three phase AC source was implemented and connected to the load to model the grid. It should however be noted that while all IUT only produced single phase power, the Sunways AT2700 required three phases to be present at the output before it would produce an output. The AC power source was setup to produce an output AC voltage of 240 Volts RMS at mains frequency (50 Hz). The source was current limited to create a safety margin so that the source could not supply more power than the load. For example, when a 4.6 kW inverter was tested with the load sized at 7kW, the AC source was current limited to 25 Amps resulting in an output of 6 kW.

4.9 Environmental Testing Chamber

As it was believed the DC current injection of GCTSPPVI may be temperature dependent, it was required to be able to maintain a constant ambient temperature when desired and to be able to quickly increase or decrease the ambient temperature. The environmental temperature chamber was fitted with a sealed, airtight door and a fan forced cooler as well as a heater. Both the cooler and heater were controlled by a central system which would turn the devices on and off when appropriate based on what temperature set point was set by the user. An associated issue with the environmental chamber was the cyclical nature of the cooler. As a result, when the temperature of the chamber was manually set to low temperatures below the ambient temperature, the chamber temperature would oscillate by approximately five degrees. An example of this is given below.

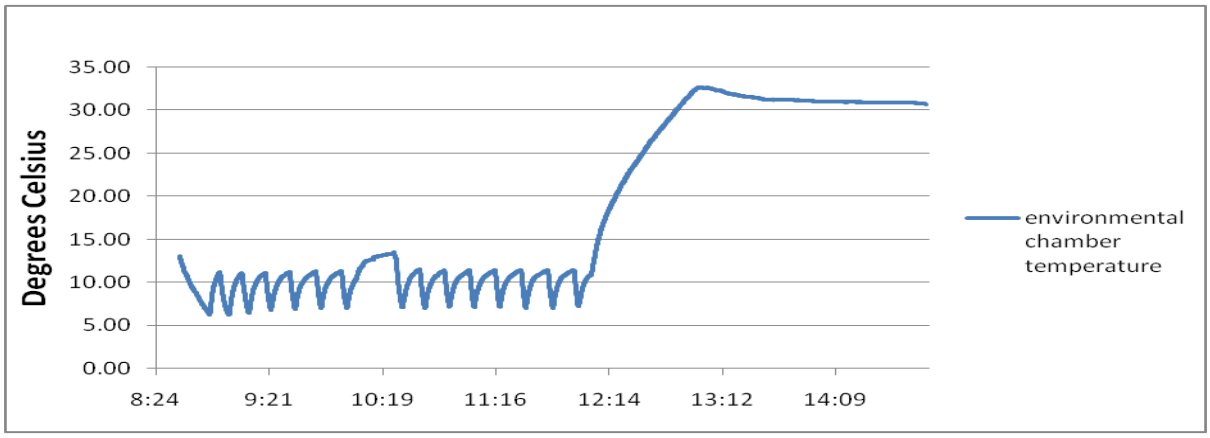

Figure 3: Measurements while the IUT's Internal Temperature Stabilises Followed by a Step Change to 30 Degrees Celsius

4.10 Temperature Probes

Three temperature probes were set up at various positions of the test circuit. The first temperature probe was positioned inside the environmental chamber which was used to ensure the temperature of the chamber was settling at the manually entered set points. The second probe was initially positioned to the heat sink of the IUT but was later repositioned inside the casing of the tested GCTSPPVI. As it was believed that DC current injection may be dependent on the temperature of the internal device used to measure DC current, the probe was positioned as close to the internal current control circuit and power semi-conductors as possible without coming into physical contact. Due to the

design of the Sunways inverter (HERIC topology), the casing could not be fully closed because of the wiring of the temperature probe. To ensure that the test setup had not impacted the thermal properties of the IUT, aluminium taping was used to seal the DUT making it thermally equivalent to having the casing fully closed. While this is clearly not a desirable setup for a test procedure to be used by a standard, it was adequate for verifying DC current injection's temperature dependency. The third temperature probe was placed outside the environmental chamber next to the rest of the test circuit. This temperature was solely used as a reference temperature to ensure that neither the chamber's nor internal inverter's temperature were tracking the ambient temperature.

4.11 Data Logging Equipment

Two different data logging programs were used to log the output of the DMM used to measure DC voltage drop across the shunt and the three different temperature probes with respect to time. The output of the DMM was logged with corresponding time stamps every 15 seconds using a LabVIEW program. The output of each temperature probe was logged with corresponding time stamps every 10 seconds using a program designed by Agilent.

4.12 Testing Procedure

In order to prove repeatability of results, all tests were conducted twice. All tests were conducted with the IUT being fully loaded by supplying a DC input corresponding with the inverter's rated output. The AC power source was sized with each GCTSPPVI to model the grid so that when the inverter was producing its rated output, a small portion of the load was supplied by the AC source. As the inverter output increases from zero to its rated output, the output of the AC source reduces by the corresponding amount.

4.13 Start Up Procedure

To ensure no power was being supplied without a load, the three phase load bank was the first piece of equipment to be sized and turned on. Once a load is present, the DC generator can be turned on along with the AC power source with the appropriate current limits imposed. Once the field windings of the DC generator had been increased to give the appropriate DC input of the PV simulator, the simulator program could be initiated to supply an appropriate DC input to the DUT.

4.14 Initial Temperature Set Points

As it was not initially known how long the environmental chamber would take to reach the set point or how long the IUT's internal temperature would take to stabilise, the first DC current injection test was proposed to set the environmental chamber to 20 degrees and then after a reasonable period of time had elapsed, to step the temperature down to 10 degrees. This procedure was applied to the SMA SB5000TL with the IUT's temperature being measured with a probe positioned on the heat sink. The environmental chamber and IUT's heat sink temperatures are displayed in Figure 4.

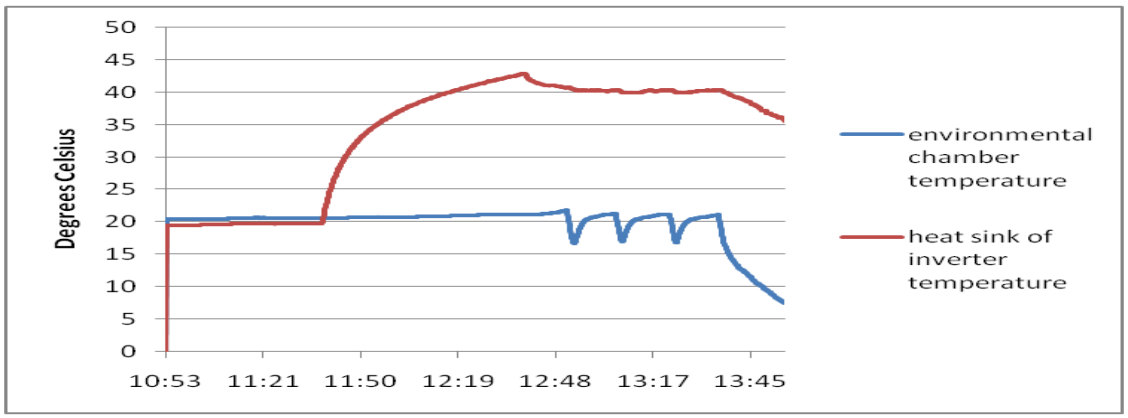

Figure 4: Initial Temperature Testing Procedure on 16/09/09

After plotting the temperature data, it became apparent that this test procedure was not satisfactory. As the heat sink temperature clearly decreased before a temperature step change was applied to the chamber, It was determined that the heat sink temperature could be influenced by the cool air supplied by the fan forced cooler. As a result, the temperature of the heat sink was not an accurate representation of the inverter's internal (current measuring device) temperature. After analysing the results from the first testing procedure, it was also decided that a step change of 10 degrees may not be large enough to show the extent of the temperature dependency of DC current injection. It was therefore decided to increase the temperature step change to a magnitude of 20 degrees Celsius.

4.15 Revised Temperature Set points

In each testing procedure, the same temperature step was applied. Initially, the environmental chamber was set to a set point of 10 degrees Celsius. After the internal

inverter temperature had stabilised, the set point environmental chamber was increased to 30 degrees Celsius. Once the internal inverter temperature had again stabilised at the second steady state, all testing equipment and was shutdown in the correct manner ensuring a load was always present whilst power was being generated.

5 Experimental Results

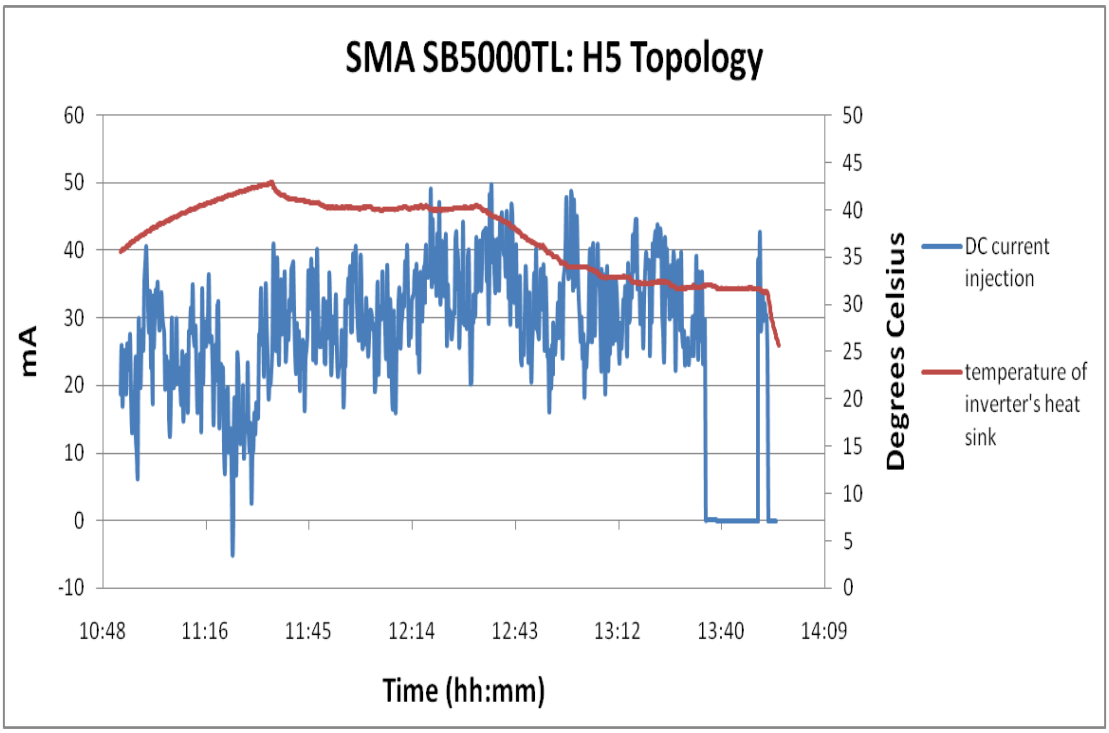

Figure 5: Plot of DC Current Injection and Inverter Heat Sink Temperature Taken on 16/09/09

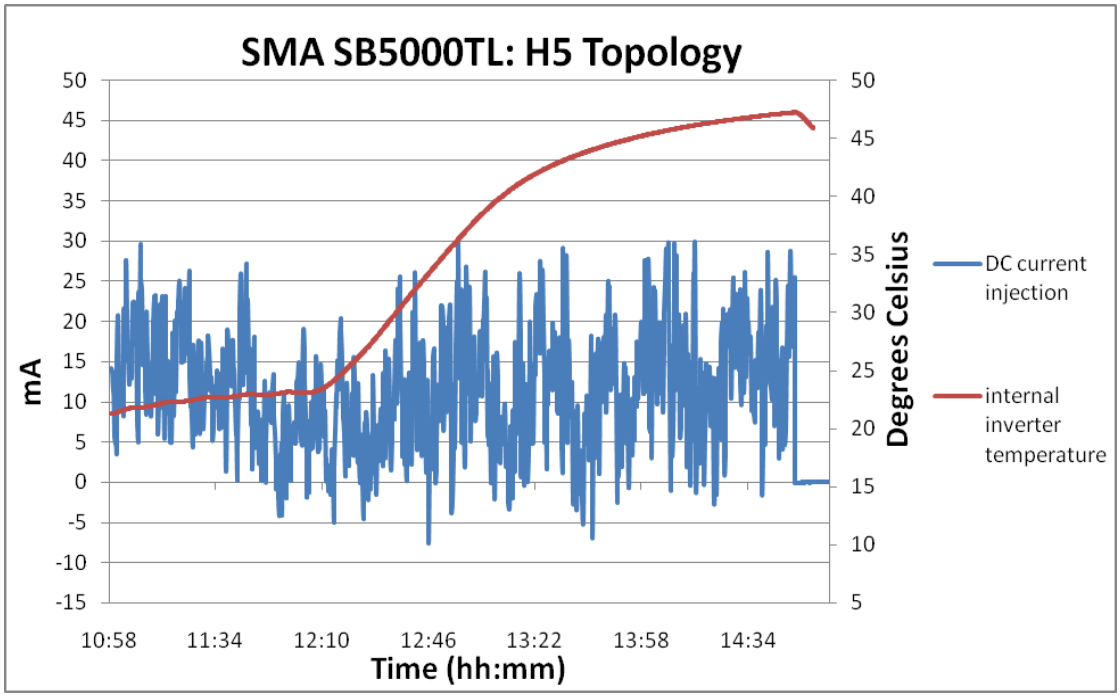

Figure 6: Plot of DC Current Injection and Internal Inverter Temperature Taken on 18/09/09

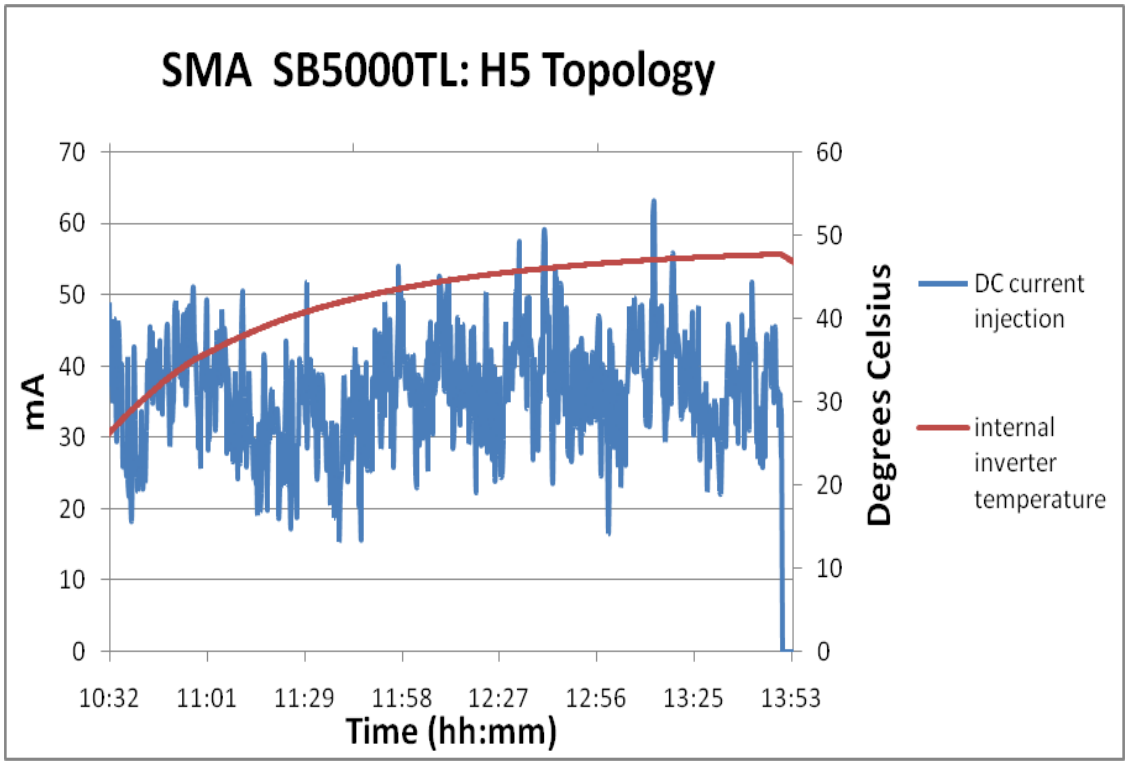

Figure 7: Plot of DC Current Injection and Internal Inverter Temperature Taken on 23/09/09

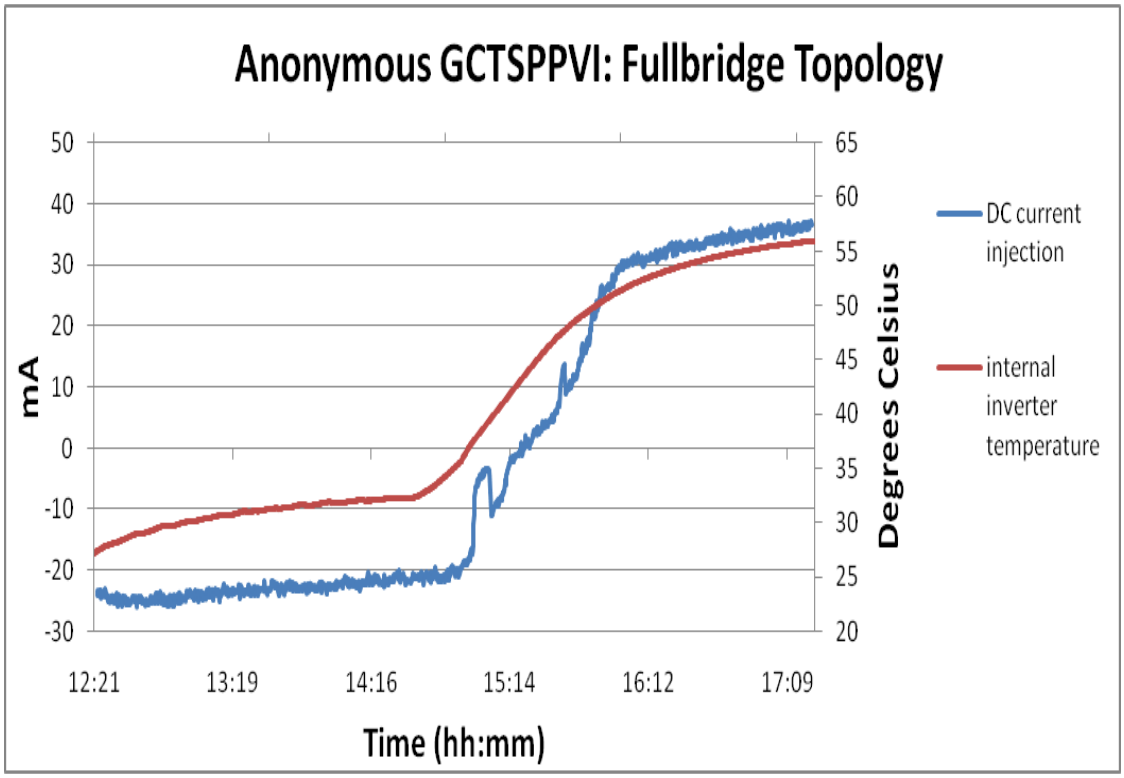

Figure 8: Plot of DC Current Injection and Internal Inverter Temperature Taken on 16/10/09

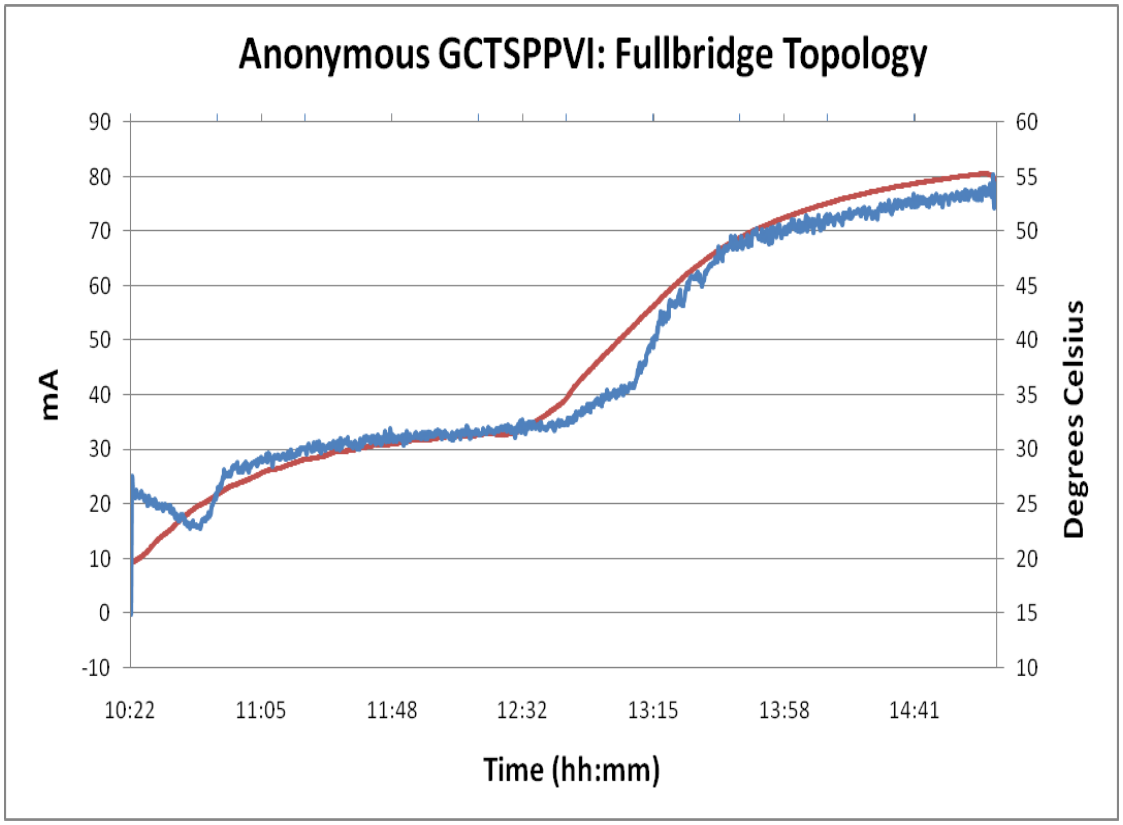

Figure 9: Plot of DC Current Injection and Internal Inverter Temperature Taken on 21/10/09

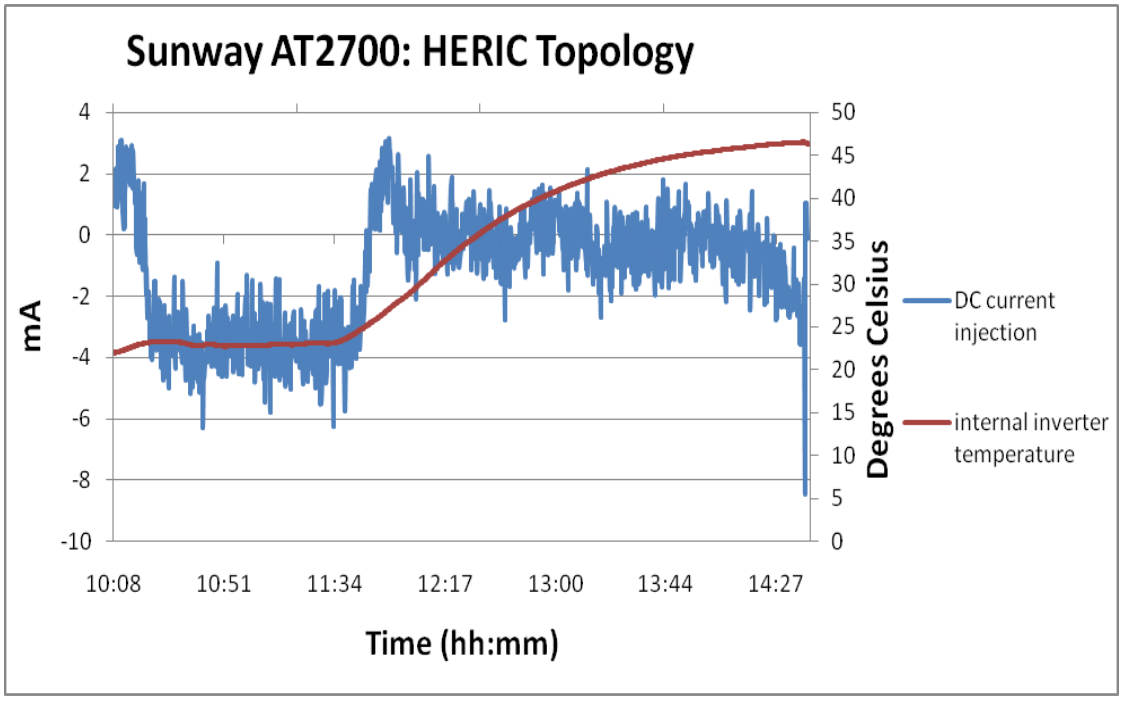

Figure 10: Plot of DC Current Injection and Internal Inverter Temperature Taken on 28/10/09

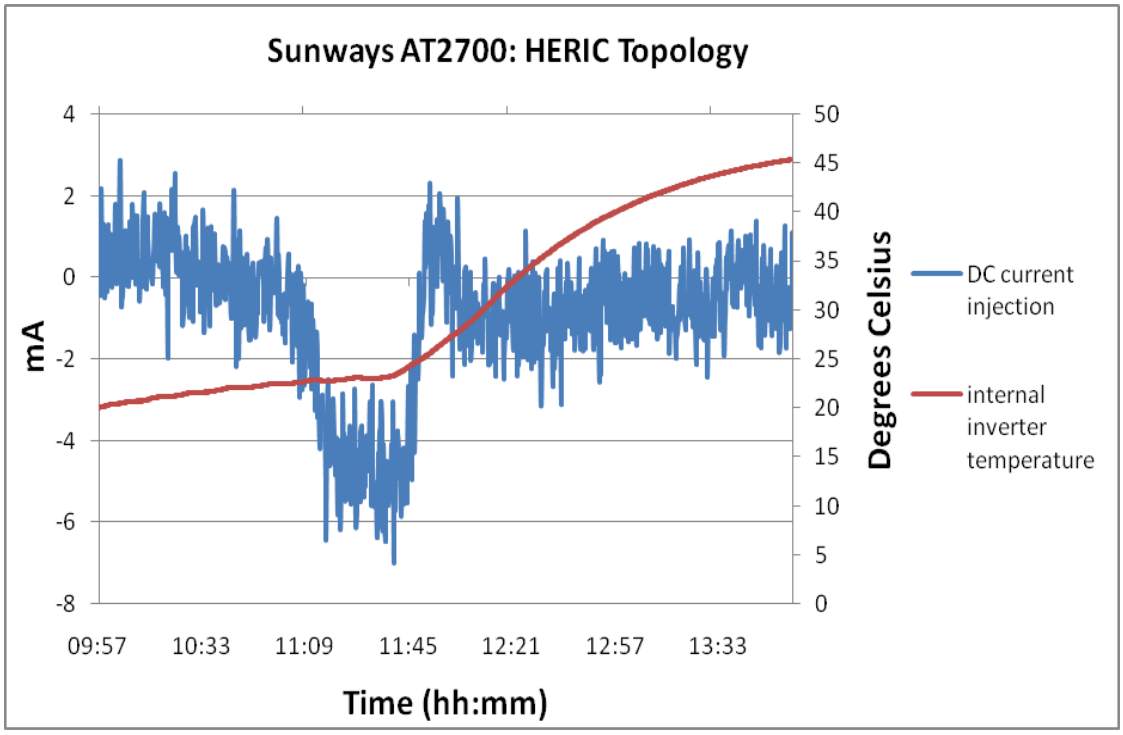

Figure 11: Plot of DC Current Injection and Internal Inverter Temperature Taken on 30/10/09

6 Analysis of SMA SB500TL (Utilising a H5 Topology) Testing Results:

The maximum tolerable DC injection level allowed by AS4777.2 for an inverter with a nominal output of 4.6 kW was calculated to be 95.83mA. As Figures 5, 6 and 7 demonstrate, the SMA SB5000TL was well below this level during all tests and was therefore in accordance with AS4777.2 during all tests. All DC current injection limits for each tested inverter to comply in AS4777.2 are calculated in Table 14 found in the Appendices.

As the heat sink temperature of the SMA SB5000TL during the first test was influenced by external conditions (cool air from cooler), no useful conclusions can be drawn from the results. Therefore, the only figures of interest are 6 and 7. As the DC current injection fluctuated greatly, a two minute moving average was taken and is illustrated below.

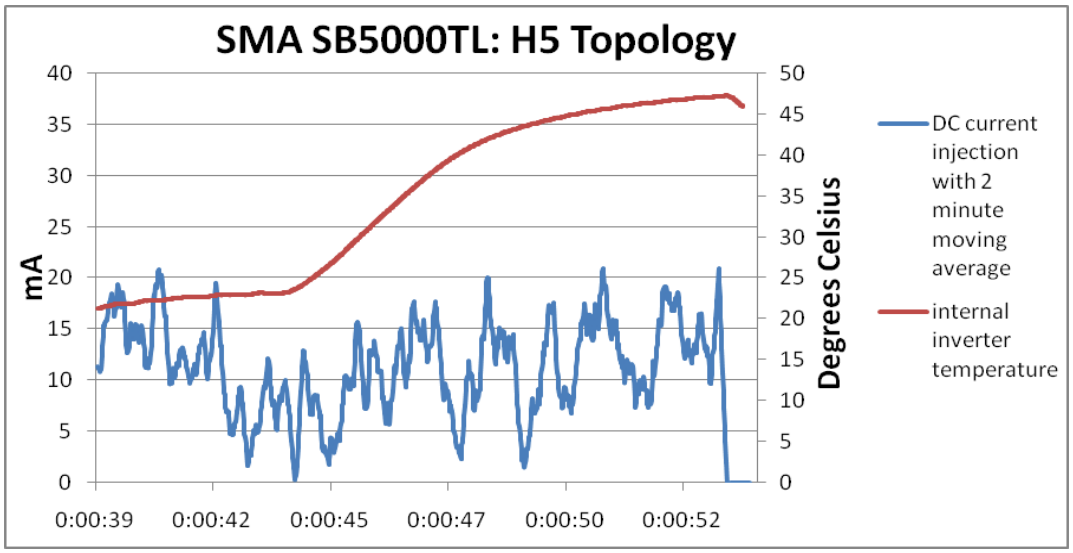

Figure 12: Plot of DC Current Injection with Two Minute Moving Averages and Internal Inverter Temperature Taken on 18/09/09

While Figure 12 still has an oscillating "noisy" component, it clearly demonstrates a decrease in DC current injection when the internal inverter temperature stabilises

while the environmental chamber is at 10 degrees. Once the new set point of 30 degrees is applied to the environmental chamber and the internal inverter temperature increases, the DC current injection levels increase once again. It could be argued that this demonstrates a relationship between the DC current injection of the SB5000TL and operating temperature. However as the initial test procedure regarding set points was not deemed adequate and the third test did not include the initial 10 degree step change to 10 degrees; there is not sufficient evidence to confirm this. A second test including the initial step change to 10 degrees and then the step change to 30 degrees would be required to verify this trend.

One thing that is clearly indicated is that for the SB5000TL, the DC current injection is not directly proportional to the internal inverter temperature. It appears that when the inverter temperature stabilises, the current control method is able to reduce DC current injection, however when the temperature changes, the current control method implemented can not limit the DC current injection to the same levels. This level of detail regarding the control method of the SB5000TL however is not available and further tests would be required to verify this.

Another issue which became apparent while comparing Figure 6 and Figure 7 was that DC current injection levels were not repeatable for the same internal inverter temperature. When the internal inverter temperature stabilised after the environmental chamber step change to 30 Degrees Celsius, levels during the first test typically ranged from -5 to 25 mA. However during the second test procedure, levels were typically in the range of 20 to 50 mA. As the range of variation is similar (30 mA) with all values being approximately 25mA higher during the second test and given both testing procedures were the same with no uncontrolled variables, this indicates that a residual offset of some sort may have remained from the initial test procedure.

7 Analysis of Anonymous GCTSPPVI(Utilising a Fullbridge Topology) Testing Results:

The maximum tolerable DC injection level allowed by AS4777.2 for an inverter with a nominal output of 1.5kW was calculated to be 31.25 mA. As Figure 8 and Figure 9 demonstrate, the IUT exceeded this level during for both tests and as a result, was not in compliance with AS4777.2.

As can be seen in Figure 8 and Figure 9, the DC current injection is clearly directly proportional to the internal inverter temperature. During both test procedures, the DC current injection levels stabilise when the internal inverter temperature stabilises and immediately increase when a step change is applied the environmental chamber temperature.

As was the case with the SB5000TL inverter, there was an issue with repeatability of the magnitude of the relative variation of the DC current injection levels during the testing of the inverter utilising a fullbridge converter. While both test procedures on the anonymous GCTSPPVI resulted in the same temperature dependency, the first test saw values vary from 35 to -25mA where as the second test saw values vary from roughly 80mA to 30mA. As the variation from maximum to minimum is similar (50mA) for each test with all values in the second test being approximately 45mA higher and the procedure was the same with no uncontrolled variables, this indicates that a residual offset of some sort may have remained from the initial test procedure.

8 Analysis of Sunways AT2700 (Utilising a HERIC Topology) Testing Results:

The maximum tolerable DC injection level allowed by AS4777.2 for an inverter with a nominal output of 2.7kW was calculated to be 56.25 mA. As Figure 10 and Figure 11 demonstrate, DC current injection levels were well below this level during both tests and as a result and was therefore in compliance with AS4777.2.

While Figure 10 and Figure 11 still have an oscillating “noisy” component, a distinct temperature dependency in regards to the DC current injection can be seen. While the DC current injection levels are clearly not directly proportional to the internal inverter temperature, DC current injection levels drop significantly when the internal inverter temperature stabilises while the environmental chamber is at 10 Degrees. Once the new set point of 30 degrees is applied to the environmental chamber and the internal inverter temperature increases, the DC current injection levels rise immediately back to the same levels prior to the internal inverter temperature stabilising.

Unlike in the case of the other inverters tested, there were no issues with repeatability of the magnitude of variation of DC current injection levels. During both test procedures, the DC current dropped to approximately -4mA and then increased to approximately 0mA after the temperature step change was applied to the environmental chamber.

9 Discussion on Techniques Proposed to Minimise DC Current Injection

Due to time constraints and the specific scope of the project, no attempts were made to try and identify the current control method implemented in any of the IUT or to try and determine if there had been any attempt made to calibrate the current measurement device in regard to offset drift caused by a change in the temperature. Despite this, a review of past literature illustrated that there are designs which propose that they are capable of calibrating the Hall Effect sensor and therefore capable of largely removing the temperature dependency of DC current injection. Such methods include the previously mentioned self calibrating current sensing devices presented in [6] which outlines a control strategy which implements a DC link Hall Effect sensor to calibrate the Hall Effect sensor at the output. As the current flowing from the DC input and therefore the DC link sensor is known to be zero during all free wheeling states, the offset of the sensor measuring the output current can be constantly updated and therefore calibrated. While this precise technique has clear associated issues such as introducing an additional Hall Effect sensor which will increase losses and assuming that two different Hall Effect sensor units will have the exact same response to temperature drift, it does indicate that methods have been developed to overcome the issue of DC current being temperature dependent.

10 Recommendations and Future Work

While the test circuit setup and procedure was primarily proposed to verify a dependent relationship between DC current injection levels and internal inverter temperature, this was hoped to result in proposed amendments to AS4777.2. Before it can be recommended that the test circuit setup and procedure is suitable to be used to propose amendments, there are several areas that need to be looked into.

Firstly, two out of the three inverters tested resulted in non-repeatable DC current injection levels. As previously mentioned, both of the inverters which resulted in non-repeatable magnitude of the variation of DC current levels saw all values increase during the second test procedure. It should be noted that none of the IUT were operated in between testing procedures. While it is outside the scope of this report to investigate the cause of this non repeatability in DC current levels, it appears that it could be a result of some residual offset remaining from the previous measurements. A possible cause of this offset could be remaining residual magnetisation of the Hall Effect sensor. As Hall Effect sensors are electro-magnetic devices, if the magnetic flux did not decrease to zero after the first test procedure, all measurements taken there after may have a non-temperature dependent offset. This requires further investigation before it can be confirmed that one test of the proposed procedure is adequate to determine whether or not an inverter is in compliance. Without further investigation or identifying the cause of the non temperature dependent offset, it would have to be recommended that the test procedure be carried out twice for each IUT. This is because it may be possible for an inverter which may produce DC current levels in accordance with AS4777.2 during the first test but may produce DC current levels above the acceptable level during the second test procedure.

Secondly, AS4777.2 outlines that GCTSPPVI must be tested in regards to the power output of the inverter.

> '*If the inverter does not incorporate a mains frequency isolating transformer, it shall be type tested to ensure the d.c. output current at the a.c. terminals of the inverter is below the above limits at all power levels'.*

As all testing procedures being discussed in this report were carried out with all IUT operating at their rated outputs, this was not investigated in this report. Whether this requirement of test DC current injection at different power levels is necessary given the internal inverter temperature is changed by altering the ambient temperature requires further investigation. It should be noted however that this would seem unlikely given the only believed effect of adjusting the inverter power level is changing the current flow through the device and therefore influencing the internal inverter temperature.

Pending on further investigation demonstrating there is no need to test the IUT at different power levels; it is the recommendation of this report that the proposed test circuit setup is appropriate for testing whether inverters comply with AS4777.2 regarding tolerable DC current injection levels. This recommendation is broken down as follows:

- Test circuit setup as previously described
- Testing procedure as previously described testing each inverter for a two hour period
- Number of tests per inverter will depend on findings from further investigation

A further possibility for future research could be to reverse engineer a selection of GCTSPPVI inverters which had varying DC current injection trends. The purpose of this would be to determine which control scheme results in which DC current injection trend. It would also help to determine whether or not inverter manufacturers are utilising methods similar to those previously mentioned to compensate for the temperature dependency of current measurement devices such as Hall Effect sensors.

PART B: PV Array Voltage Fluctuation

11 Introduction: PV Array Voltage Fluctuation

As previously mentioned, GCTSPPVI have no galvanic isolation between the AC grid connection point and DC sections of the inverter. Aside from this being potentially hazardous in the case of fault [1], it also means the DC input of the inverter (PV array) is directly connected to the AC output and grid. The implication of this is that depending on the implemented topology, switching scheme and output filter configuration, the PV array voltage can potentially be influenced by the AC output and can therefore fluctuate in one way or another. If the voltage at the DC terminals of the PV array instantaneously jumps from one potential to another, this is potentially hazardous as an induced capacitive current can occur which could be of a large enough magnitude to interfere with equipment or cause a reflex in a person [11]. An instantaneous change in the PV array voltage is due to a non DC (zero) instantaneous common mode voltage which can be described as the average voltage of the two points where the inductor and the grid are respectively connected with respect to earth [12]. This is presented in Equation 1.

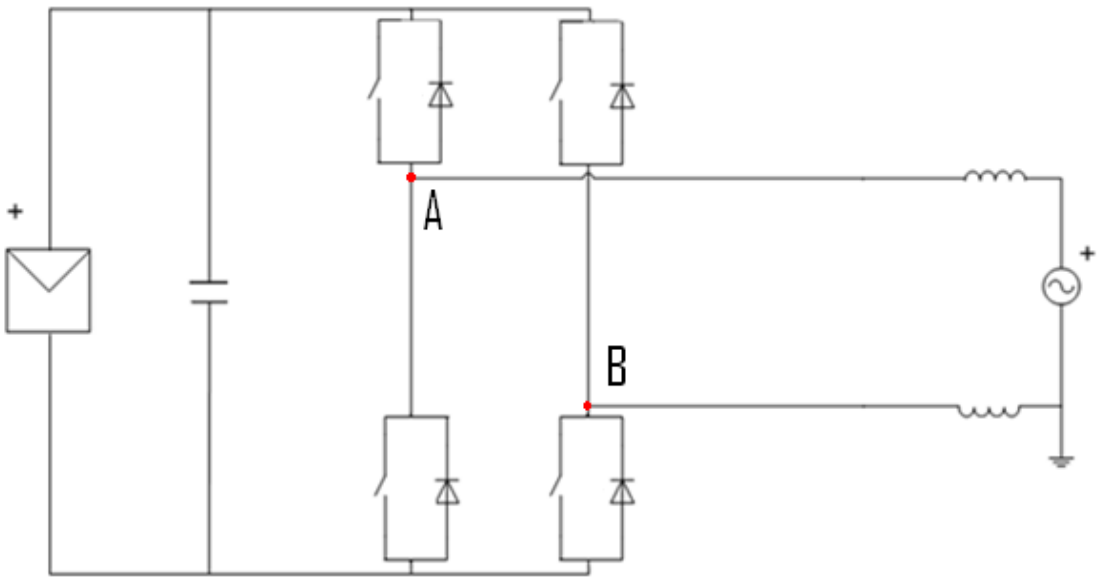

Figure 13: Labelled Junction Voltages of a Fullbridge Topology

$$V_{common\ \ mode} = \frac{V_{A-earth} + V_{B-earth}}{2}$$

Equation 1: Common mode Voltage

Aside from the potential safety issues mentioned regarding capacitive leakage currents, PV array voltage fluctuation can cause another issue in regards to EMC [3].A large voltage fluctuation will induce electromagnetic disturbances which could interfere with the operation of other equipment. As Equation 2 demonstrates, the magnitude of the leakage current is not only proportional to the PV array voltage fluctuation but also the PV array and frame capacitance with respect to earth[1], [3], [2].

$$i_{leakage}\ (t) \propto f(C_{array} . \frac{dV_{DC-earth}(t)}{dt})$$

Equation 2: Capacitive Leakage Current

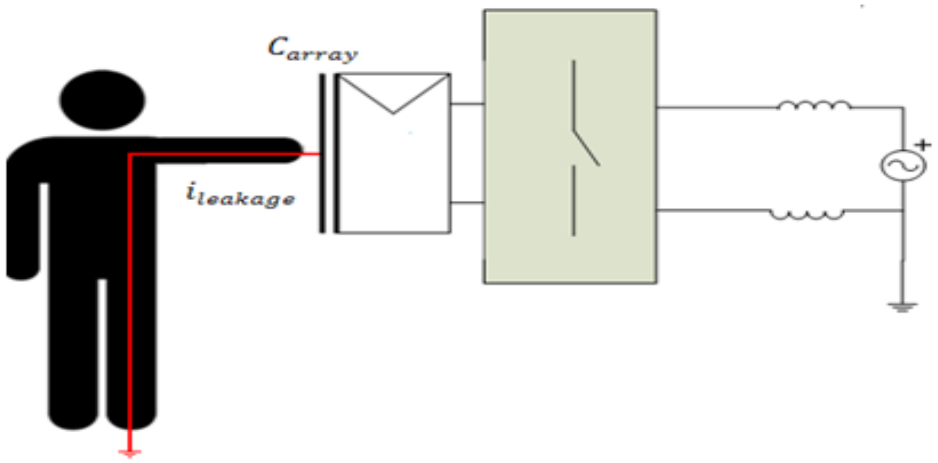

Figure 14: Capacitive Leakage Current Travelling through a Person

The capacitance of the array and frame is dependent on several factors including PV array and frame construction, distance between conductors and environmental conditions [13], [14].Whether a system's frame is earthed or not will also have a large

impact on the leakage current. In a system with an earthed frame, only small leakage current as a result of the small capacitances between PV cells and either the front glass panel or back plate are potential hazards to whoever comes in contact with the PV array or frame. This is because the vast majority of the large capacitive leakage current caused by the capacitance of the frame will flow through the frame if it is earthed. The smaller currents in a system with an earthed frame have been tested and found to be below the human perception threshold [1]. The issue with earthing the entire frame of a large array is that connections are susceptible to corrosion or to be disconnected due to environmental conditions so it cannot be ensured that the entire array will always remain earthed. In terms of environmental conditions, if there is large amount of moisture on the array and frame various internal capacitances between each cell and the frame will be combined resulting in a larger leakage current [13], [14].

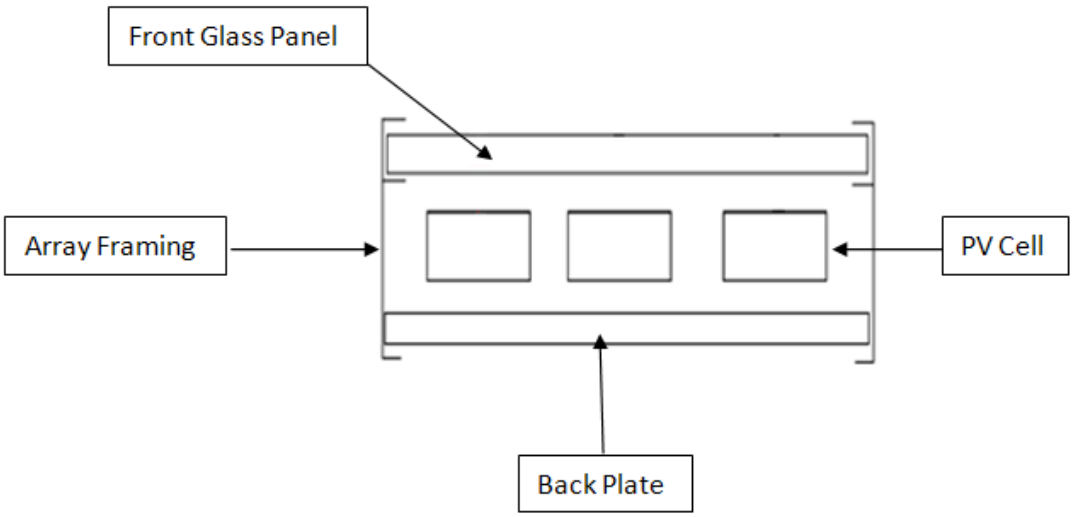

Figure 15: Cross Section Model of Typical PV Array and Framing

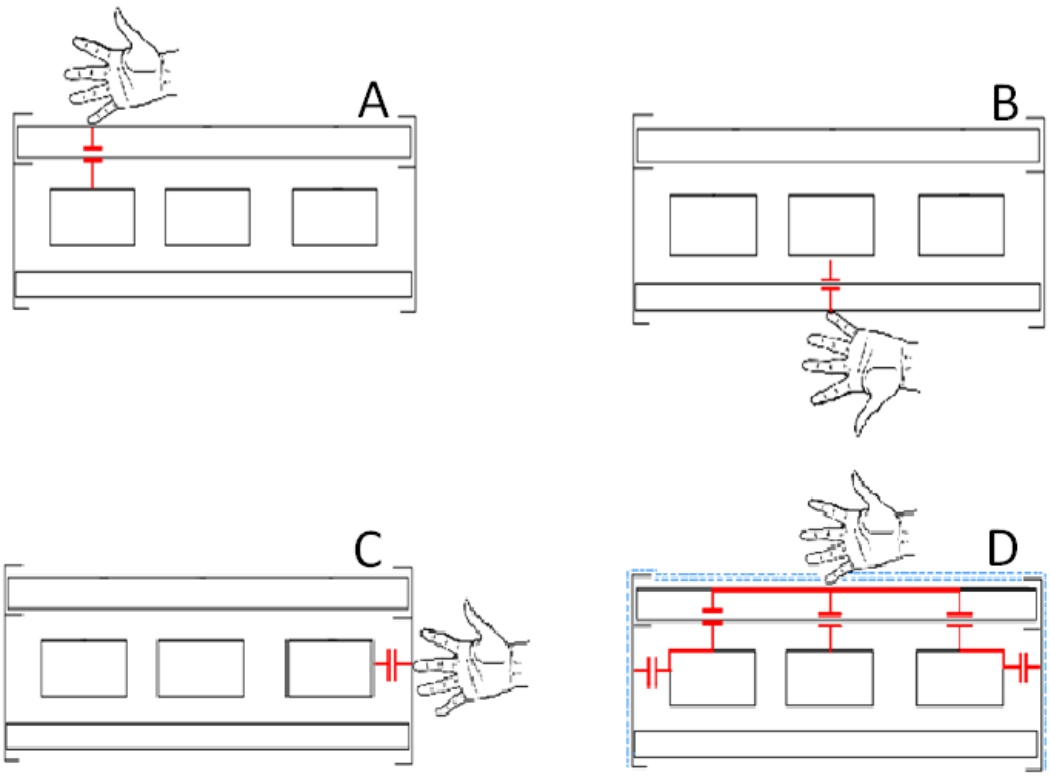

Figure 16: **A-**Capacitance between Cells and Front Glass Panel, **B-** Capacitance between Cells and Back Plate, **C-**Capacitance between Cells and PV Frame, **D-**Combined Capacitance between all Cells and Front Glass Panel in Addition to Capacitance between Cells and Frame when Array is exposed to Moisture

The purpose of Section B of this report is to investigate PV array voltage fluctuation in regards to various GCTSPPVI topologies, switching schemes and output filter configuration. As numbers of installed GCTSPPVI are expected to steadily increase in Australia and internationally, it is important to gain a better understanding of which topologies and switching schemes are suitable for PV applications. This was achieved through the analysis of experimental testing of several GCTSPPVI with different topologies and simulations of different GCTSPPVI topologies, switching schemes and output filter configurations. Findings from Section B of this report will also be used to provide future Murdoch University students with a better understanding of the operation of various GCTSPPVI.

11.1 Literature Review

Several past works of literature present the operation and switching schemes of certain GCTSPPVI topologies and switching schemes. B. Bletterie, [3] Presents several switching schemes and various output filter configurations for a simple full bridge GCTSPPVI topology but does not go into any depth regarding PV array voltage fluctuation at the DC input (PV array). J. M. A. Myrzik and M. Calais, [15] Identifies several different transformerless topologies, discusses what switching scheme they implement and the resulting voltage fluctuation trend. These voltage fluctuations however have not been verified with either simulations or experimental test results.

There are a number of past sources which define the operation of GCTSPPVI implementing a HERIC topology. Sources [16], [12] and [17] all present simulations of HERIC topologies. In all of these past references, a DC or zero instantaneous common mode voltage is discussed. It is then concluded that capacitive current leakages will therefore be zero or very small due to the DC common mode voltage.

"*The inverter generates no common-mode the converter therefore the leakage current through the parasitic capacitance of the PV would be very small*, …" [16].

"To avoid these leakage currents, it is necessary to use inverter topologies that avoid common-mode voltages".[12]

An issue in certain past references is that terms are not clearly defined. As previously mentioned, [16] and [17] both discuss common mode voltage however the term is not clearly defined in either of them. As a result, the difference between PV array voltage fluctuation and common mode voltage is not clearly illustrated and is sometimes interchanged. For example, [17] states the following:

"There is not a fluctuating potential on the DC side, this means that the DC voltage remains constant through all grid period. This way the leakage current through the parasitic capacitance would be very small".

This statement comes into conflict with the HERIC patent *[18]which states:*

"…Leads to a voltage at the solar generator terminals fluctuating with a low-frequency of 50 Hz at half the grid amplitude".

There are further conflicts in past references. [2] Presents experimental test results from a GCTSPPVI implementing a H5 topology with a sinusoidal PV array voltage with [17] claiming "*no fluctuating potential on the DC side".*

These contrasting statements on PV array voltage fluctuation for certain topologies displayed a requirement for a more detailed analysis on various GCTSPPVI topologies, switching schemes and output filter configurations which had not been adequately addressed in past literature. Further more descriptions on the operation of various GCTSPPVI topologies had not been verified by both simulations and experimental testing of. Finally, no references had been found which concisely illustrates how GCTSPPVI implementing various topologies, switching schemes and output filter configurations can be modelled and simulated.

12 GCTSPPVI Topologies

In both the current international and Australian market, a wide range of GCTSPPVI topologies are available for purchase. This report will introduce and demonstrate the operation of four different GCTSPPVI topologies and two different switching schemes which are the most common. The different topologies that will be discussed are:

- Fullbridge Converter Topology
- Halfbridge Converter Topology
- H5 Topology
- Highly Efficient Reliable Inverter Concept (HERIC) Topology

Simplified circuit diagrams of each topology are given below.

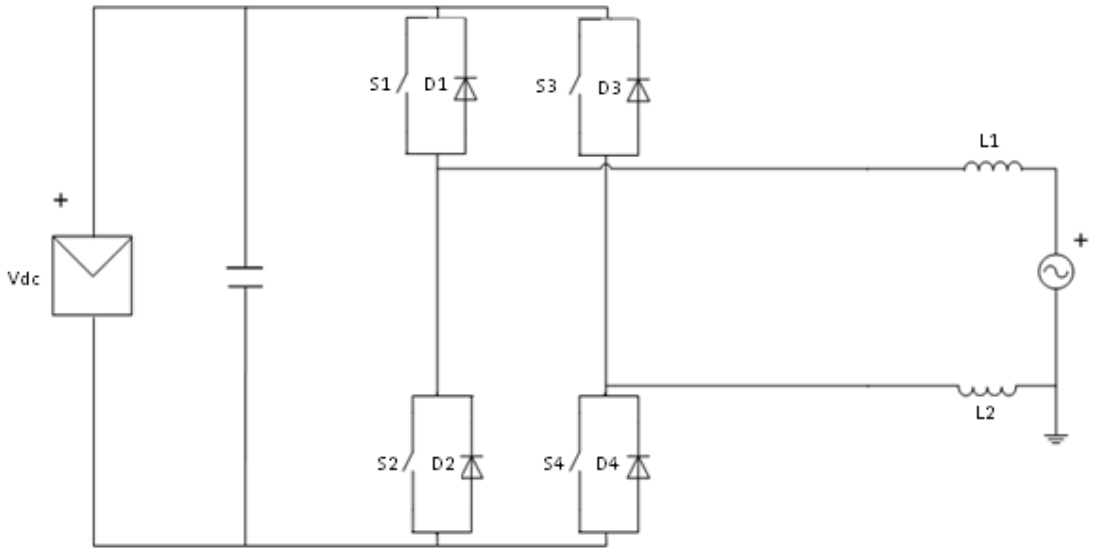

Figure 17: Full Bridge Converter Topology

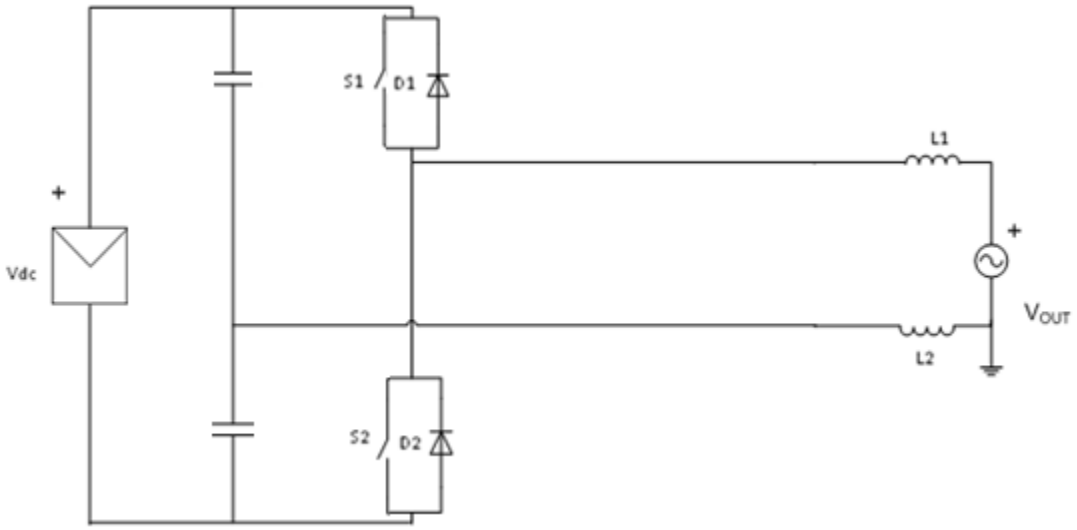

Figure 18: Halfbridge Converter Topology

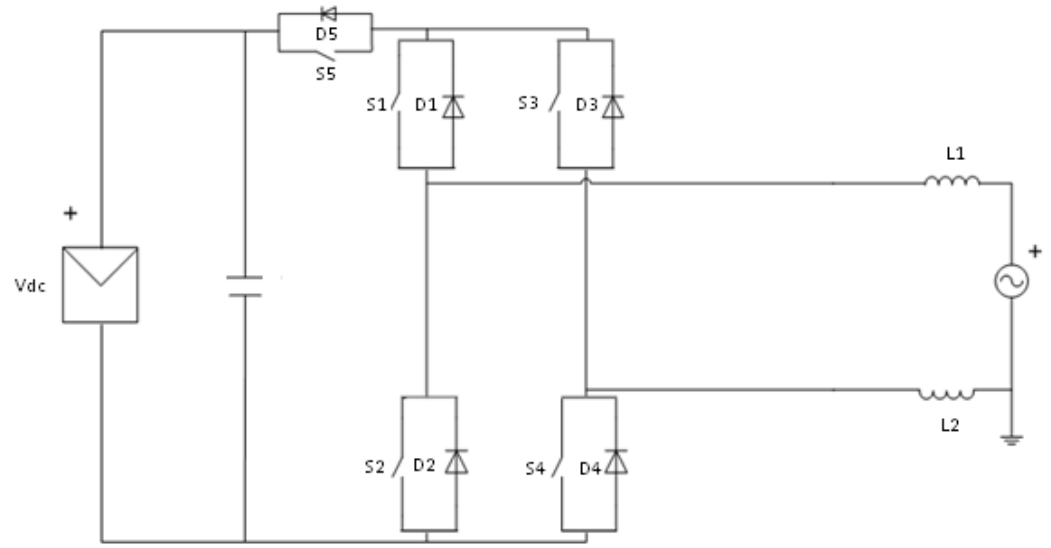

Figure 19:H5 Topology

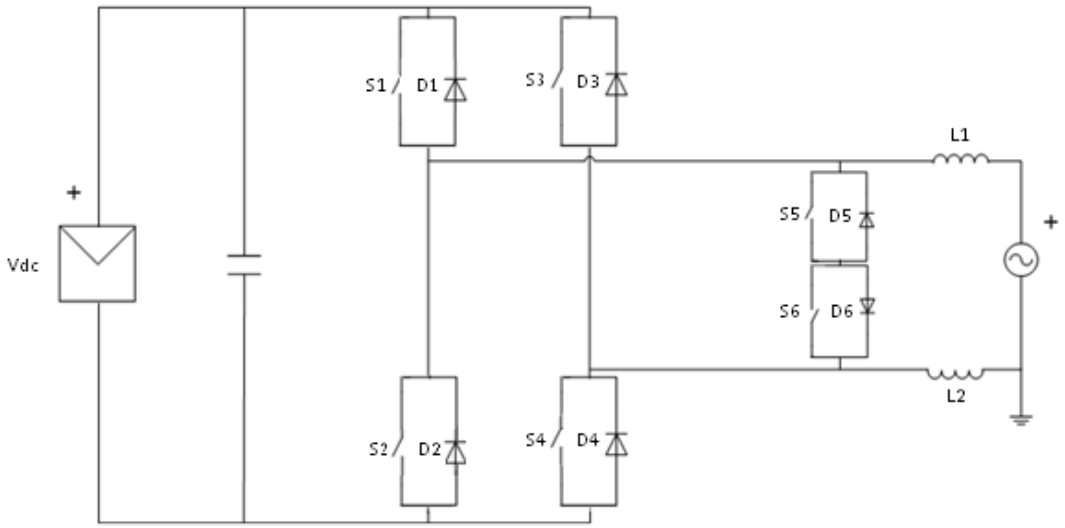

Figure 20: HERIC topology

12.1 Full Bridge topology

In the past, the most common inverter design had utilised the full bridge topology. Both the H5 and HERIC topology consist of the fundamental full bridge topology but with incorporated additional switches during which the free-wheeling period. As can be seen in Figure 17, the full bridge or H-bridge as it is sometimes known consists of two parallel strings of two switching power devices in series with anti-paralleled diodes. The full bridge converter can be used to generate two different PWM pulse trains depending on the switching scheme implemented. The two schemes are called bipolar and unipolar switching.

12.2 Bipolar Switching Scheme

A full bridge converter which uses a bipolar switching scheme is called a two level converter. With a bipolar switching scheme, the full bridge converter only has two switching states as the junction voltage (V_j) switches from $+V_{DC}$ to $-V_{DC}$ using PWM. When used as a two level converter, the full bridge converter uses the switching scheme outlined in Table 4. The resulting pulsed output is displayed in Figure 21. Additionally, Figure 22 displays the carrying current paths at each switching state.

Switching State	Switches on	Switches off	Pulsed Output Voltage (V_j)
1	S1, S4	S2, S3	$+V_{DC}$
2	S2, S3	S1, S4	$-V_{DC}$

Table 4: Switching States for Bipolar Switching Scheme for a Fullbridge Converter

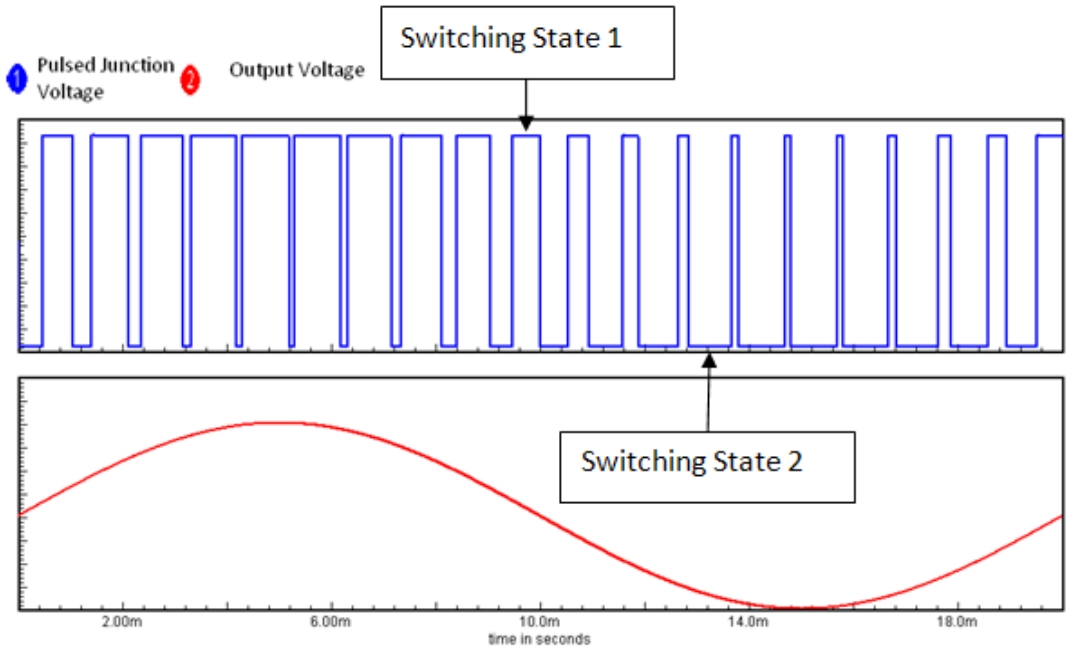

Figure 21: Bipolar (Two Level) Switching Scheme

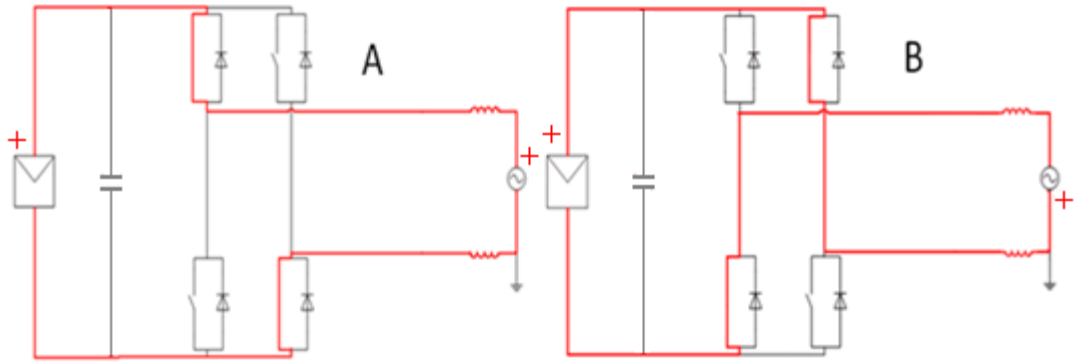

Figure 22: **A**-Current Path for Fullbridge Converter implementing Bipolar Switching Scheme during Switching State 1, **B**-Current Path for Fullbridge Converter implementing Bipolar Switching Scheme during Switching State 2

12.3 Unipolar Switching Scheme

A full bridge converter which uses unipolar switching is called a three level converter. A unipolar switching scheme is where the output of the converter (V_j) switches between $+V_{DC}$and zero during the positive halfwave and between $-V_{DC}$ and zero during the negative halfwave. Unlike bipolar switching, unipolar switching requires at least three different switching states as the junction voltage (V_j) can be either $+V_{DC}$, $-V_{DC}$ or zero although most inverters implement four switching states by having a different switching combination to create the zero junction voltage for each halfwave. This to evenly distribute the use of switches making heating symmetrical and thereby reducing losses.

Both the H5 and HERIC topology operate as three level converters all be it by implementing different switching schemes. One of the main associated advantages of implementing a unipolar switching scheme as opposed to a bipolar scheme is that the switching losses are significantly reduced because the associated voltage drop from switching from one state to another is halved. One of the downsides of implementing a unipolar switching scheme however is that there are higher associated harmonic content in the output current around the zero crossing (particularly at lower power levels) [9].

A number of different unipolar switching schemes exist for fullbridge topologies with associated advantages and disadvantages regarding PV array voltage, switching losses and complexity of control signal generation. The three unipolar switching schemes implemented by fullbridge topologies that will be discussed in this report are the standard method outlined in [19]and one phase chopping (type A and B). The three switching schemes and associated switching states and orders are presented in Table 5, Table 6 and Table 7.

Switching State	Switches on	Switches off	Junction Voltage	Halfwave
1	S1, S4	S2, S3	$+V_{DC}$	Positive
2	S1,S3	S2,S4	0	Positive
3	S1, S4	S2,S3	$-V_{DC}$	Positive
4	S2, S4	S1, S3	0	Positive
5	S2,S3	S1,S4	$+V_{DC}$	Negative
6	S1,S3	S2,S4	0	Negative
7	S2,S3	S1,S4	$-V_{DC}$	Negative
8	S2,S4	S1,S3	0	Negative

Table 5: Switching States for Standard Unipolar Switching Scheme for a Full bridge Converter [19]

Switching State	Switches on	Switches off	Junction Voltage
1	S1, S4	S2, S3	$+V_{DC}$
2	S2,S4	S1,S3	0
3	S2, S3	S1, S4	$-V_{DC}$
4	S2, S4	S1, S3	0

Table 6: Switching States for One Phase Chopping Unipolar Switching Scheme (Type A) for a Full bridge Converter [15]

Switching State	Switches on	Switches off	Junction Voltage
1	S1, S4	S2, S3	$+V_{DC}$
2	S2, S4	S1, S3	0
3	S2, S3	S1, S4	$-V_{DC}$
4	S3,S1	S2,S4	0

Table 7: Switching States for One Phase Chopping Unipolar Switching Scheme for a Full bridge Converter(Type B) [9]

The main difference between the three presented unipolar switching schemes is the implementation of different free-wheeling states during each halfwave. While both one phase chopping methods operate similarly with the only difference being that type B implements a different switching state for the free-wheeling state of each halfwave, the standard method is subtly different because both free wheeling states occur in the same halfwave. The resulting pulsed output of the one phase chopping scheme (type B) is displayed in Figure 23. The associated current paths are displayed Figure 24.

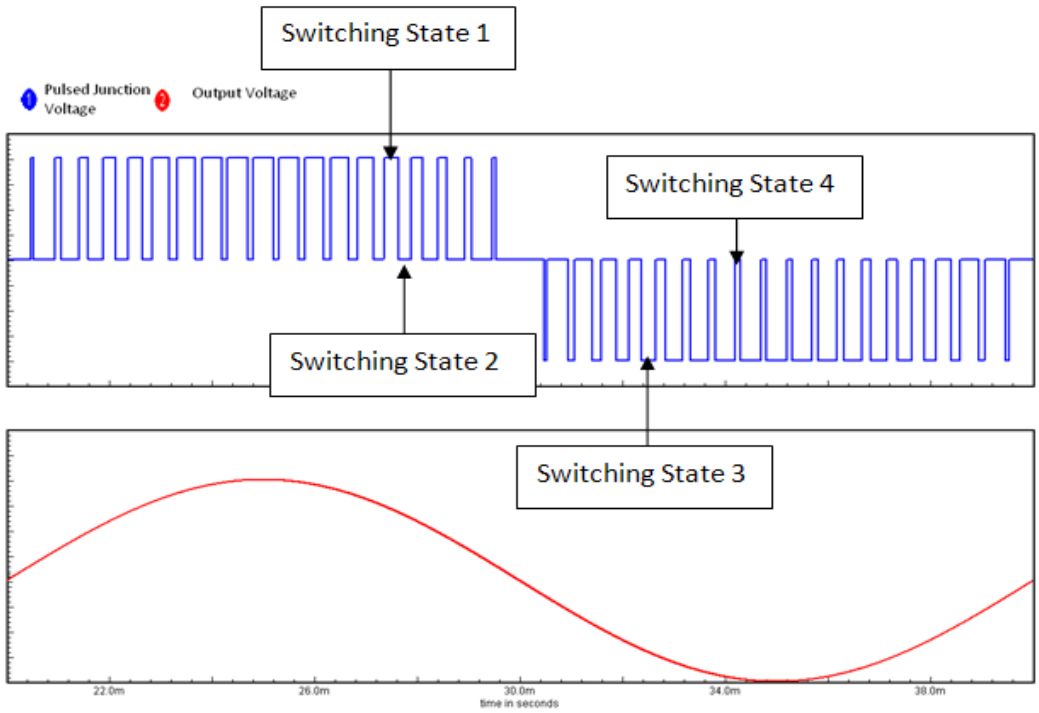

Figure 23: Unipolar (Three Level) Switching Scheme

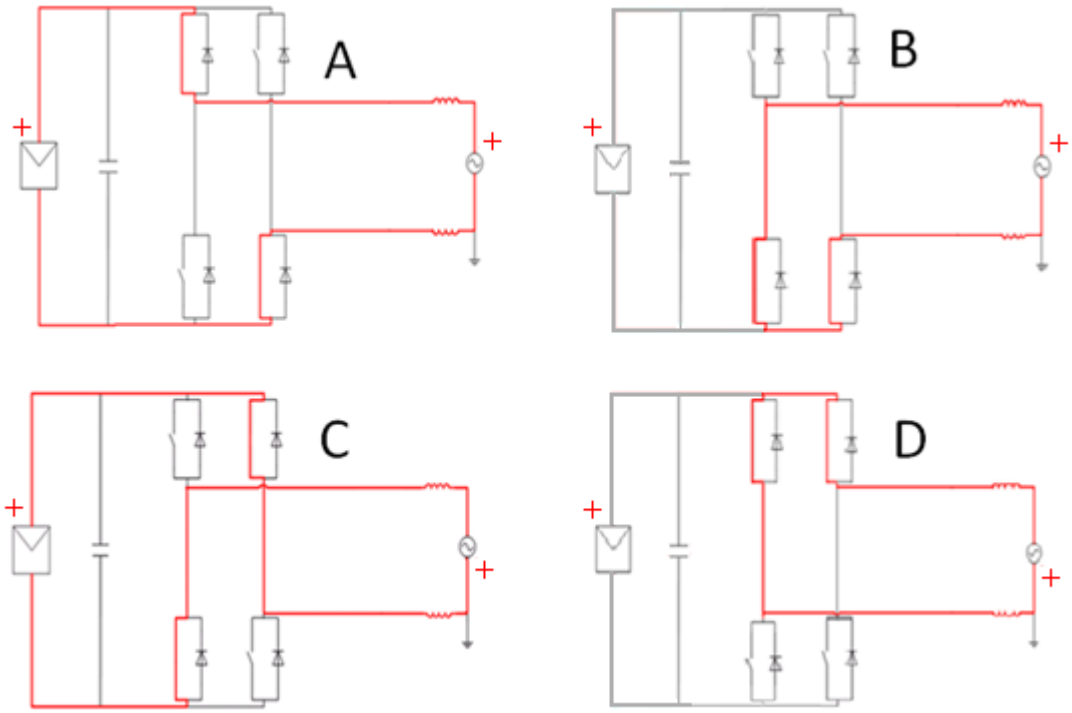

Figure 24: **A-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 1, **B-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 2, **C-**Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 3 **D-** Current Path for Full bridge Converter implementing Unipolar Switching Scheme during Switching State 4

12.4 Half Bridge Topology

The full bridge has been the inverter topology design of choice in the past over a half bridge design which consists of only one string of two switching devices and parallel diodes in series for several reasons. Firstly, with only two switches in series, the halfbridge converter is only capable of transmitting a pulse train to the output with a magnitude of half that of the full bridge ($+\frac{1}{2}V_{DC}$ to$-\frac{1}{2}V_{DC}$). This means that for the same DC input voltage a half bridge converter may require a front end boost converter to step up the input voltage of the inverter. Introducing a new stage of the inverter will introduce charging and power devices which will result in additional losses and an overall lower efficiency. As a higher DC input to the halfbridge converter is required, it also means implemented switching device with a higher voltage rating. Such switching devices typically have higher losses and must be switched at a slower rate which may result in an

increase in harmonic content of the output. It is also worth noting that the topology is only capable of implementing bipolar switching as the design consists of two switches making a free wheeling period impossible.

Another associated advantage of utilising a halfbridge topology is that the design naturally prevents DC current injection into the AC network [6]. As a halfbridge converter implements a split input capacitance, one capacitor is always present in the current conducting path.

Switching State	Switches on	Switches off	Output voltage
1	S1	S2	$+V_{DC}$
2	S2	S1	$-V_{DC}$

Table 8: Switching States of Bipolar Switching Scheme for Halfbridge Converter

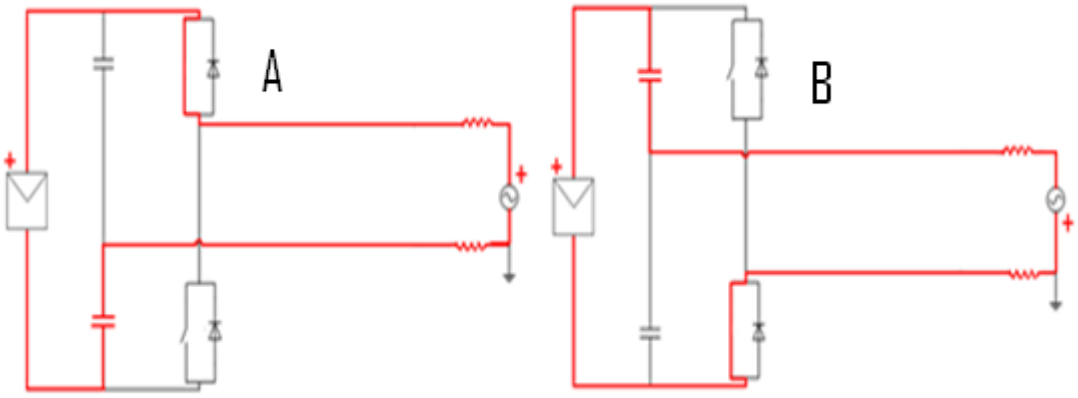

Figure 25:**A-** Current Path for Half Bridge Converter during Switching State 1, **B-**Current Path for Half Bridge Converter during Switching State 2

12.5 H5 Topology

The H5 topology is a patented design from the leading German inverter manufacturers SMA. The design which is now being used in most of SMA's new inverter designs has

the highest measured efficiency of 98 percent due to its switching configuration and free wheeling period. As Figure 2 demonstrates, the H5 topology consists of a fullbridge converter with an additional switch paralleled with a diode between the DC input and fullbridge. As previously mentioned, the H5 topology implements a unipolar switching scheme. The various switching states are given below inTable 9. The current paths generated by each switching state of the H5 topology are also illustrated in Figure 26

Switching State	Switches on	Switches off	Output voltage
1	S1, S4, S5	S2, S3	$+V_{DC}$
2	S1	S2, S3, S4, S5	0
3	S2, S3, S5	S1, S4	$-V_{DC}$
4	S3,	S1, S2, S4, S5	0

Table 9: Switching States for Unipolar Switching Scheme for Inverter with a H5 Topology

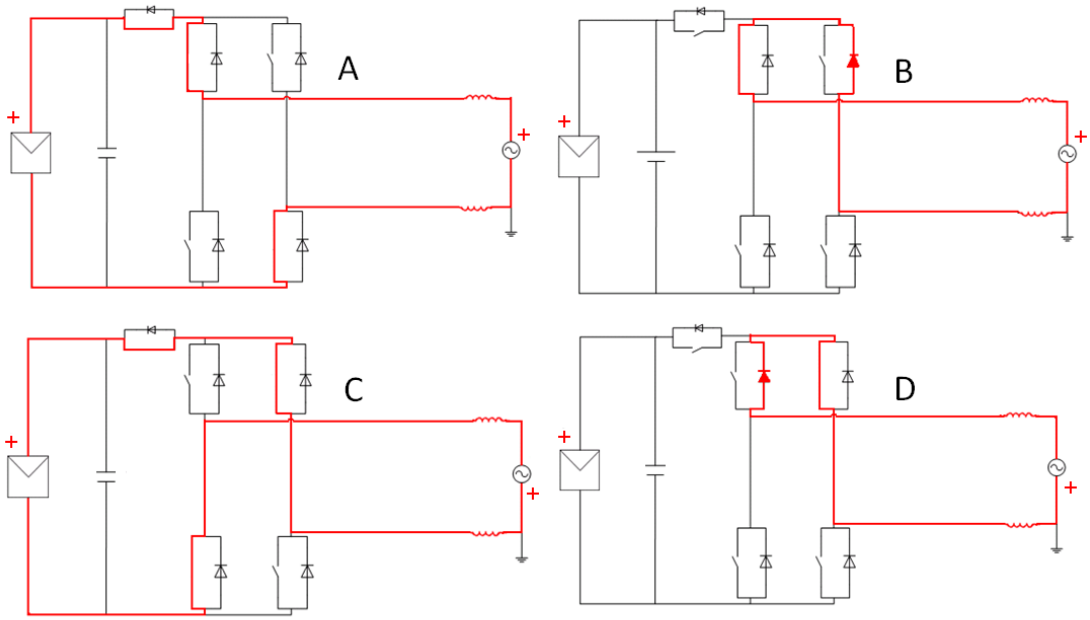

Figure 26: **A-**Current Path for H5 Topology during Switching State 1, **B-**Current Path for H5 Topology during Switching State 2, **C-** Current Path for H5 Topology during Switching State 3, **D-** Current Path for H5 Topology during Switching State 4

12.6 HERIC Topology

The HERIC topology is also becoming increasingly more popular because of its higher efficiencies and is used in most of the German manufacturers Sunways new inverter designs. As Figure 20demonstrates, similarly to the H5 design, it consists of a fullbridge converter but has two additional switches anti-paralleled with diodes in series between the output and the fullbridge converter. The HERIC topology also implements a unipolar switching scheme. The various switching states are given below in Table 10. The current paths generated by each switching state of the HERIC topology are also illustrated in Figure 27.

Switching State	Switches on	Switches off	Output voltage
1	S1, S4, S6	S2, S3, S5	$+V_{DC}$
2	S6	S1, S2, S3, S4, S5	0
3	S2, S3, S5	S1, S4, S6	$-V_{DC}$
4	S5	S1, S2, S3 S4, S6	0

Table 10: Switching States for Unipolar Switching Scheme for Inverter with a HERIC Topology

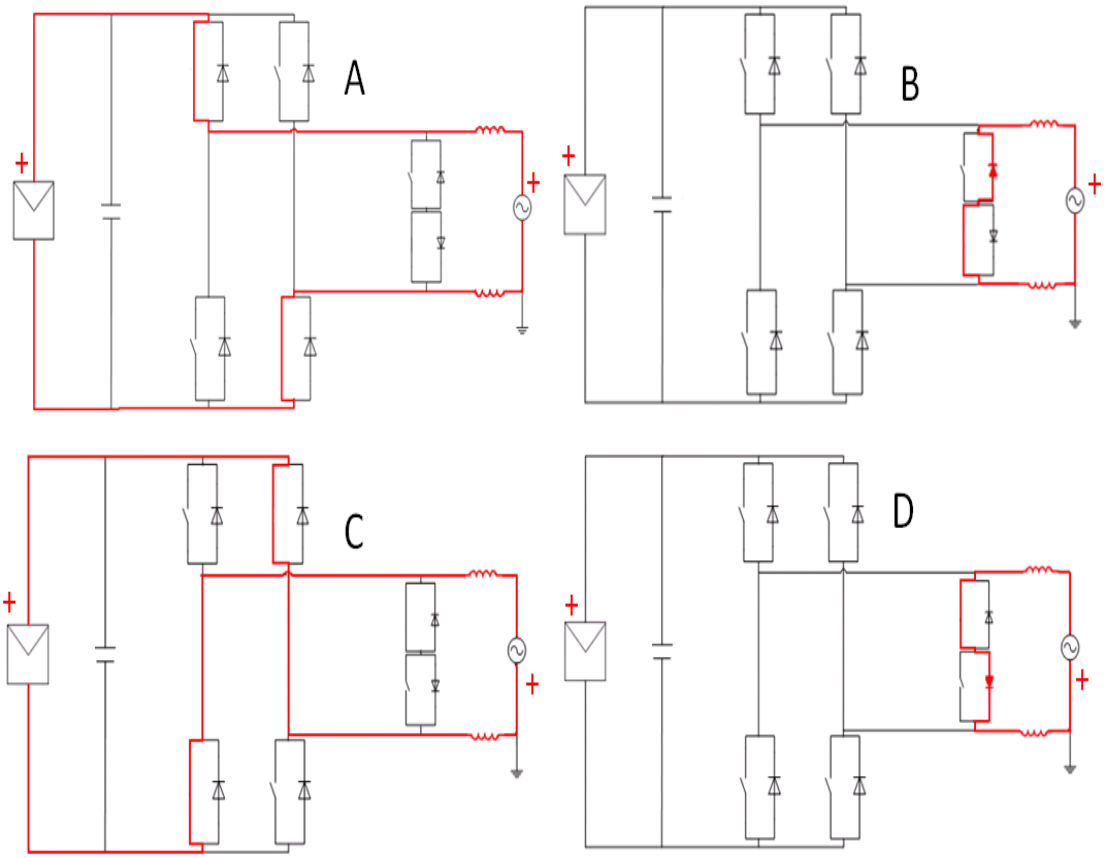

Figure 27: Current Path for HERIC Topology during Switching State 1

13 Modes of Operation for GCTSPPVI

As previously stated while up to four unique switching states can be implemented, a typical GCTSPPVI can be characterised by two modes of operation. The first mode of operation is when the output current increases as the inductor of the output filter is charged up. During this mode, the DC input (PV array) is always connected to the grid through the fullbridge (or halfbridge) allowing an increase in the output current in the same direction as the increase of the grid current. During this time the PV array input is effectively used to charge up the split filter output inductors. The second mode of operation is when the output current decreases relative to the direction of the grid current as the output filter inductors are discharged until the first mode of operation recommences. The duration of operating at one mode before switching to the other is pulse width modulated at a high frequency with the duration of each mode being the difference between the total period and the length of time on the previous mode of the other.

The first mode of operation is achieved in the same manner for both unipolar and bipolar switching schemes for topologies incorporating a fullbridge which is closing S1 and S4 during the positive halfwave and closing S2 and S3 during he negative halfwave. The pulsed output (V_j) will be $+V_{DC}$ during this mode of operation. In the case of a halfwave topology this would be achieved by closing S1 in the positive halfwave and S2 in the negative. The second mode of operation however can be achieved in a number ways and is dependent on both the topology and implemented switching scheme of the GCTSPPVI. In the case where a bipolar switching scheme is implemented, the discharging of the output filter inductors is achieved by switching to the opposite switching configuration (closing S2 and S3 during the positive halfwave or S1 and S4 during the negative halfwave). The pulsed output (V_j) would be $-V_{DC}$ during this mode of operation for a GCTSPPVI implementing a bipolar switching scheme. In the case where a unipolar switching scheme is implemented, this is achieved by a free-wheeling state whereby no current flows from the DC input to the switching stage of the inverter. In this instance, the output filter inductors act as a source and begin to

discharge. This free wheeling can be produced from either closing S1 and S3 or S2 and S4. The pulsed output (V_j) would be zero during this mode of operation for a GCTSPPVI implementing a unipolar switching scheme.

The following figures are used as an example illustrate the associated current and voltage waveforms of the different modes of operation for a GCTSPPVI implementing a unipolar switching scheme over a short period of time. Figure 28 illustrates the selected point of operation at half of the maximum output voltage magnitude$\left(\frac{\sqrt{2}\times 240}{2}\right) = 169.71V$. At this selected point of operation, the duration time of mode one and two are the same as shown in Figure 29 resulting in the inductor current charging for as long as it discharges as demonstrated in Figure 30.

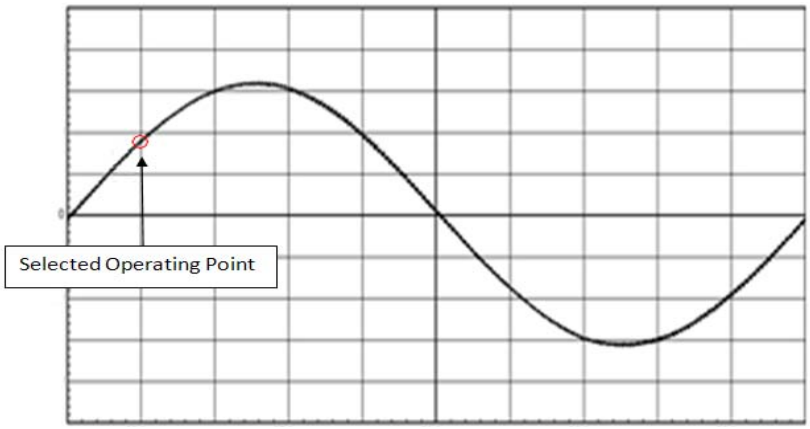

Figure 28: Output Voltage of Fullbridge Utilising Unipolar Switching Scheme with Selected Operation Point of $0.5\times V_{OUT-max}$

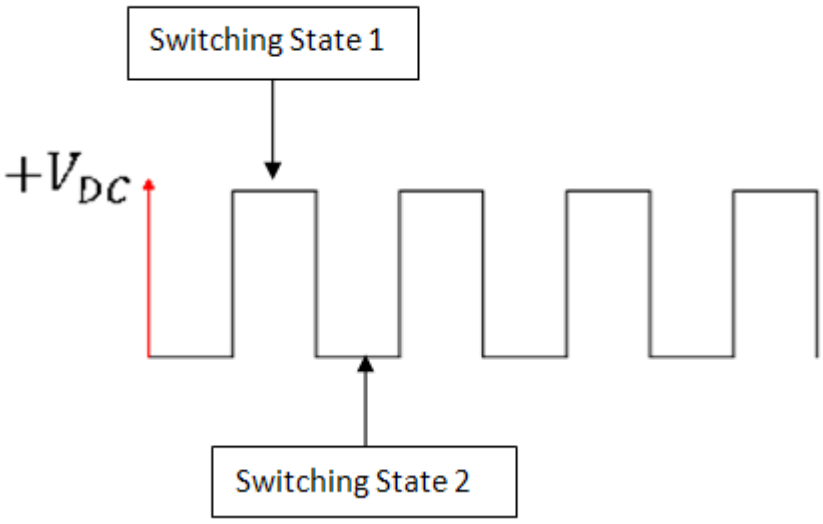

Figure 29: PWM Pulse Output (V_J)at Selected Operating Point

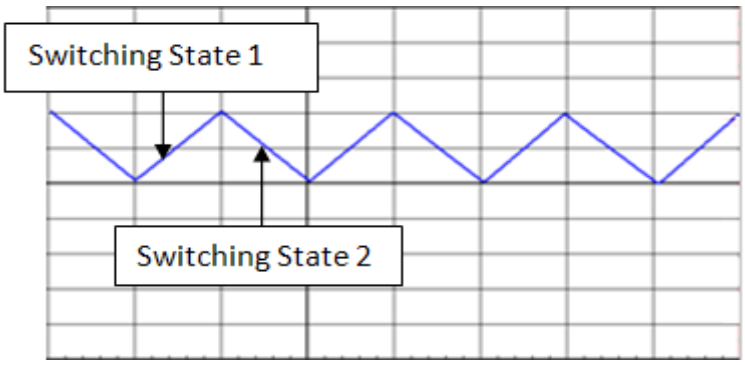

Figure 30: Split Inductor Current (I_L) at Selected Operating Point

The associated current loops for each operation mode at the selected operating point are displayed in Figure 31. As can be seen Equation 3, during operation mode 1 the split filter inductances are being charged (positive voltage drop) and then act as a source and are discharged during the second operation mode (negative voltage drop).

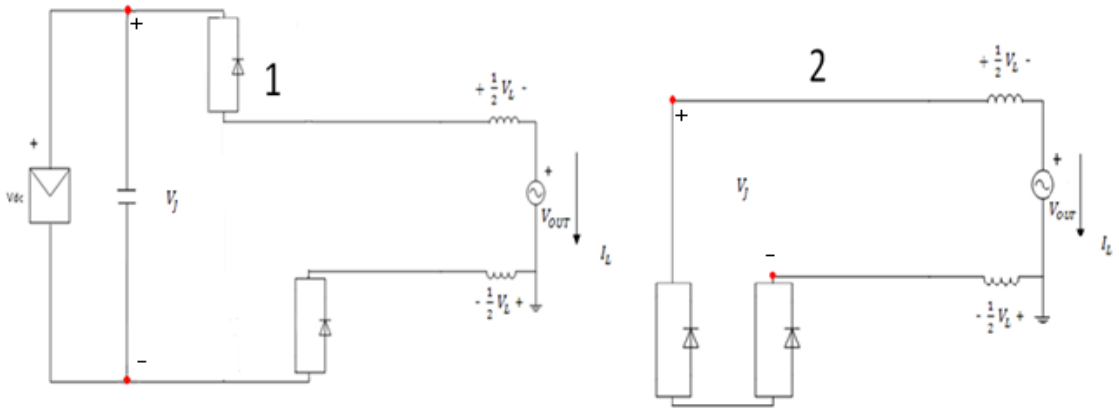

Figure 31: **1**-Current Path of GCTSPPVI implementing One Phase Chopping Unipolar Switching Scheme during Operating Mode 1, **2**-Free Wheeling Current path of GCTSPPVI implementing One Phase Chopping Unipolar Switching Scheme during Operating Mode 2

Operation Mode 1: $V_L = V_{DC} - V_{OUT} = 240 \times \sqrt{2} \times \frac{2.5}{2} - \left(\frac{\sqrt{2}\times 240}{2}\right) V = \mathbf{254.56V}$

Operation Mode 2: $V_L = -V_{OUT} = = -\left(\frac{\sqrt{2}\times 240}{2}\right) V = \mathbf{169.71V}$

Equation 3: Calculation of voltage across Split filter Inductance (V_L) at Selected Operating Point

14 Simulating PV Array Voltage Fluctuation

In order to gain a better understanding of the fluctuation of PV array terminal voltages with respect to ground, several different GCTSPPVI topologies were simulated using circuit simulation software. The focus of these simulations was to determine which topologies and switching schemes are suitable for PV applications and to provide future Murdoch University students with a better understanding of the operation of various GCTSPPVI. The selection of software used was based on appropriateness to the specific task, usability, precision, cost and familiarity of the software package for the possibility of future work and education of future students. Based on these criteria, ICAP (Version 4Windows Educational Standalone) was selected.

The following topologies and switching schemes were simulated:

- Fullbridge converter topology implementing a bipolar switching scheme
- Fullbridge converter topology implementing a one phase chopping unipolar switching scheme (Type B)
- Fullbridge converter topology implementing a classic unipolar switching scheme
- Halfbridge Converter Topology
- H5 Topology
- Highly Efficient Reliable Inverter Concept (HERIC) Topology

The level of detail regarding the simulation was decided to be as detailed as necessary to simulate accurate waveforms of the PV array voltage fluctuations of the positive and negative DC input terminals. It was therefore decided to include all aspects of control regarding correct switching schemes and PWM pulse trains whilst not being concerned with the inverter efficiency and therefore losses. As a result, all ideal elements were used where possible. However as most ICAP components are models of existing components, many non-ideal components had to be implemented which increased the complexity of each circuit simulation.

14.1 Selection of Appropriate Modelling

Regardless of the topology or switching scheme implemented by a given GCTSPPVI, certain operational functions are generic for all GCTSPPVI simulations presented in this report. All simulations of the various GCTSPPVI topologies were modelled under the following assumptions:

- Constant solar radiation
- Supplying to a grid with unity power factor, no THD, voltage flicker or change in frequency of the grid voltage
- No DC current injection

It should be noted that while the assumptions listed above are practically unlikely, they were made in the interest of simplifying the circuit as much as possible without jeopardising the general trend and magnitude of the PV array voltage fluctuation or output PWM pulse trains. In addition, only the switching stage of the various GCTSPPVI topologies was included. Commercially available manufactured inverters are highly sophisticated pieces of equipment. As a result they have many intricate protection sub-circuits used to measure parameters such as the presence and quality of the grid. As will be discusses in more depth in the next chapter, no maximum power point tracker (MPPT) was modelled as the PV array was modelled with an ideal DC voltage source. The simplifications were used as the additional sub-circuits add no additional insight in regards to PV array voltage fluctuations at a fixed power level.

Another simplification resulted in the omission of any boost or buck converters. Many GCTSPPVI implement a front end boost converter before the switching stage. As can be seen in Figure 32, the negative input terminal is at the same potential as the negative output terminal. As a result, omitting this stage will change the magnitude of the array fluctuation but not the fluctuation which is of primary concern.

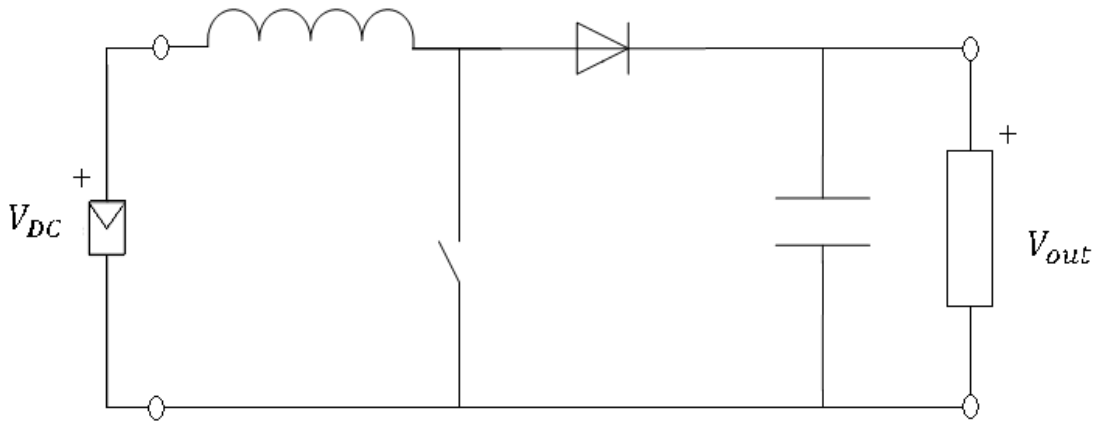

Figure 32: Front End Boost Converter

14.2 Dead Time

Any physically implemented high frequency switching device will implement a concept whereby a small period time elapses where no switches are closed known as dead time. In practice there may be delays and inaccuracies in the control signals determining the state of each switching element or asymmetry in the semiconductor devices used. During the dead time, all switches are opened. The purpose of this dead time is to ensure that there is no overlapping of different states as this would resulting in undesirable operation such as shorting out the DC input. While it was initially hoped dead time could be omitted due to the ideal switches implemented in all simulations, non-ideal logic gates used to create the gate control signal for certain switches introduced non-ideal characteristics. This resulted in the requirement of implementing dead time for all three level converters (fullbridge topology implementing a unipolar switching scheme, H5 and HERIC topologies). An RC filter with a paralleled diode across the resistor was implemented to create dead time. All sizing equations can be found in Appendix A in Table 15.

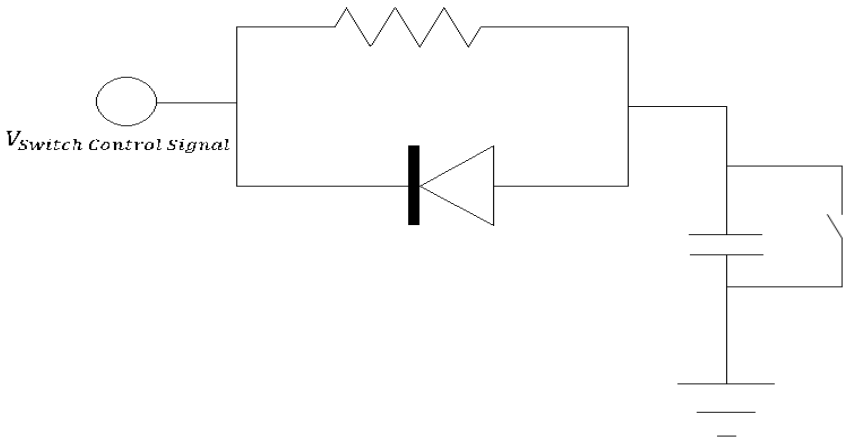

Figure 33: RC Filter used to Implement Dead Time

14.3 Anti-paralleled Diodes

All simulated topologies and switching schemes in this report have all switching devices connected to anti-paralleled diodes. This is typical for most types of converters and is a design requirement for several reasons. While there several different power semiconductors may be used as switches in inverters, the most common are IGBTs or MOSFETS. While MOSFETS are capable of reverse current conduction, IGBTs are not and therefore require anti-paralleled diodes. Anti-paralleled diodes are required to allow a closed current path during dead time. Anti-paralleled diodes were required for H5 and HERIC topology simulations as they require current to flow through certain diodes for nominal operation during free-wheeling states

14.4 Switching States

A fullbridge converter must have two switching devices in a closed state and two in an open state at all times except during dead time. While there are only six possible unique switch combinations whereby two switches remain closed while the other two are open, different combinations will result in different pulsed outputs which can be achieved by implementing a number of different control signals and by changing the order of the different switching states. It is important however to note that some of these switching combinations will result in non desirable operation.

For example, two switches in the same bridge such as S1 and S2 can never be closed at the same time. This would result in short circuit across the DC input.

A requirement of having 2 switches closed at all times during nominal operation is due to the following reasons:

- Reduction of losses
- Phase shift between output waveform and reference waveform

For GCTSPPVI which implement power semiconductors such as MOSFETS which are capable of carrying reverse current, it is desirable to have two switches closed at all times. This is because losses are reduced when the current path is through the MOSFET as opposed to a forward-biased diode.

A minor phase shift could potentially cause issues when the reference current waveform is around the zero crossing. During this time, it is possible for the grid to be in the negative halfwave and the control signals supplied to the switching devices are for the positive halfwave. If only one switch is closed, current will have to flow through a forward biased diode to complete the free wheeling current path. Figure 34 displays such a scenario for a fullbridge converter implementing a unipolar switching scheme whereby the output current and reference signal are marginally out of phase at an operating point near the zero crossing. If only one switch was closed to produce the free wheeling state, only S4 would be closed instead of S2 or S3 (depending on which unipolar switching scheme is implemented). As D2 is reverse-biased, current will not flow through D2 which would cause an open circuit. As this free wheeling current path includes the split filter inductors, the current can not change instantaneously. This is why all switches must be capable of bidirectional current flow.

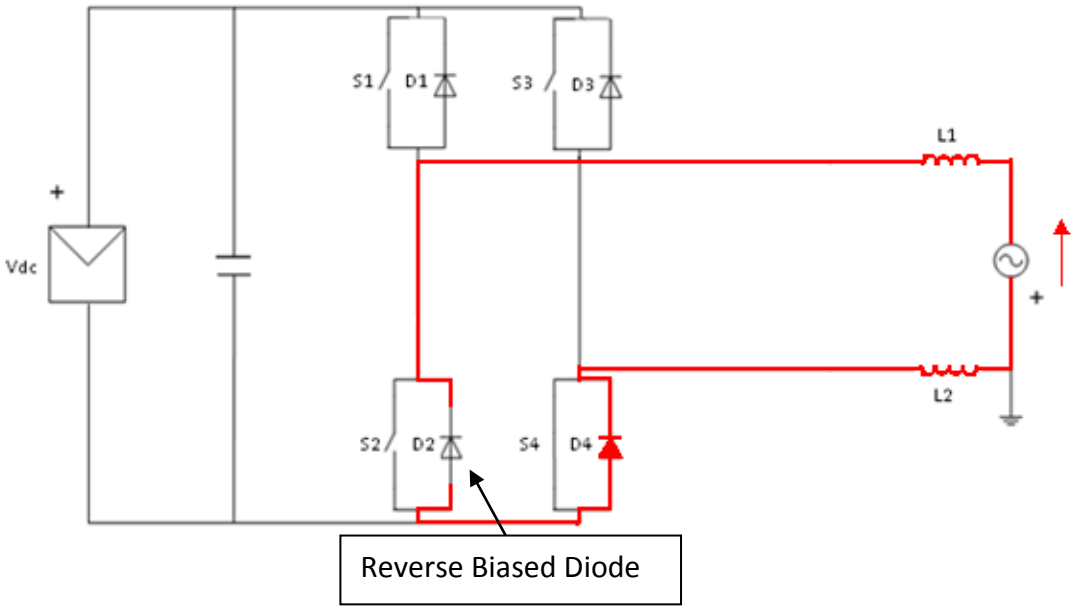

Figure 34: Scenario of Operating with One Closed Switch Resulting in a Fault

14.5 PV Array

As previously mentioned, the PV array (DC input) was modelled for all simulations using an ideal (non current limited) DC voltage source. This was based on the assumption that the PV array was constantly operating at the knee point (maximum power point) of the I-V curve being exposed to a constant solar radiation therefore removing the need for a MPPT. The magnitude of the DC input was sized by the ratio of the sawtooth signal divided by the control signal as outlined in [19]. All sizing calculations can be viewed in Appendix A in Table 15.

As it is outside the scope of this report to simulate and measure capacitive leakage currents, the capacitance of the array was only modelled for the H5 topology. This was due to the fact that during the free-wheeling state where the array is disconnected from the output, the DC input had no reference to ground. The size of the total capacitance was based on measurements under dry conditions from [1].

14.6 Switching Device Selection

As previously mentioned, the most common power semiconductors used as switches for GCTSPPVI are IGBTs or MOSFETS. As modelling real power devices would add no additional insight in regards to PV array voltage fluctuation, ideal voltage controlled switches which close when the gate control signal exceeds a manually entered threshold voltage were implemented. It should be noted that the threshold voltage of the utilised voltage controlled switches in ICAP must be exceeded to change the state of the switch. As the gate control signals supplied to each switch were pulsed between 0 and 5 Volts, the threshold voltage was set to 4.98 Volts.

14.7 Control Signal Generation

All simulated GCTSPPVI discussed in this report implement switches which are either switched at mains frequency or high frequency PWM for either a halfwave or the whole period. In the case of the mains frequency switches, the switch is controlled by a pulsed voltage source which is either high during the positive halfwave and low during the negative halfwave or vice-versa. In the case of a high frequency switch, the fundamental PWM control signal was generated by implementing a "nearly" ideal comparator requiring rails supply voltages of $\mp$15 Volts producing an output of either 0 or 5 Volts.

It is important to note that there is a subtle difference between the inputs of the comparator for bipolar and unipolar switching schemes. As outlined in [19], in order to generate control signals for switches for a GCTSPPVI implementing a bipolar switching scheme, the two inputs of the comparator are:

- Mains frequency (50 Hz) sinusoid
- sawtooth at high frequency (10kHz)

It should be noted that while most GCTSPPVI have a higher switching frequency than 10 kHz (typically in the range of 15 to 20kHz), a slower frequency was selected to decrease the required sampling time of simulations. An example of these two inputs is displayed in Figure 35. It should be noted however that for the purpose of the illustration, the sawtooth frequency was reduced to 1 kHz.

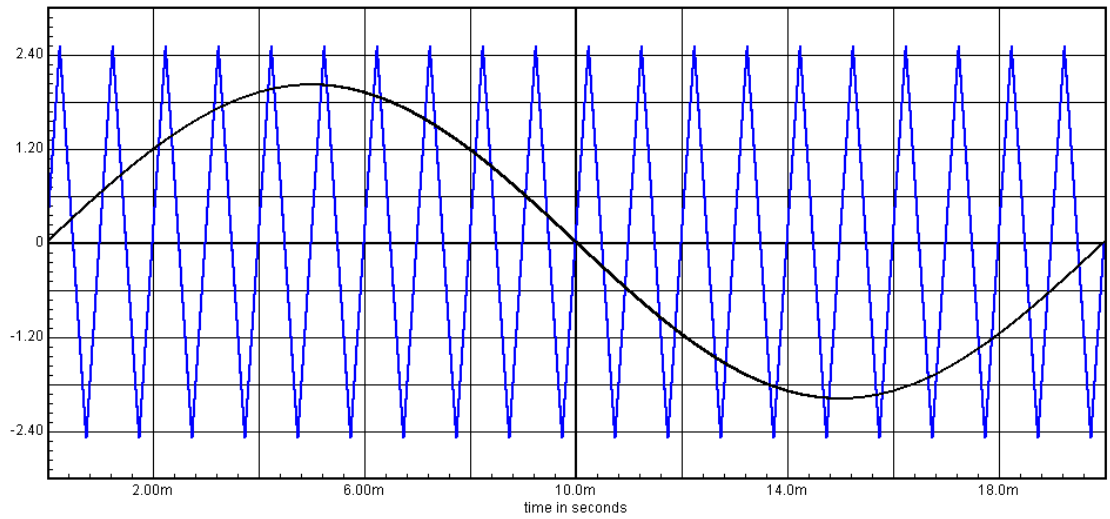

Figure 35: Comparator inputs for generating high frequency PWM control signal for GCTSPPVI

Implementing a Bipolar Switching Scheme

As introduced in [12]the two inputs of the comparator required to generated control signals for switches for a GCTSPPVI implementing a unipolar switching scheme are the following:

- Mains frequency (50 Hz) full wave rectified sinusoid
- sawtooth at high frequency (10kHz) with a minimum value of zero

An example of these two inputs is displayed in Figure 36. It should be noted however that for the purpose of the illustration, the sawtooth frequency was reduced to 1 kHz.

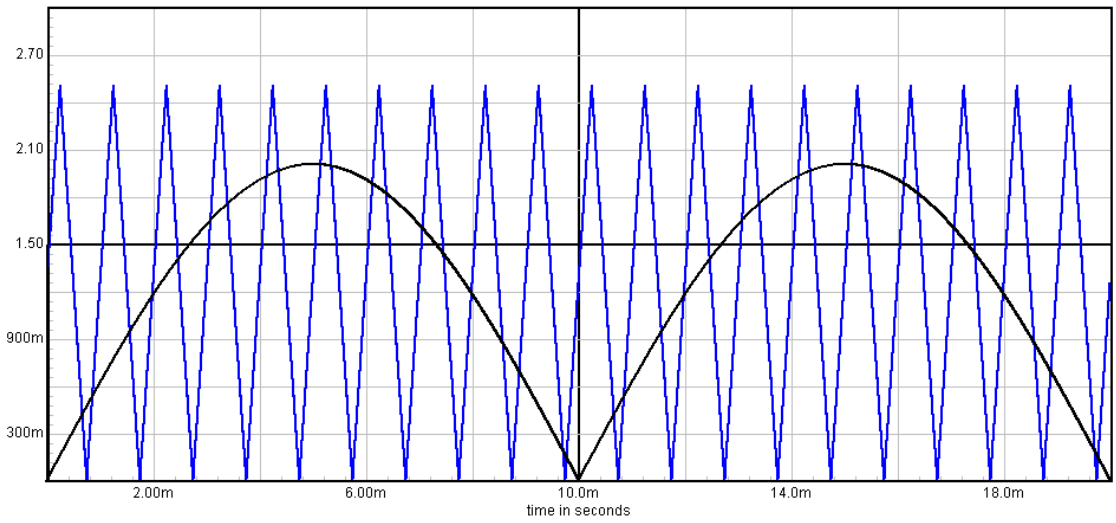

Figure 36: Comparator inputs for generating high frequency PWM control signal for GCTSPPVI

Implementing a Unipolar Switching Scheme

As demonstrated in Table 6 and Table 7, most unipolar switching schemes require high frequency switches to be switching for only half a period. This was achieved by implementation of AND and OR logic gates whose inputs were the output of the comparator compared to a pulsed DC voltage source which remained high for half the period.

The other requirement of most unipolar switching schemes is that while one high frequency switch is closed, the other remains open and vice-versa. This was achieved by using an ideal inverter (Schmitt trigger). As the AND and OR logic gates were models of actual chips, the outputs were not perfectly binary. To overcome this, a standard Schmitt trigger was connected to the output of the logic gates. This is due to the fact that a Schmitt trigger only changes its state if the input goes above or below a threshold voltage. As the ICAP library did not have a standard Schmitt trigger, one was produced by connecting two inverter Schmitt Triggers in series. As all simulations are not concerned with losses this method was acceptable.

It should be mentioned that while commercially available inverters implement a voltage control method or a current control method similar to that outlined in Figure 1 to produce a PWM signal, the comparator method is adequate for all simulation as it will not influence the PV array voltage fluctuation.

14.8 Diode Model Selection

Generic diodes with no reverse breakdown voltage or current limit were implemented. All parameters are displayed in Appendix A in Table 15.

14.9 Sizing of load

As all simulations were designed under the assumption of supplying to the grid at unity power factor, the grid was modelled by a purely resistive, earthed load for all simulations. The load was sized to result in all topologies producing a rated output of 1.5kW. All sizing equations are displayed in Appendix A in Table 15.

14.10 Sizing of LC Filter

AS4777.2 has strict guidelines regarding harmonic content produced by a grid connected inverter. While Section 4.5 of AS4777.2 states the THD of the output current must not exceed 5%, it also lists specific requirements regarding odd and even harmonic content. To ensure all grid connected inverters are in compliance with Section 4.5, the output filter is a crucial component. While it was outside the scope of this report to investigate which output filters were implemented by the various IUT, an LC filter using split inductance was implemented for all simulations to produce a sinusoidal output. As LC filters can become unstable if the resonant frequency of the capacitor is similar to the mains or switching frequency, the filter must be sized accordingly. It should be noted that it is out of the scope of this report to investigate the impact of filters on PV array voltage fluctuation. All sizing equations are displayed in Appendix A in Table 15.

15 Simulation Results

The following section presents simulated PV array voltage fluctuations of the Dc input terminals of the inverter and output voltages for all GCTSPPVI topologies previously introduced. All switching control signals and comparator inputs can be viewed in the appendices.

15.1 Simulations for a Fullbridge Converter Implementing a Bipolar Switching Scheme

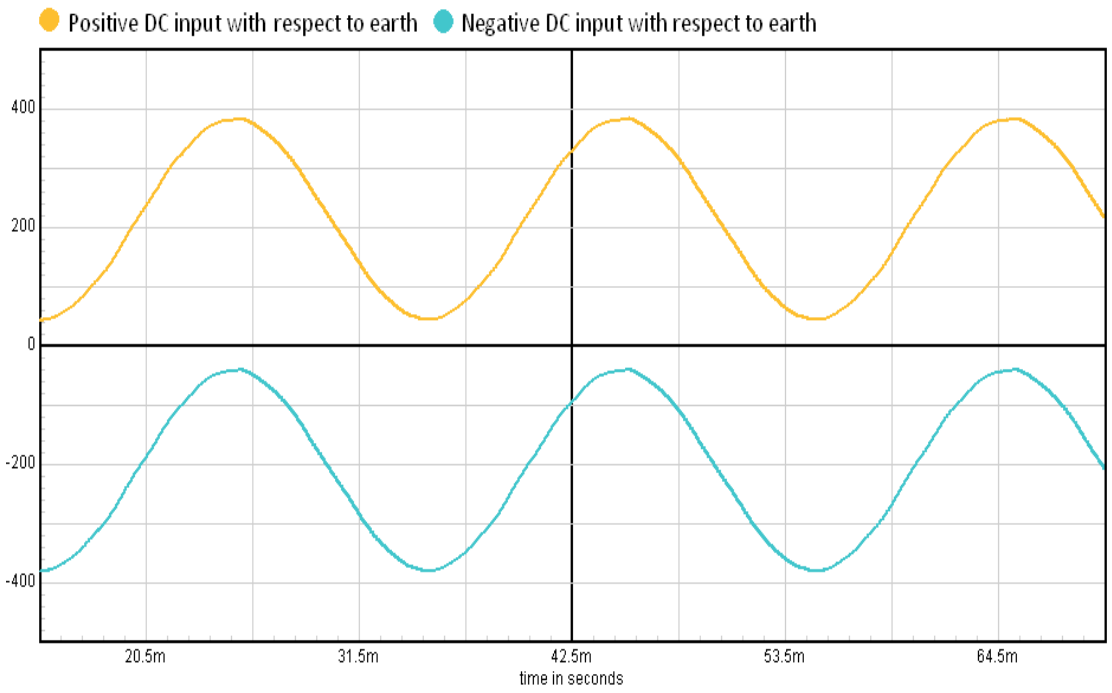

Figure 37: ICAP Simulation of PV Array Voltage Fluctuation for Fullbridge Topology Implementing a Bipolar Switching Scheme with a Split Inductor Output Filter

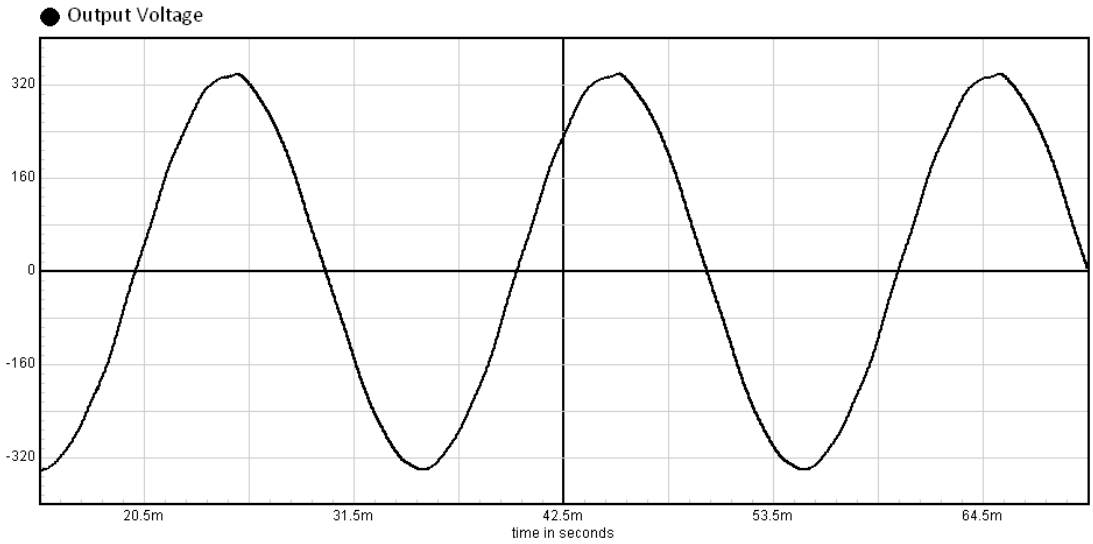

Figure 38: Output Voltage Generated by a Fullbridge Topology Implementing a Bipolar Switching Scheme with a Split Inductor Output Filter

15.2 Simulation of Fullbridge Converter Utilising a Standard Unipolar Switching Scheme

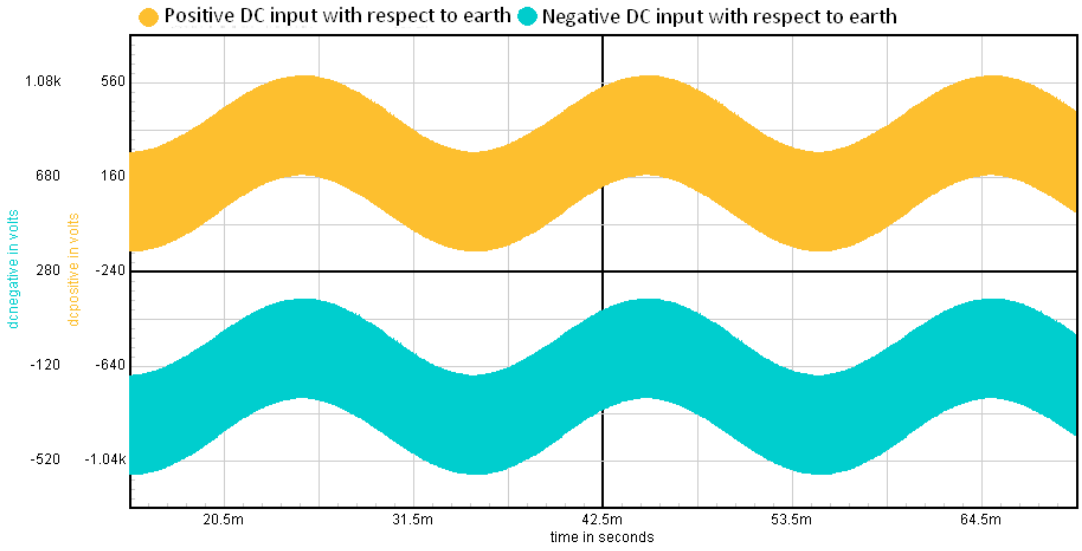

Figure 39: PV Array Voltage Fluctuation for Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter

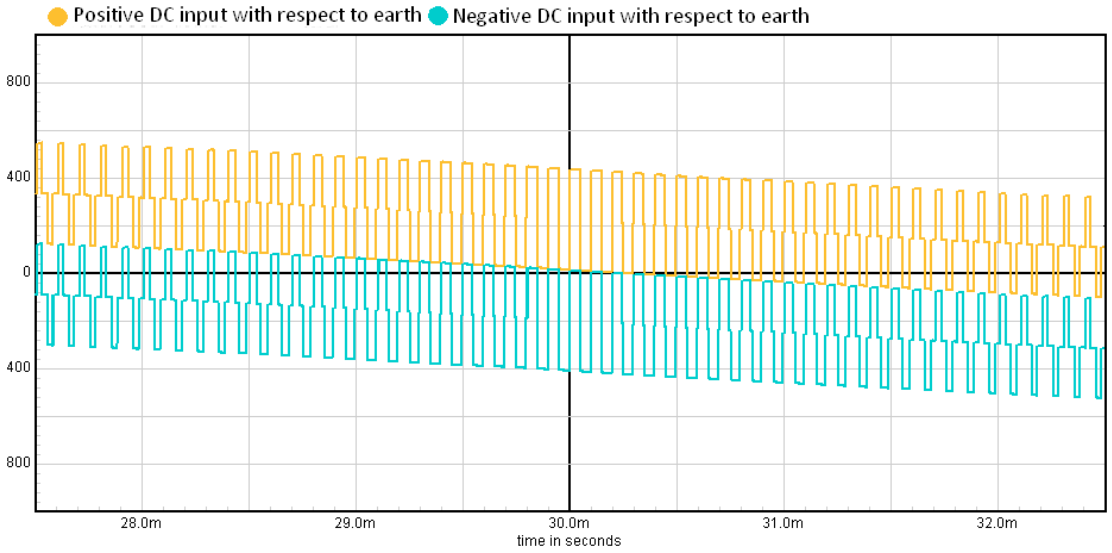

Figure 40: High Resolution of PV Array Voltage Fluctuation at Zero Crossing for a Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter

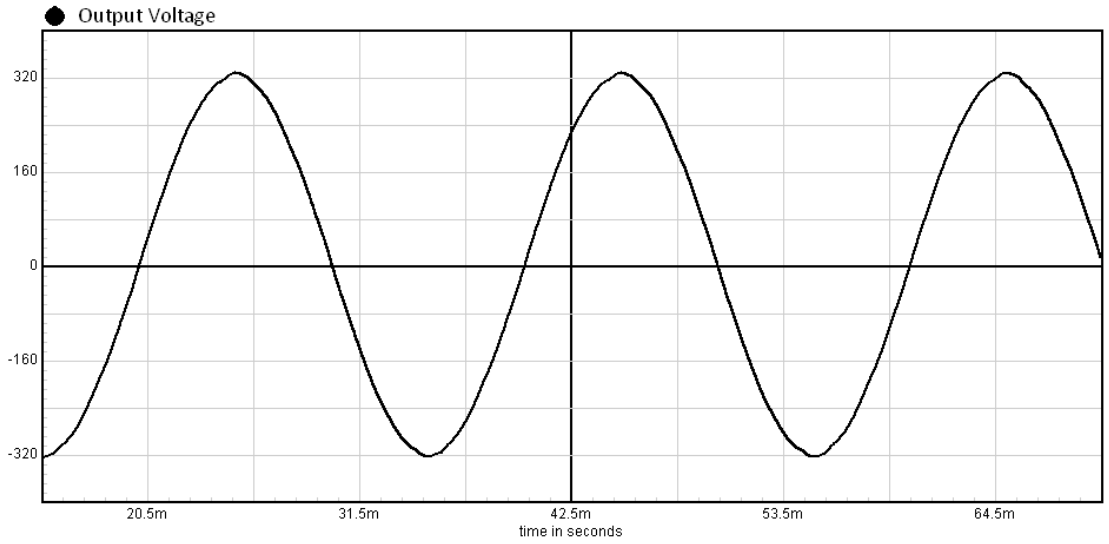

Figure 41: Output Voltage Generated by a Fullbridge Topology Implementing a Standard Unipolar Switching Scheme with a Split Inductor Output Filter

15.3 Simulations for a Fullbridge Converter Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter

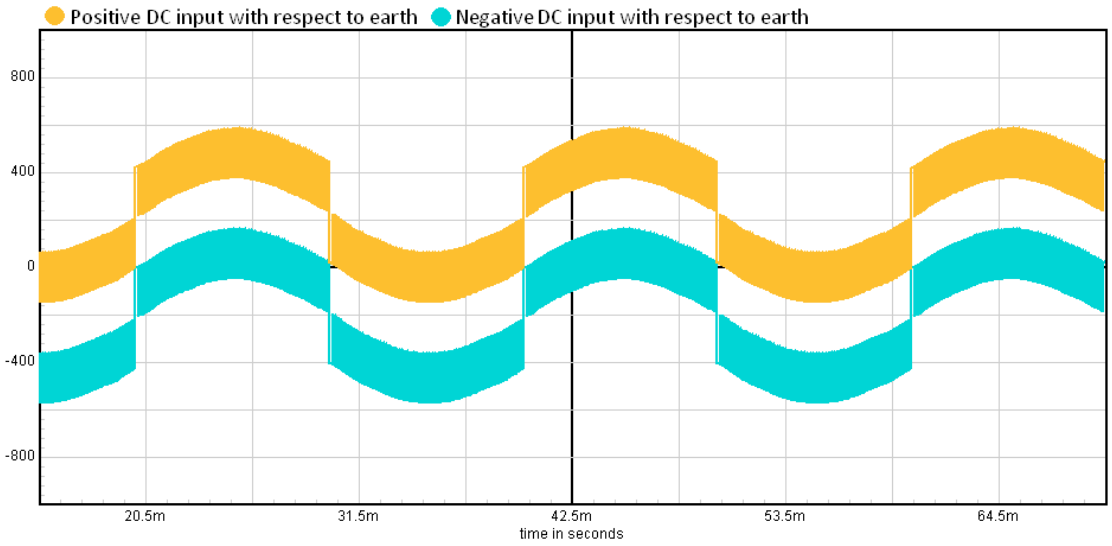

Figure 42: PV Array Voltage Fluctuation for Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme(Type B) with a Split Filter Inductor Output Filter

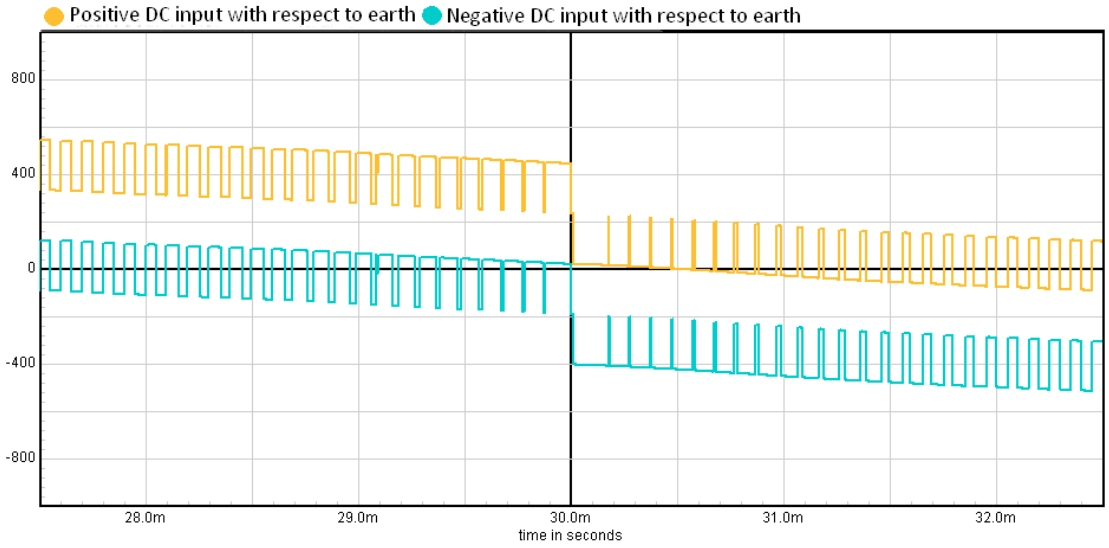

Figure 43: High resolution of PV array voltage fluctuation at Zero Crossing of Output Voltage for a Fullbridge Topology implementing One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter

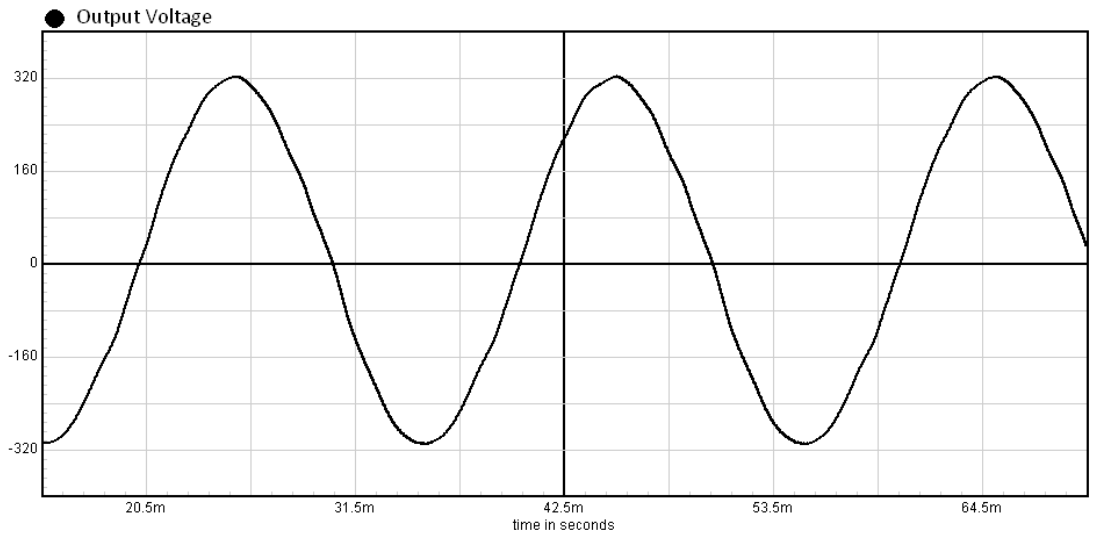

Figure 44: Output Voltage Generated by a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Split Inductor Output Filter

15.4 Simulations for a Fullbridge Converter Utilising a One Phase Chopping Unipolar Switching Scheme (Type B) With Single Output Filter Inductor

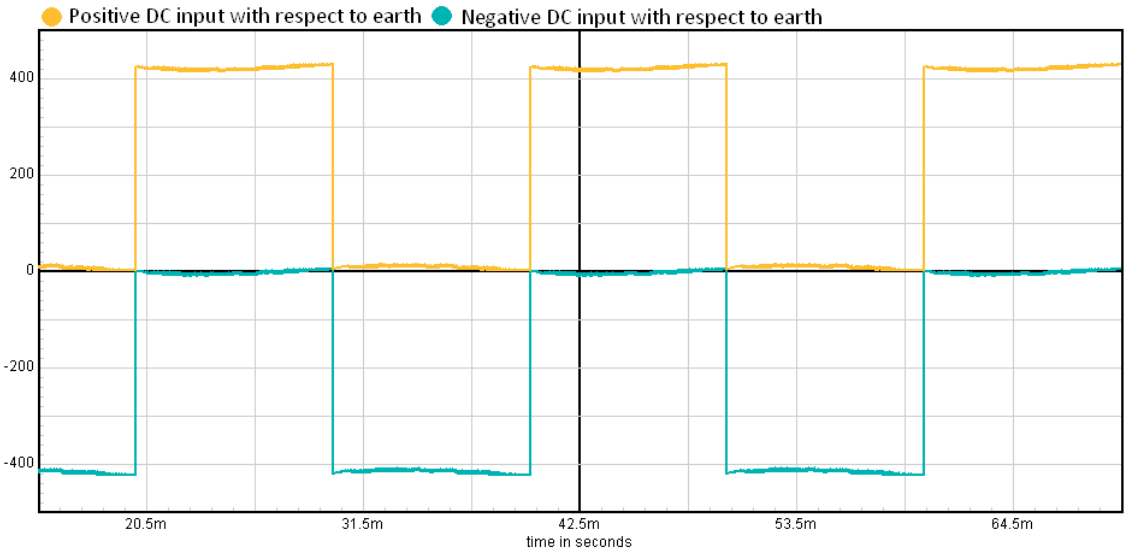

Figure 45: PV Array Voltage Fluctuation of Fullbridge Topology Implementing a One Phase Chopping Switching Scheme (Type B) with a Single Output Filter Inductor

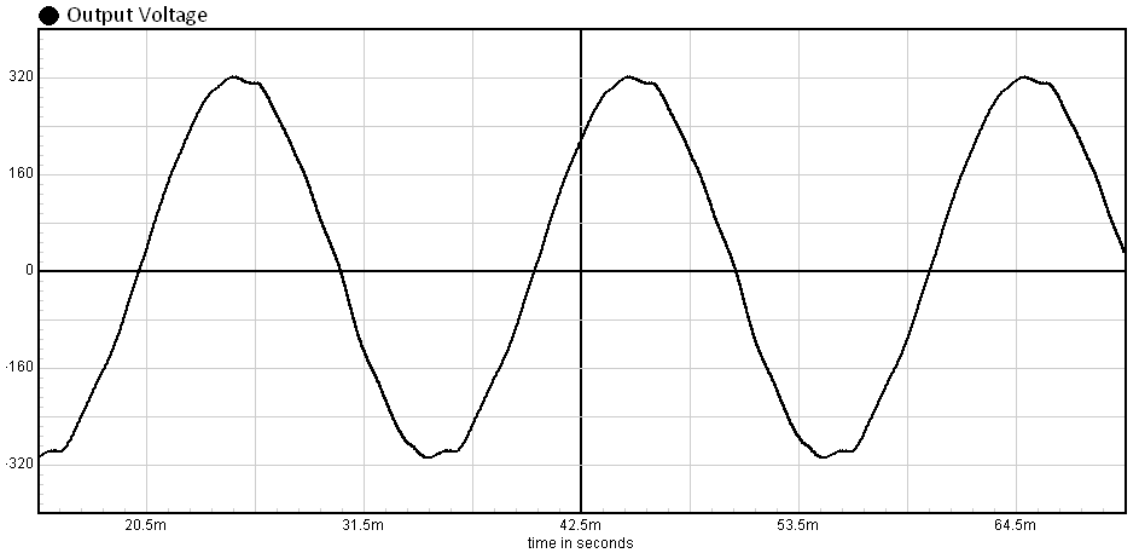

Figure 46: Output Voltage Generated by a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Single Inductor Output Filter

15.5 Simulation of Halfbridge Converter with Single Inductor Output Filter

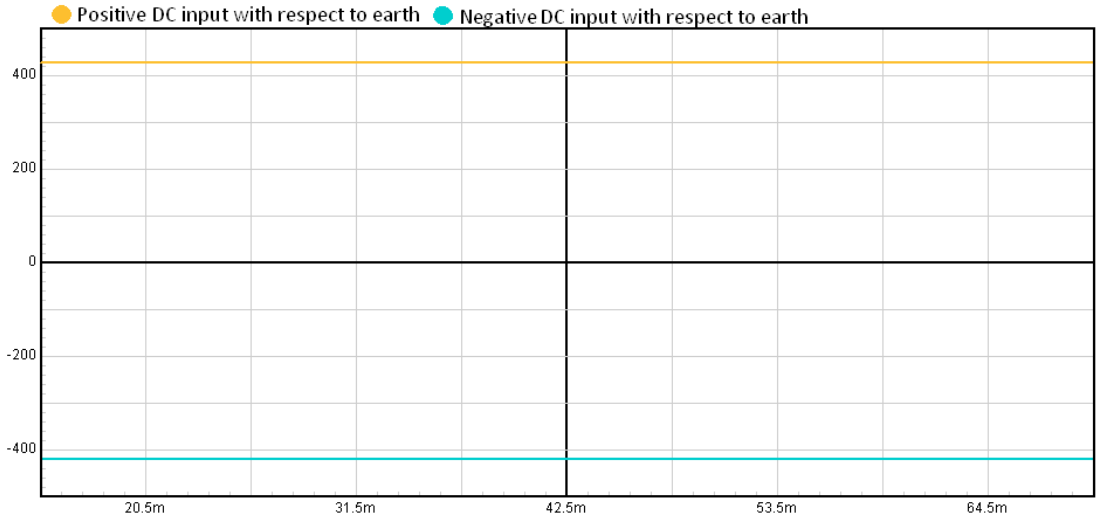

Figure 47: PV Array Voltage Fluctuation for Halfbridge Topology with Single Inductor Output Filter

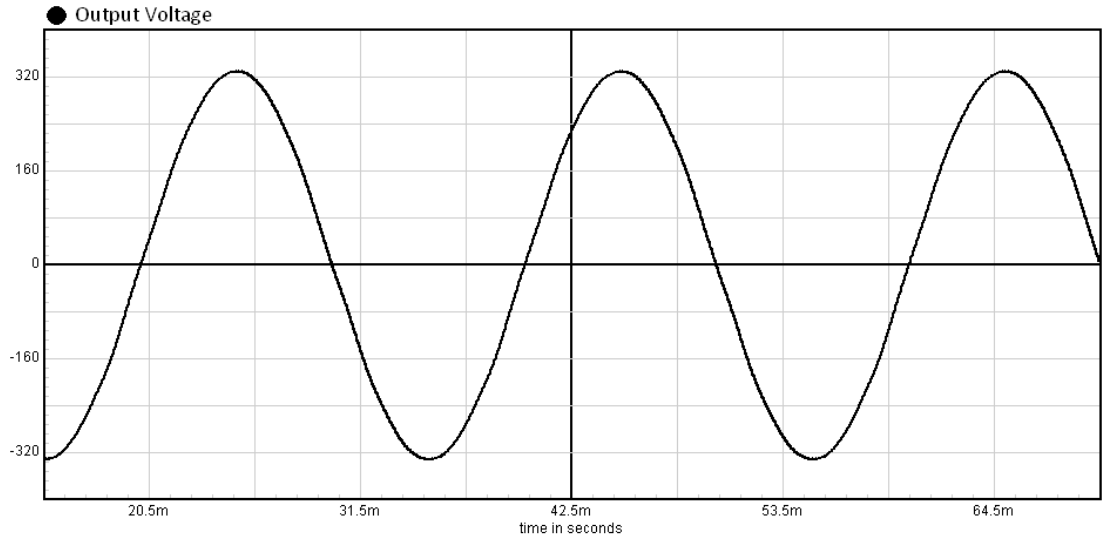

Figure 48: Output Voltage Generated by a Halfbridge Topology with a Single Inductor Output Filter

15.6 Simulation of Halfbridge Converter with Split Inductor Output Filter

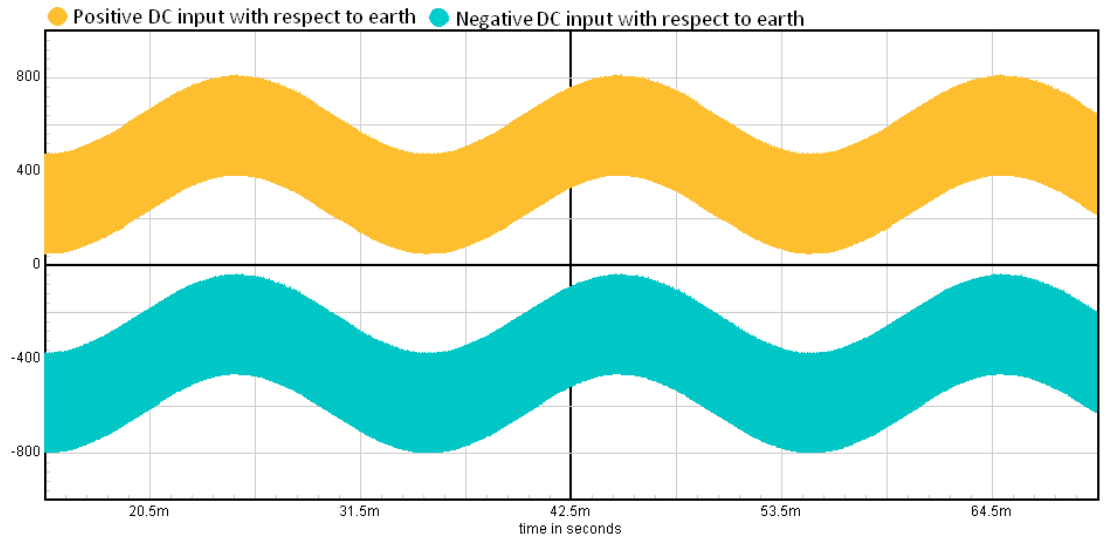

Figure 49: PV Array Voltage Fluctuation for Halfbridge Topology with Split Inductor Output Filter

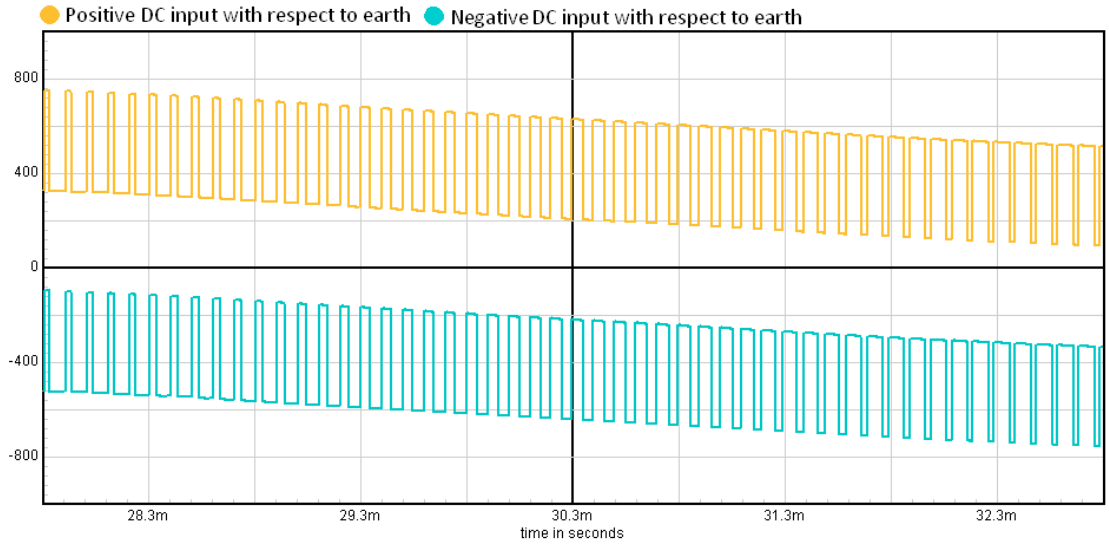

Figure 50: High resolution of PV array voltage fluctuation at Zero Crossing of Output Voltage for a Halfbridge Topology Implementing a Split Inductor Output Filter

15.7 Simulation of HERIC Topology

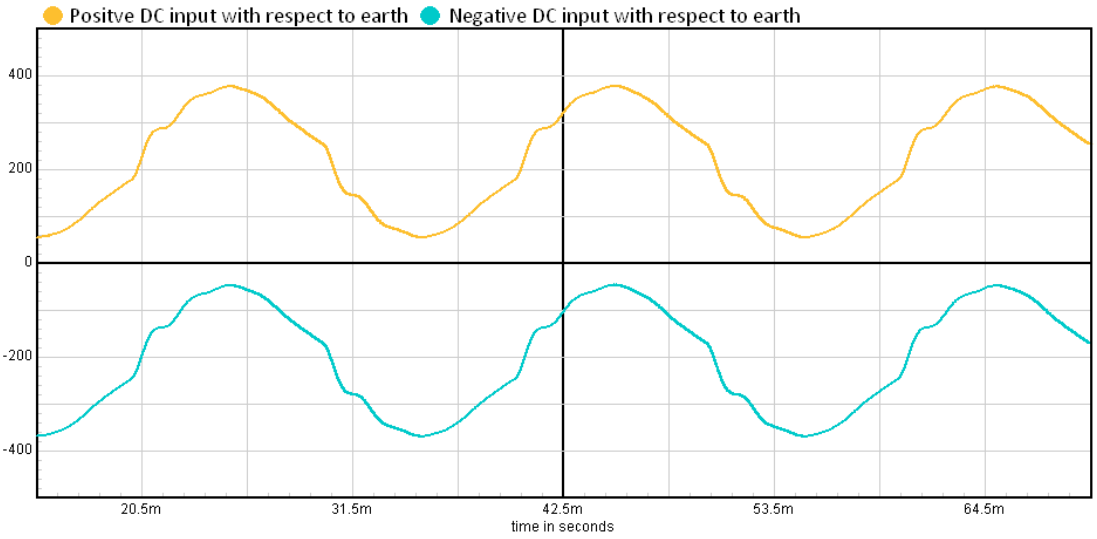

Figure 51: PV Array Voltage Fluctuation for a HERIC Topology with a Split Inductor Output Filter

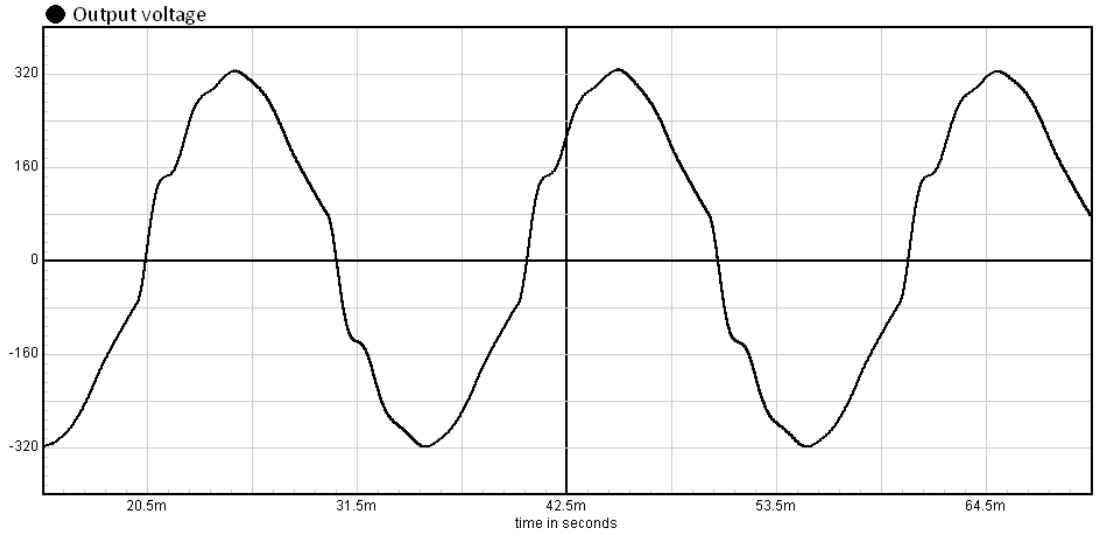

Figure 52: Output Voltage Generated by a HERIC Topology with a Split Inductor Output Filter

15.8 Simulation of H5 Topology

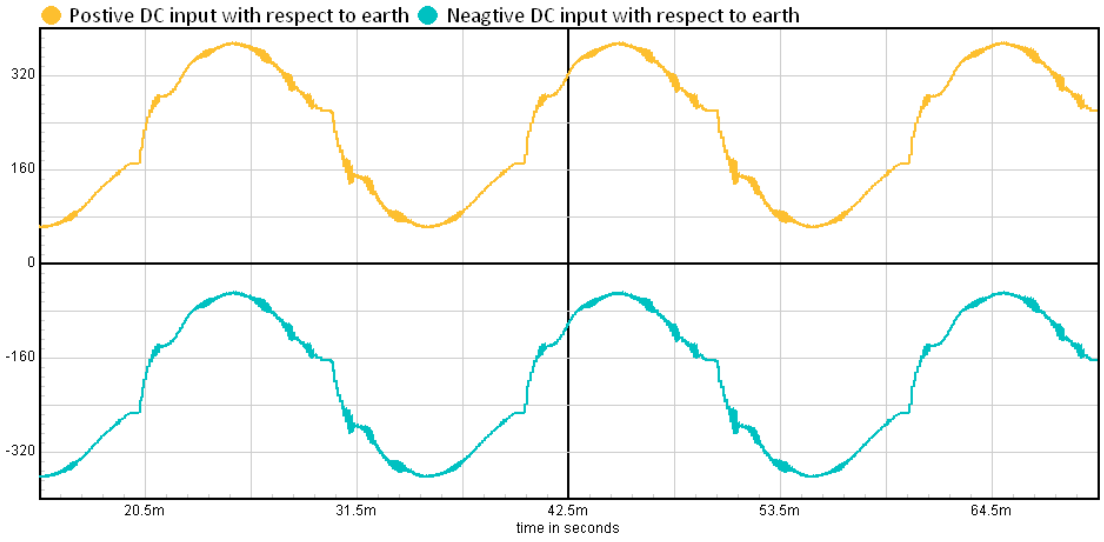

Figure 53: PV Array Voltage Fluctuation for a H5 Topology (with Total Array to Earth Capacitance of 21nF) with a Split Inductor Output Filter

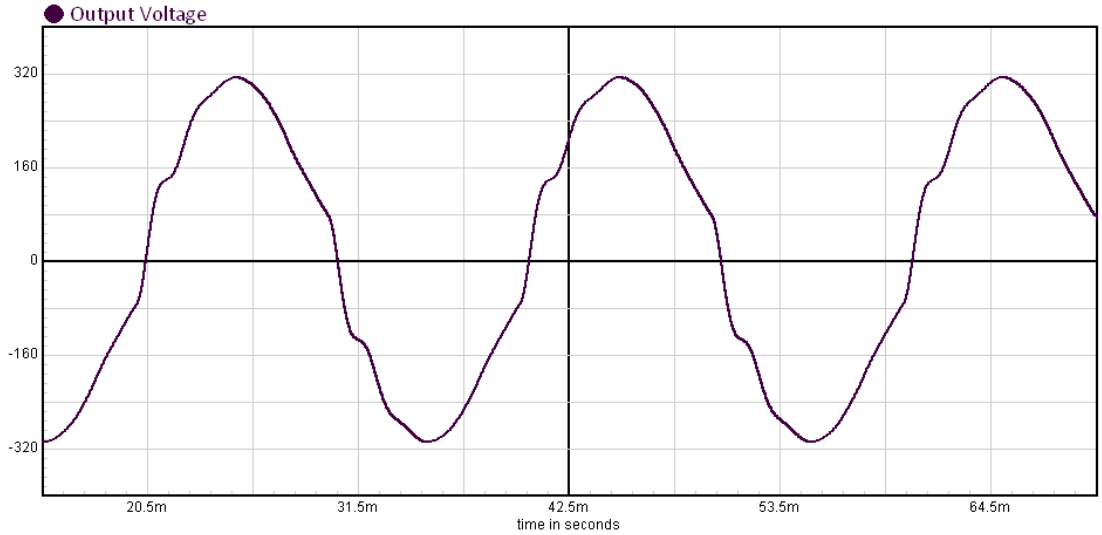

Figure 54: Output Voltage Generated by a H5 Topology with a Split Inductor Output Filter

16 Test Circuit Setup

All PV array voltage fluctuation experimental results were measured during the testing of DC current injection with test circuit setup and procedure outlined in Part A. As a result, the same three GCTSPPVI listed in Table 3 were tested as demonstrated in Figure 2, the output of the PV simulator is measured through three separate channels on a digital oscilloscope. As the input for each channel of the oscilloscope implemented did not share a common ground, the following setup could be used:

- Channel 1: Probe was connected to positive terminal of PV simulator output and measured with respect to ground
- Channel 2: Probe was connected to negative terminal of PV simulator output and measured with respect to ground
- Channel 3:Probe was connected to positive terminal of PV simulator output and measured with negative terminal of PV simulator output

It should also be noted that in each experiment, all references for each channel were set to be the same. This however is not of great concern as the primary interest is the pattern and magnitude of the voltage fluctuation not the offset.

17 Experimental Results

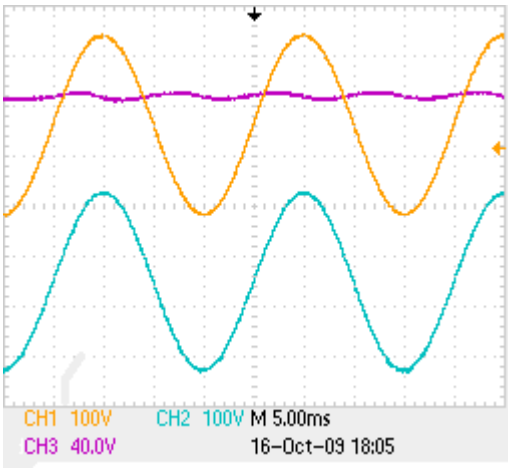

Figure 55: PV Array Voltage Fluctuation for Fullbridge Topology Implementing Bipolar Switching Scheme with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV

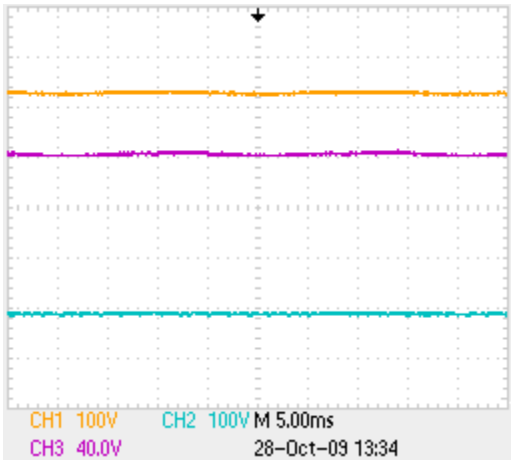

Figure 56: PV Array Voltage Fluctuation for HERIC Topology with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV

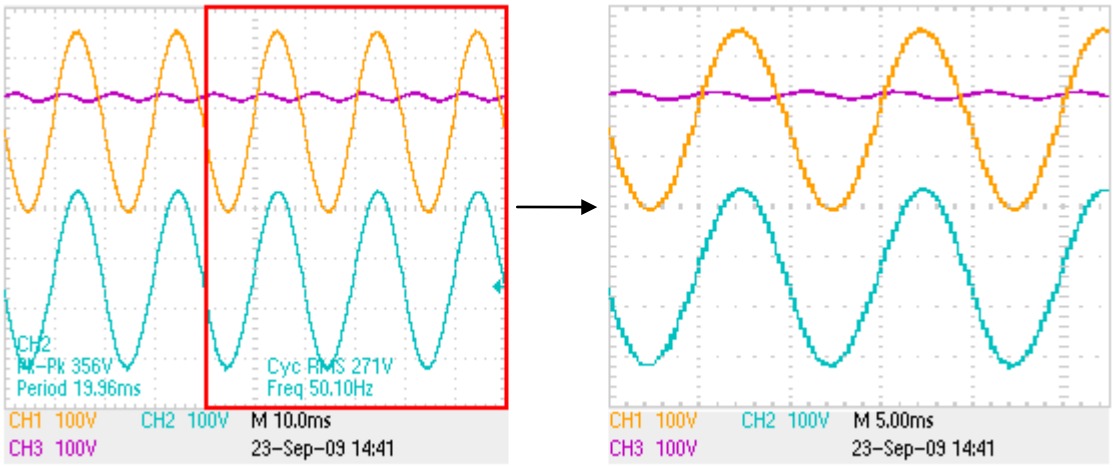

Figure 57: PV Array Voltage Fluctuation for H5 Topology with CH1 Measuring Positive DC input with Respect to Earth, CH2 Measuring Negative DC voltage fluctuation with Respect to Earth and CH3 Measuring ΔV

18 Analysis of PV Array Voltage Fluctuations

The following two tables provide summaries of the simulated and tested PV array voltage fluctuations.

Topology	**Switching Scheme**	**Simulated PV Array Fluctuation**	**Is the Design suitable for GCTSPPVI Applications?**
Fullbridge	Bipolar	**Waveform:** Sinusoidal at mains frequency **Amplitude:** ½ Vgrid	Yes
Fullbridge	Standard unipolar	**Waveform:** Instantaneous PWM steps at twice the switching frequency (20kHz) **Amplitude:** steps of ½ Vgrid	No
Fullbridge with single inductor output filter	One phase chopping unipolar (type B)	**Waveform:** Instantaneous PWM steps at switching frequency (10kHz) **Amplitude:** ½ Vgrid	No
Fullbridge with split inductor output filter	One phase chopping unipolar (type B)	**Waveform:** Instantaneous steps at mains frequency (50Hz) **Amplitude:** Vgrid	
Halfbridge with single inductor output filter	Bipolar	**Waveform:** DC **Amplitude:** Negative DC input at –Vgrid	Yes
Halfbridge with split inductor output filter	Bipolar	**Waveform:** Instantaneous PWM steps at switching frequency **Amplitude:** Vgrid	Yes
HERIC	Unipolar	**Waveform**: Sinusoidal at mains frequency **Amplitude:** ½ Vgrid	Yes
H5	Unipolar	**Waveform:** Sinusoidal at mains frequency **Amplitude:** ½ Vgrid	Yes

Table 11: Various Switching Schemes and Associated Voltage Fluctuations

Topology	Switching Scheme	Experimental PV Array Fluctuation	Did Experimental Results Verify Simulated Results
Fullbridge	Bipolar	**Waveform:** Sinusoidal **Amplitude:** ½ Vgrid	Yes
HERIC	Unipolar	**Waveform**: DC. **Amplitude:** Negative DC input grounded	No
H5	Unipolar	**Waveform:** Sinusoidal **Amplitude:** ½ Vgrid	Yes

Table 12: Summary of Comparison between Experimental Results and Simulations

All simulations except for the HERIC topology both corresponded with past literature and the experimentally test results. The tested GCTSPPVI utilising a HERIC topology produced DC fluctuation with the negative DC input constantly remaining at zero Volts where as the simulation clearly produced a mains frequency sinusoidal array fluctuation with an amplitude of half the grid voltage. While this initially seemed contradictory, [20] describes three different GCTSPPVI designs which incorporate the HERIC topology. [20] states that the all AT series GCTSPPVI consist of a front end DC actuator which connects the negative terminal of PV array to the neutral of the grid and therefore, to ground. As the tested GCTSPPVI incorporating the HERIC topology was a Sunways AT2700, tested and simulations results do not contradict one and other but in fact verify the difference in PV array voltage fluctuation between HERIC topologies which do or not implement a front end DC actuator.

While all simulated array voltage fluctuations matched the general trend of both tested results and expected results based on past literature, there were some minor discrepancies. In particular both simulations of the H5 and HERIC topologies are significantly distorted at the zero crossing of the output voltage. As can be seen in Figure 58 and Figure 59, the non ideal nature of the implemented comparator resulted in semi states when the sawtooth was above the reference signal for a very small period of time were the comparator output was neither high or low.

While this resulted in non perfect sinusoidal outputs, it in no way diminishes the validity of the simulations regarding PV array voltage fluctuation.

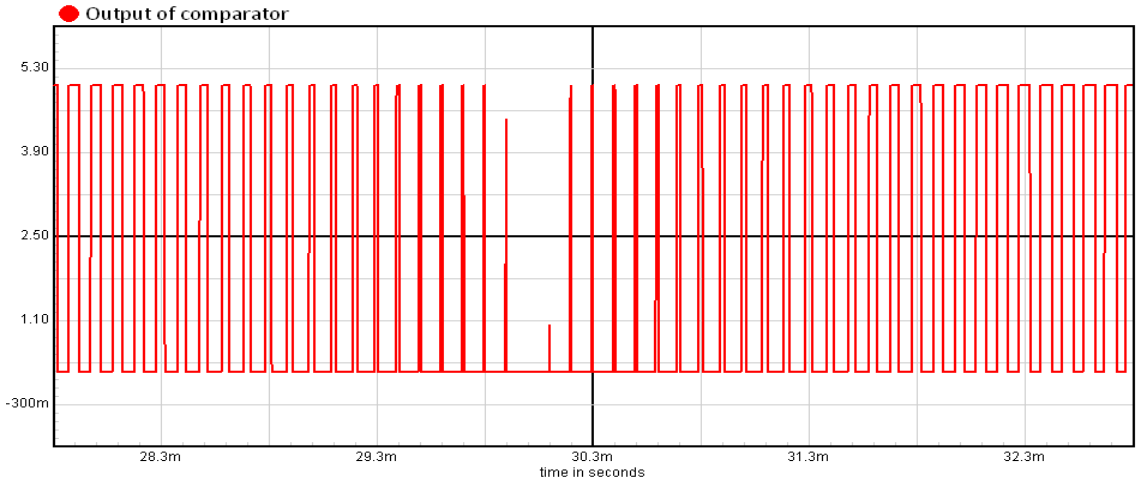

Figure 58: Comparator Output of H5 Topology

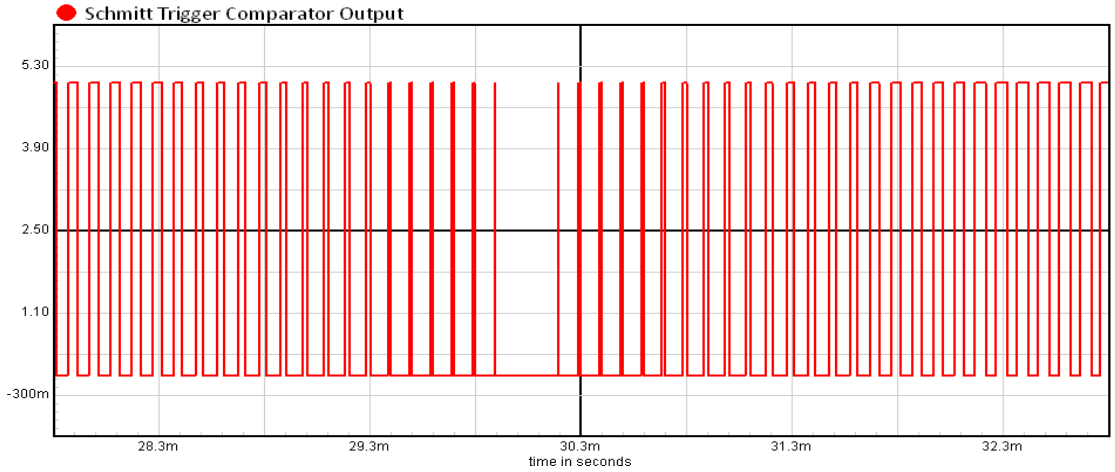

Figure 59: Output of Comparator After two Schmitt Inverters

Another discrepancy which can be seen in Figure 53 is the small noise component of the PV array voltage fluctuation of the H5 topology. This is due to the H5 topology simulation being the only simulation with modelled array capacitance and therefore the only simulation producing leakage current. As the leakage current is fluctuating, the DC input current will also fluctuate causing the PV array voltage to have a small "noisy" high frequency fluctuation.

19 Conclusions

All simulations and experimental results successfully demonstrated which GCTSPPVI topologies, switching schemes and output filter configurations are suitable for PV applications in regards to reducing PV array voltage fluctuation and capacitive leakage current. Additionally, this report has provided future Murdoch University students with a clear and concise introduction into the operation of various GCTSPPVI and provided models for the most common GCTSPPVI topologies.

20 Recommendations and Future Works

Based on the associated advantages of each switching scheme, it would seem the H5 and HERIC topologies have a high potential to drastically increase their market share of installed GCTSPPVI in the future. This is due to their ability to utilise the higher efficiency of a unipolar switching scheme without the associated high frequency voltage fluctuations. In particular, the H5 topology can achieve this with only one additional switch which can be controlled without the requirement of an additional control signal by interconnecting the control signal of S3 and S4 [21].

While this report has provided extensive modelling, simulations and testing for most common GCTSPPVI designs, there are additional topologies that have not been investigated. In particular, topologies including a symmetrical boost converter, neutral point clamped (NPC) and HERIC with a front end DC actuator could all be simulated. It may also be of benefit to measure the PV array voltage fluctuation of a GCTSPPVI implementing a halfbridge converter topology with a single inductor output filter to verify simulated results.

PART C: OVERVIEW OF REPORT

21 Conclusions and Final Comments

Part A of this report has presented a clearly defined test circuit setup and procedure for testing DC current injection for grid-connected single-phase photovoltaic inverters implementing both transformerless and high frequency transformer topologies. The setup and procedure has been experimentally tested by using two commercially available and one anonymous GCTSPPVI design utilising different topologies. The results demonstrated that the test circuit setup and testing procedure could be suitable for inclusion in a future amendment to AS4777.2. It is however proposed that before these amendments are recommended, further investigation is required to demonstrate whether it is sufficient to test all IUT solely at their rated output as opposed to different power levels. Additionally, further investigation is required in regards to the non repeatability of DC current injection in certain GCTSPPVI designs to determine whether one or two tests will be sufficient per IUT.

Part B of this report has defined and modelled a variety of GCTSPPVI topologies, switching schemes and output filter configurations and clearly defined their operation. All of these various models have been simulated to determine which designs are suitable for GCTSPPVI applications in regards to reducing PV array voltage fluctuation and capacitive leakage currents to eliminate potential risks to users and to ensure EMC. Two commercially available and one anonymous GCTSPPVI models utilising a selection of the simulated topologies and switching schemes were experimentally tested to verify simulated results.

Based on these results it is recommended that the following combination of topologies, switching schemes and output filter configurations are not appropriate for GCTSPPVI applications:

- Fullbridge Topology Implementing a Standard Unipolar Switching Scheme
- Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme(Type B) with a Split Filter Inductor Output Filter
- Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) with a Single Inductor Output Filter
- Halfbridge Topology with Split Inductor Output Filter

Finally, Part B of this report has provided future Murdoch University students with a clear and concise introduction into the operation of various GCTSPPVI and provided models for the most common GCTSPPVI topologies. The generated simulations of these selected GCTSPPVI will also serve as an ideal learning aid.

References

1. Martina Calais, Andrew Ruscoe, and M. Dymond, *Transformerless PV Inverter Issues Revisited, Are Australian Standards Adequate?*, in *Solar09, the 47th ANZSES Annual Conference*. 29 September-2 October 2009,: Townsville, Queensland, Australia.
2. Fritz Schimpf and L.E. Norum, *Grid connected Converters for Photovoltaic, State of the Art, Ideas for Improvement of Transformerless Inverters*, Norwegian University of Science and Technology, NTNU Department of Electrical Power Engineering: Trondheim, Norway.
3. B. Bletterie, et al., *Deliverable 2.3 Identification of general safety problems, definition of test procedures and design-measurements for protection.* Project Dispower 2006.
4. Krawietz, S., *Building the future: New possibilities for thin films in building integrated PV* Renewable Energy World Magazine, September/October 2007. **10**(5).
5. Rozenblat, L. *Electrical Power Transformer and Inductor*. [Web Page] [cited 15/10/09]; Available from: http://www.smps.us/magnetics.html.
6. Matthew Armstrong, et al., *Auto-Calibrating DC Link Current Sensing Technique for Transformerless, Grid Connected, H-Bridge Inverter Systems.* IEEE TRANSACTIONS ON POWER ELECTRONICS,, 2006. **VOL. 21**(NO. 5,).
7. Krismadinata, Nasrudin Abd Rahim, and J. Selvaraj, *Implementation of Hysteresis Current Control for Single-Phase Grid Connected Inverter.* Power Electronics laboratory Department of Electrical Engineering University of Malaya Kuala Lumpur, Malaysia, 2007.
8. Guo Xiaoqiang, et al., *DC Injection Control for Grid-Connected Inverters Based on Virtual Capacitor Concept.* Key Lab of Power Electronics for Energy Conservation and Motor Drive of Hebei Province.
9. Bowtell, L. and T.L. Ahfock, *Comparison between unipolar and bipolar single phase grid-connected inverters for PV applications*, in *AUPEC 2007*. 2007, Curtin University of Technology: Perth, Australia.
10. Technologies, A. *Understanding the Autozero Function*. [web page] [cited 23/11/09]; Available from: www.home.agilent.com/agilent/editorial.jspx?cc=SG&lc=eng&ckey=698734&nid=-536902435.0.00&id=698734&NEWCCLC=FRfre.
11. Calais, M., *Investigation of a Single-Phase Five Level Cascaded Inverter for DC Sources such as Photovolaics.* 2002.
12. Roberto Gonzalez, J.L., Pablo Sanchis, Eugenio Gubia, Alfredo Ursua, Luis Marroya,, *High-Efficiency Transformerless Single-phase Photovoltaic Inverter.* Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International, 2006.
13. T. Kerekes, R. Teodorescu, and U. Borup, *Transformerless Photovoltaic Inverters Connected to the Grid.* 2007.
14. Lin Ma, et al., *Leakage current analysis of a single-phase transformer-less PV inverter connected to the grid.* 2008.

15. J. M. A. Myrzik and M. Calais, *String and Module Integrated Inverters for Single-phase Grid Connected Photovoltaic Systems - A Review* 2003 IEEE Bologna Power Tech conference, 2003.
16. Tamás Kerekes, M., IEEE, , et al., *A new high-efficiency single-phase transformerless PV inverter topology.* 2009.
17. Gerardo Vazquez, et al., *Losses and CMV Evaluation in Transformerless Grid-Connected PV Topologies.* IEEE International Symposium on Industrial Electronics (ISIE 2009) Seoul Olympic Parktel, Seoul, Korea, July 5-8, 2009.
18. Heribert Schmidt, C. Siedle, and J. Ketterer, *DC/AC Converter to Convert Direct Electric Voltage into Alternating Voltage or into Alternating Current*, U.S. Patent, Editor. 2006.
19. Ned Mohan, Tore M. Underland, and W.P. Robbins, *Power Electronics: Converter, Applications, and Design*. 3rd ed, ed. B. Zobrist. 2003: John Wiley & Sons, Inc. 802.
20. Technology, S.P., *Compatability between Inverter and Module Technologies.* 2008.
21. M. Victor, et al., *Method of Converting a Direct Current Voltage from a Source of Direct Current Voltage, More Specifically from a Photovoltaic Couse of Direct urrent Voltage, Into a Alternating Current Voltage*. 2005: United States.
22. AS4777.2, *Grid connection of energy systems via inverters, Part 2: Inverter requirements*

2005, Sydney: Standards Australia.

23. IEEE, *Std 929-2000.* Utility Interface of Photovoltaic (PV) Systems, 2000.
24. IEEE, *Std 1547.1-2005.* IEEE Standard Conformance Test Procedures for Equipment, 2005.
25. Commission, I.E., *IEC 61727 Ed.2: Photovoltaic (PV) systems - Characteristics of the utility.* 2004.
26. V. Salasa, E.O.a., M. Alonsob, F. Chenlo, *Overview of the legislation of DC injection in the network for low voltage small grid-connected PV systems in Spain and other countries.* Photovoltaic Solar Energy CIEMAT.
27. *Automatic disconnection device between a generator and the public low-voltage grid.* DIN V VDE V 0126-1-1:2006-02, 2006.
28. *UL 1741: Inverters, Converters, Controlers and Interconnection System Equipment for Use with Distributed Energy Resources.*

Appendix A: Additional Tables

Country	Standard	Year Published	DC Current Injection
Australia	AS4777	Current	"In the case of a single-phase inverter, the d.c. output current of the inverter at the a.c. terminals shall not exceed 0.5% of its rated output current or 5 mA, whichever is the greater" [22]
USA	IEEE929-2000	2000	"The PV system should not inject dc current > 0.5% rated inverter output current into the ac interface under either normal or abnormal operating conditions" [23]
USA	IEEE Std 1547.1-2005	2005	Discusses testing procedure. In particular, it stipulates to test the inverter at 33, 66 and 100% of its continuous rated output current. The averaging for dc current measurements must be less than one cycle but less than 60. Measurements should be taken for 5 minutes [24]
International	IEC 61727 Ed 2	2004	"The PV system shall not inject DC current greater than 1% of the rated inverter output current, into the utility AC interface under any operating condition" [25]
United Kingdom	G83 England G77	Current in 2006	"Use of an isolation transformer is recommended. A DC injection detection device with inverter disable is required for transformerless inverters, the maximum DC current limit is 5 mA" [26]
Japan	Technical Guideline for the Grid Interconnection of Dispersed Power Generating Systems	Current in 2006	"DC injection detection device with inverter disable is required for transformerless inverters. Maximum allowable DC current level is 1% of inverter rated current" [26]
Germany	*DIN V VDE V 0126-1-1:2006-02*.	2006	DC injection due to a system fault needs to be prevented wand disconnection is required within 0.2s. The fault itself or the measurement of the DC current can be used as a criterion for disconnection. The test of prevention of the DC injection is tested either: a) By injecting a DC current of 1 A into the measurement setup of the inverter (shunt, or a sensor). The prevention of injection/disconnection has to occur within 0.2s. b) Simulation of a fault and concurrent

			measurement if the injected current. If the DC component is > than 1 A, disconnection has to occur within 0.2s. [27]
Spain	RD1663/2000	Current in 2006	No dc current limits [26]
USA	UL 1741	2005	<0.5% [28](was removed in May 2007 and replaced by IEEE929)

Table 13: Standards Regarding DC Current Injection for GCTSPPVI

Inverter Under Testing	**Nominal Output**	**Tolerable Maximum DC Current Injection to be in Accordance with AS4777**	**Result**
SMA SB5000TL: H5 Topology	4.6kW	$\left(\frac{4.6\text{kW}}{240\text{V}}\right) \times 0.5\%$ =95.83mA	Compliant
Anonymous GCTSPPVI : Fullbridge Topology,	1.5 kW	$\left(\frac{1.5\text{kW}}{240\text{V}}\right) \times 0.5\%$ =31.25mA	Non-Compliant
Sunways AT2700: HERIC Topology	2.7 kW	$\left(\frac{2.7\text{kW}}{240\text{V}}\right) \times 0.5\%$ =56.25mA	Compliant

Table 14: Calculated Maximum DC Current Injection Levels

Component	Model	Value
PV Array	DC Voltage Source	$V_{DC} = \frac{2.5}{2} \times 240V \times \sqrt{2}$ $= 424.26V$
Diode	(Default)	*Junction Potential=1 V* *Reverse Breakdown Voltage=∞*
Resistive load	-	$R_{Load} = \frac{{V_{Grid}}^2}{P_{Rated}} = \frac{240V^2}{1500W} = 38.4\Omega$
Voltage controlled Switch	Schmitt Trigger	*Threshold Voltage=4.98V*
LC Filter	-	$Size\ for\ Z_{total\ L}$ $0.02 \times R_{Load} = 0.768\Omega$ $Z_l = 0.384\Omega$ $\therefore L = \frac{0.384}{2\pi 50} = \mathbf{1.22mH}$ $\omega_C = \sqrt{(2\pi 50)(2\pi f_{switching})}$ $= 4442$ $LC = (\frac{1}{\omega_C})^2$ $\therefore C = \mathbf{0.0415mF}$
RC dead time filter	-	$Size\ for\ dead\ time = 0.5\%\ of\ t_{switching}$ $= 0.005 \times 100\mu s = 50ns$ $e^{\frac{-t}{RC}} = e^{-1}$ $A\ reasonable\ combination\ would\ be:$ $\boldsymbol{R = 5\Omega}$ $\boldsymbol{C = 100nF}$
AND Logic Gate	54HCT08	-
OR Logic Gate	F4HCT32	-
Inverter	74HCT14 (Schmitt	-

	Trigger)	
Full-Wave Rectifier	ABS (ideal)	Math Function

Table 15: ICAP Model Component selection and Sizing

Appendix B: Additional Calculations

$$+V_{DC-earth} - (-V_{DC-earth}) = V_{DC} = 240 \times \sqrt{2} \times \frac{2.5}{2} = 424.26V$$

$$V_{L1} = V_{L2}$$

$$V_{DC} = V_{L1} + V_{L2} + V_{Grid}$$

$$V_{Grid} = 0V$$

$$\therefore V_{DC} = V_{L1} + V_{L2}$$

$$V_{L1} = V_{L2} = \frac{V_{DC}}{2} = 212.13V$$

For Switching State 1:

$$+V_{DC-earth} = V_{L1} + V_{Grid}$$

$$-V_{DC-earth} = -V_{L2}$$

$$\therefore \boldsymbol{+V_{DC-earth} = 212.13V, -V_{DC-earth} = -212.13V}$$

For Switching State 2:

$$+V_{DC-earth} = V_{L2}$$

$$-V_{DC-earth} = -V_{L1} + V_{Grid}$$

$$\therefore \boldsymbol{+V_{DC-earth} = 212.13V, -V_{DC-earth} = -212.13V}$$

Equation 4: PV Array Voltage fluctuation Calculations for Fullbridge Topology Implementing a Bipolar Switching Scheme

$$+V_{DC-earth} - (-V_{DC-earth}) = V_{DC} = 240 \times \sqrt{2} \times \frac{2.5}{2} = 424.26V$$

$$V_{L1} = V_{L2}$$

$$V_{Grid} = 0V$$

For Switching State 1:

$$+V_{DC-earth} = V_{L1} + V_{Grid}$$

$$-V_{DC-earth} = -V_{L2}$$

$$\therefore +\boldsymbol{V_{DC-earth}} = \mathbf{212.13}\boldsymbol{V}, -\boldsymbol{V_{DC-earth}} = -\mathbf{212.13}\boldsymbol{V}$$

For Switching State 2:

$$V_{L1} + V_{L2} = -V_{Grid}$$

$$\therefore V_{L1} = V_{L2} = 0$$

$$-\boldsymbol{V_{DC-earth}} = \boldsymbol{V_{L1}} + \boldsymbol{V_{Grid}} = -\boldsymbol{V_{L2}} = \mathbf{0}, +\boldsymbol{V_{DC-earth}} = -\mathbf{424.26}$$

Equation 5: PV Array Voltage fluctuation Calculations for Fullbridge Topology Implementing Unipolar One Phase Chopping Switching Scheme

Appendix C: Additional Figures

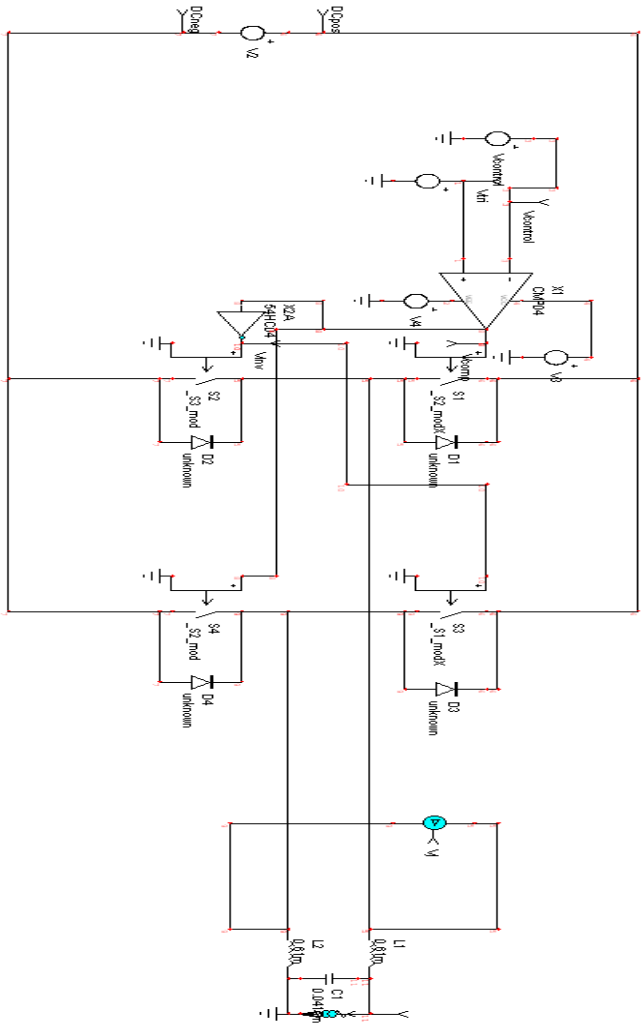

Figure 60: ICAP Model of Fullbridge Converter Implementing Bipolar Switching Scheme

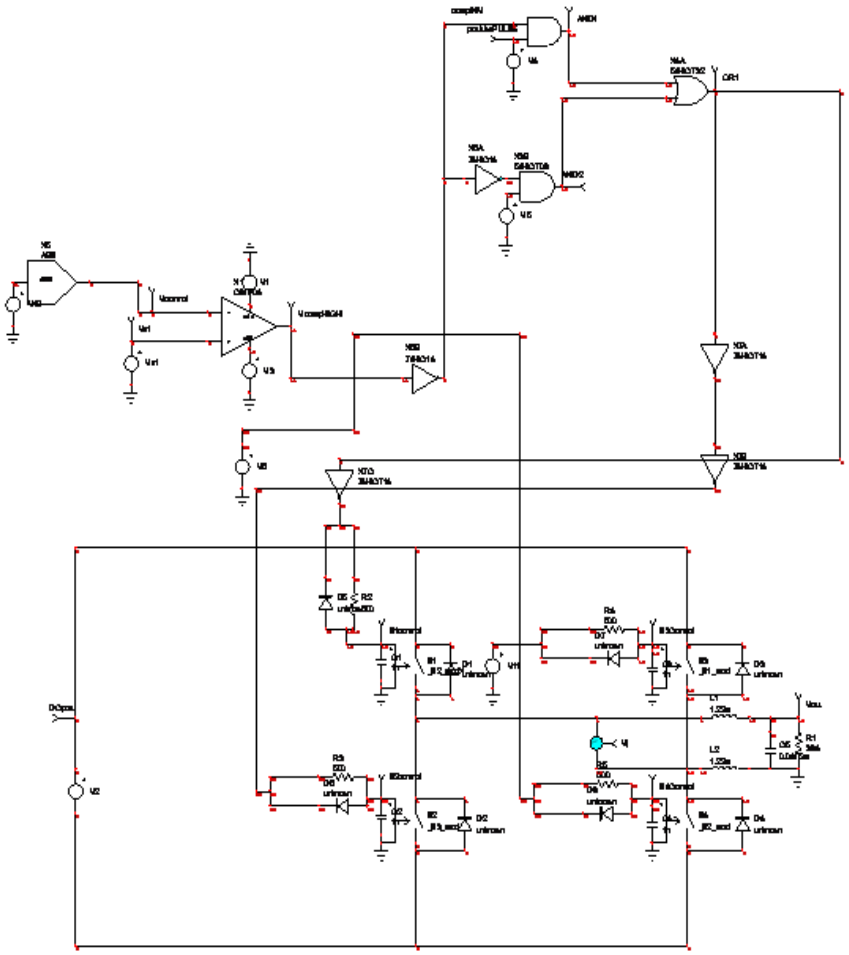

Figure 61: ICAP Model of Fullbridge Converter Implementing One Phase Chopping Unipolar Switching Scheme (Type B)

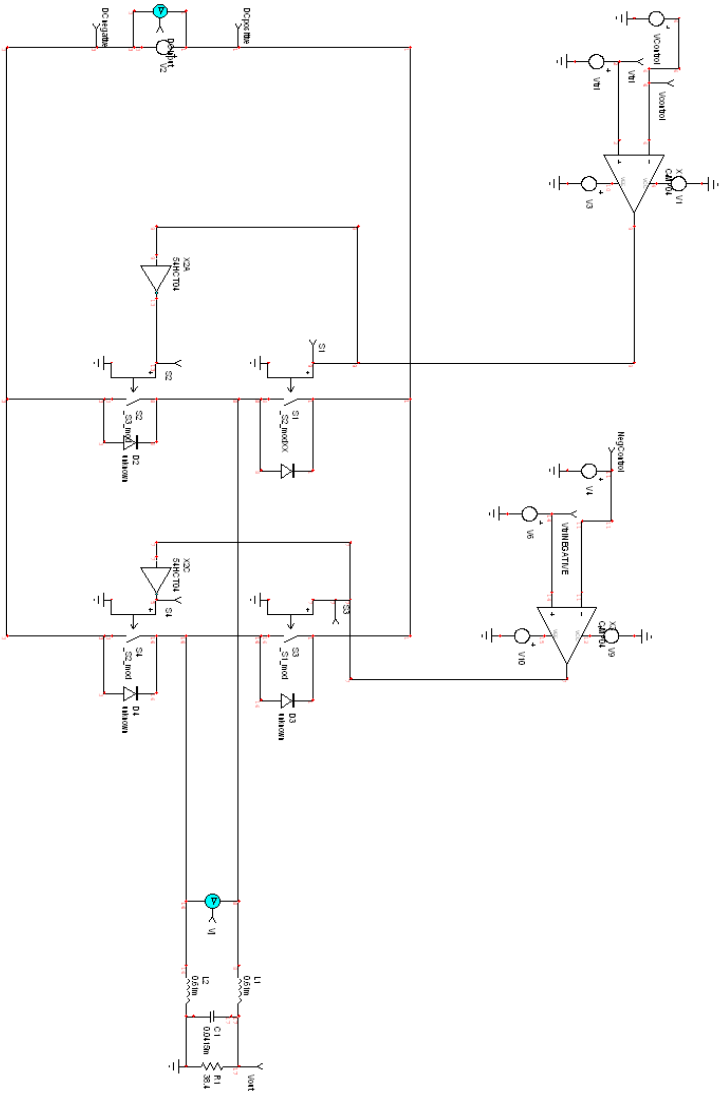

Figure 62: ICAP Model of Fullbridge Converter Implementing Unipolar Switching Scheme [19]

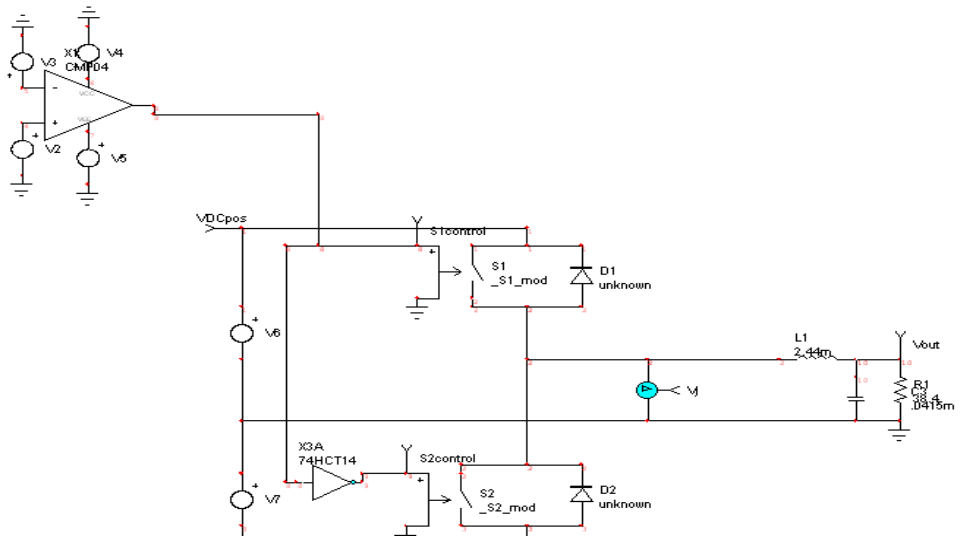

Figure 63: ICAP Model of Halfbridge with Single Filter Inductance

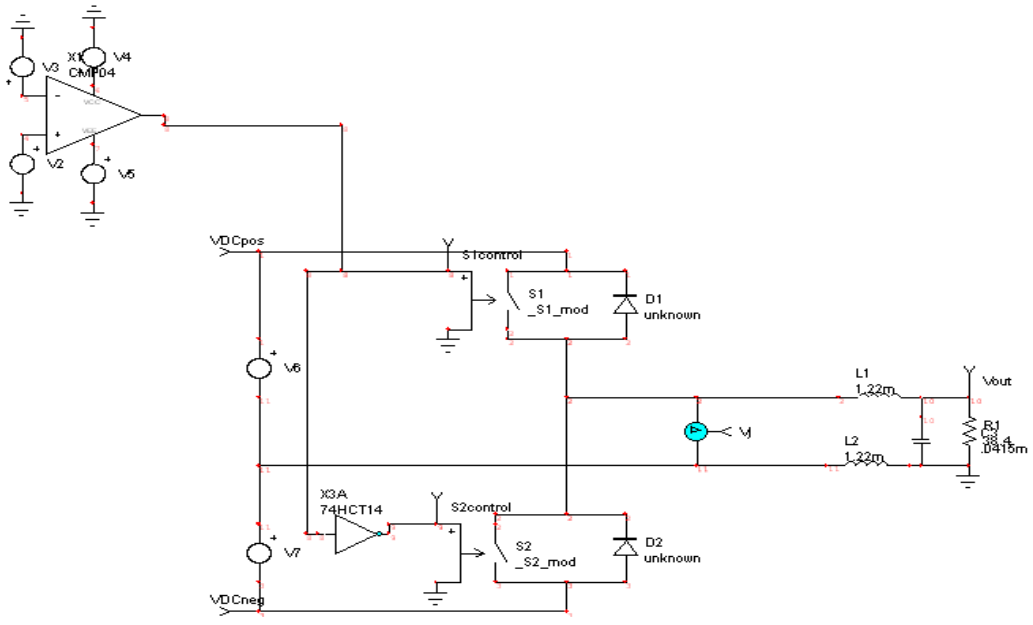

Figure 64: Halfbridge with Split Filter Inductance

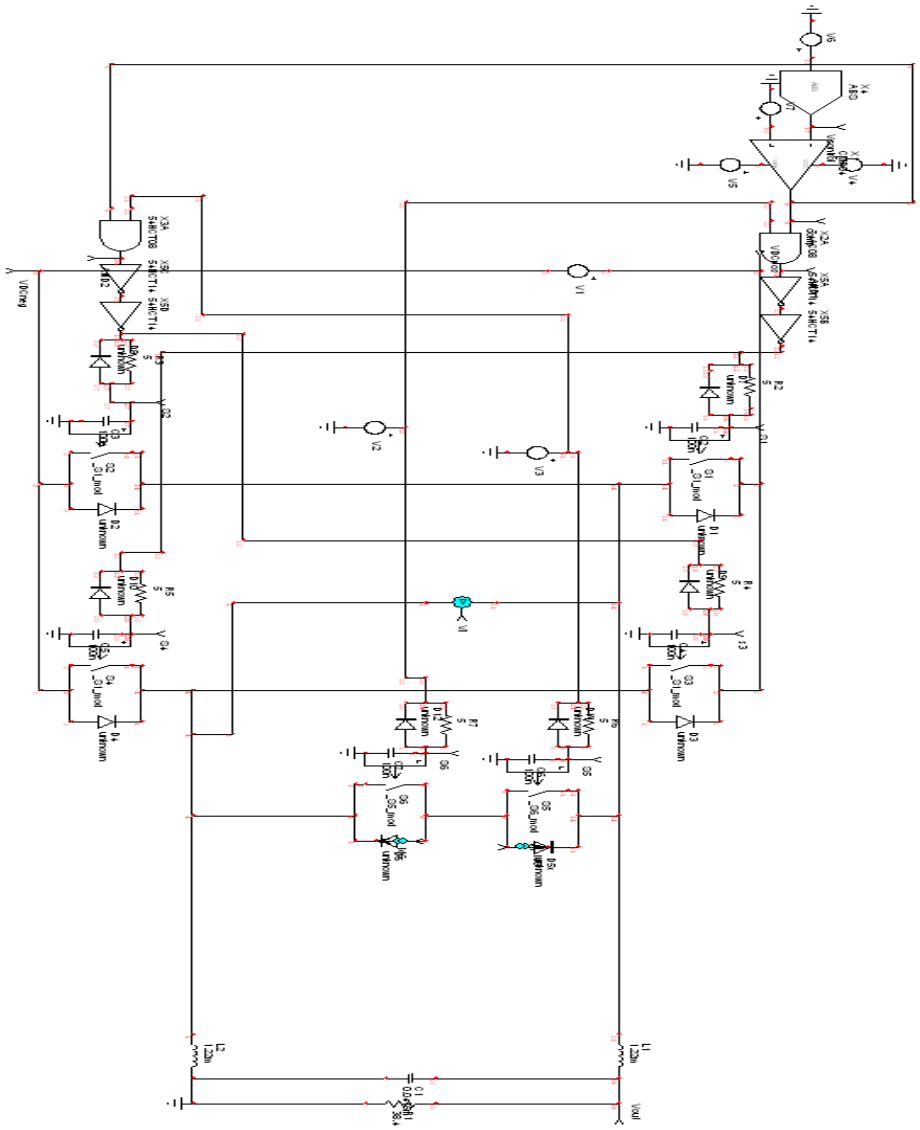

Figure 65: ICAP Model of HERIC Topology

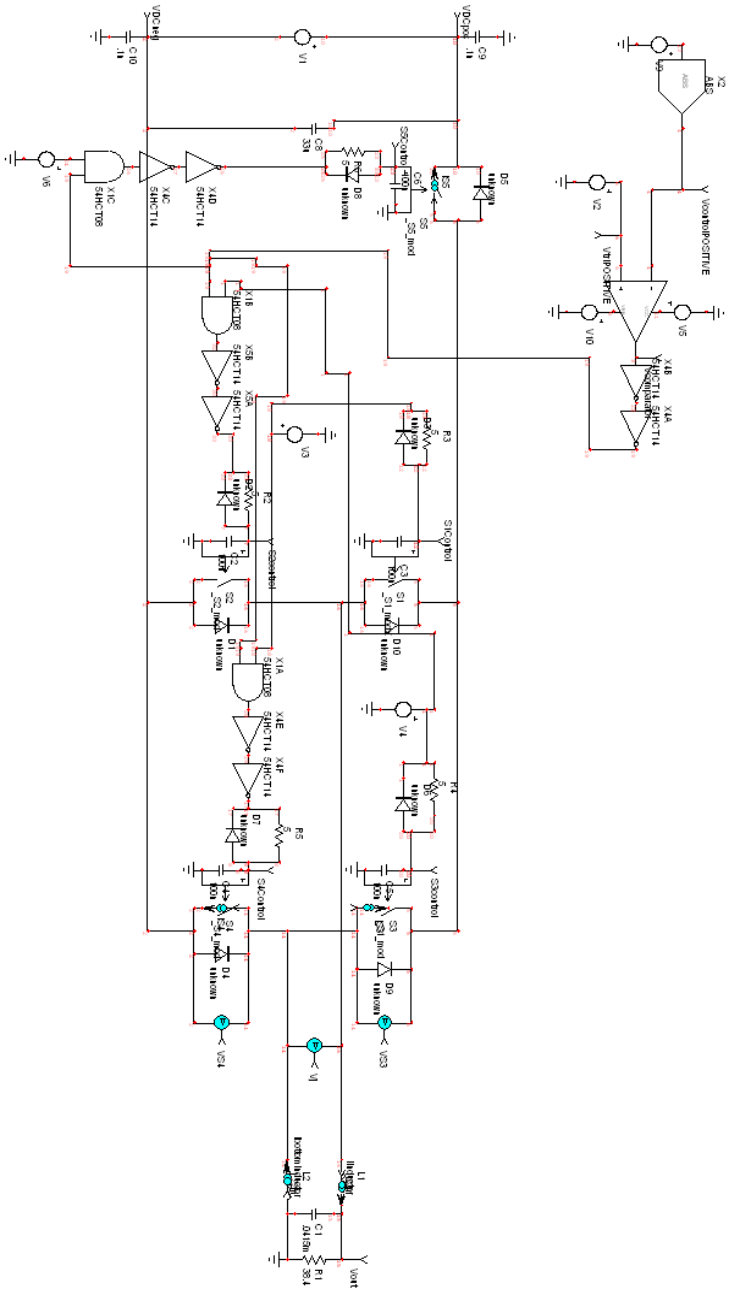

Figure 66: ICAP Model of H5 Topology

Appendix D: Additional Simulation Results

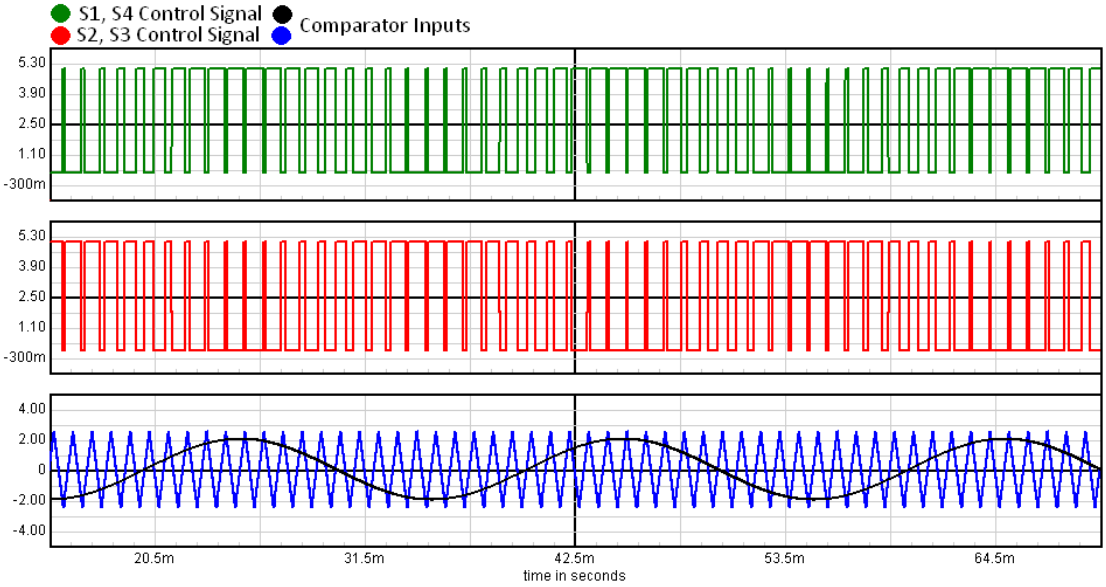

Figure 67: PWM control Signal for Switches of Fullbridge Topology Implementing a Bipolar Switching Scheme at a Switching Frequency of 1kHz

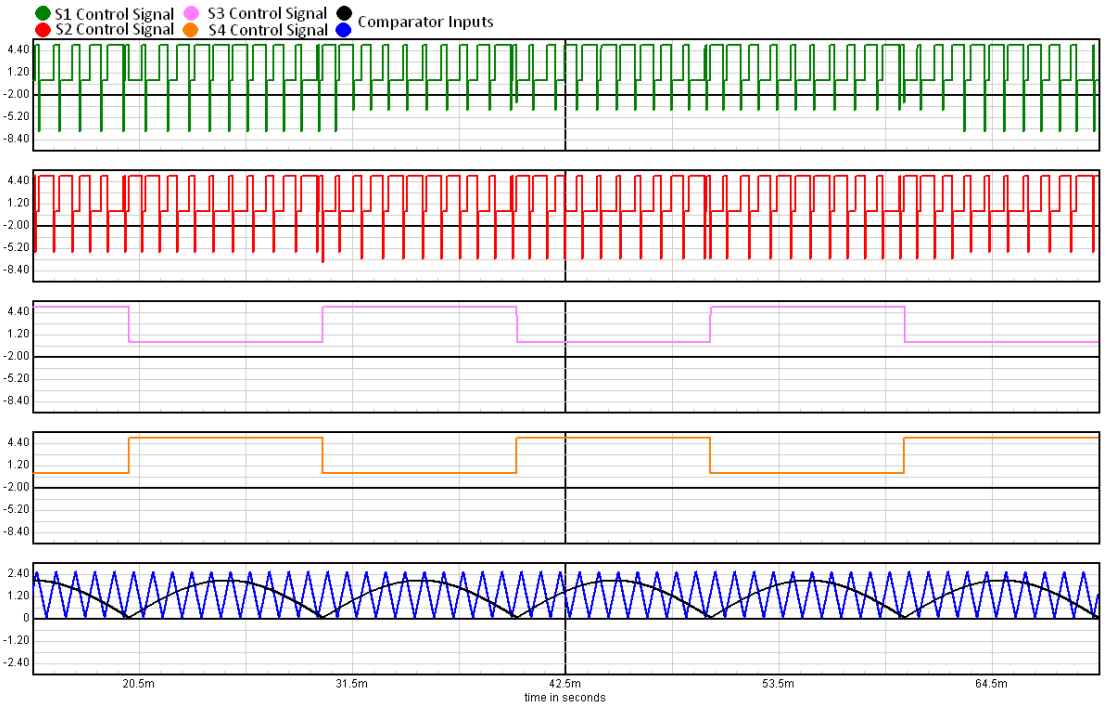

Figure 68: Control signals for a Fullbridge Topology Implementing a One Phase Chopping Unipolar Switching Scheme (Type B) at a Switching Frequency of 1 kHz

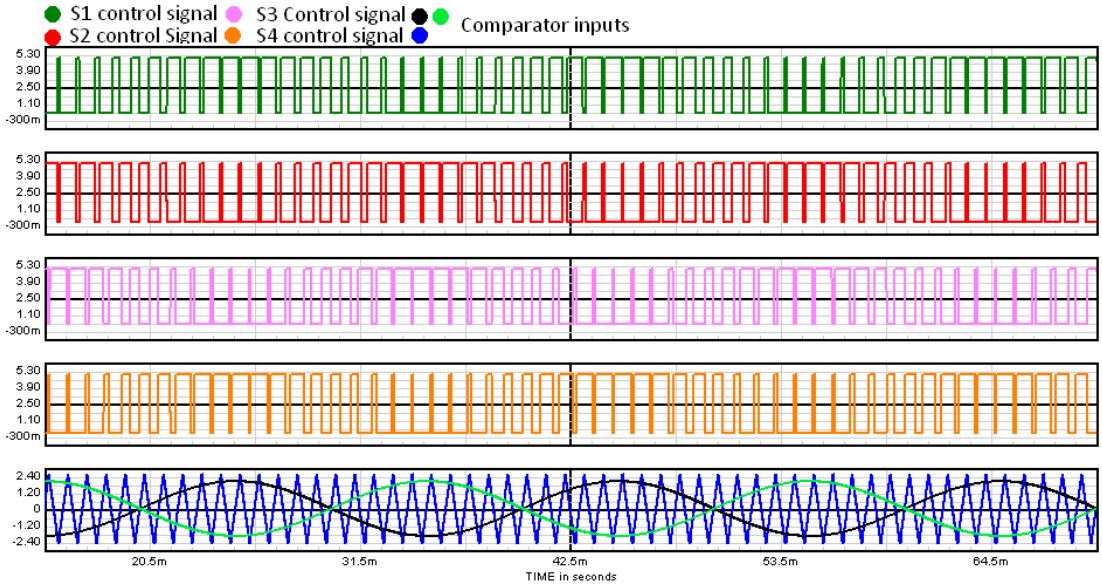

Figure 69: Control signals for a Fullbridge Topology Implementing a Unipolar Switching Scheme at a Switching Frequency of 1 kHz [19]

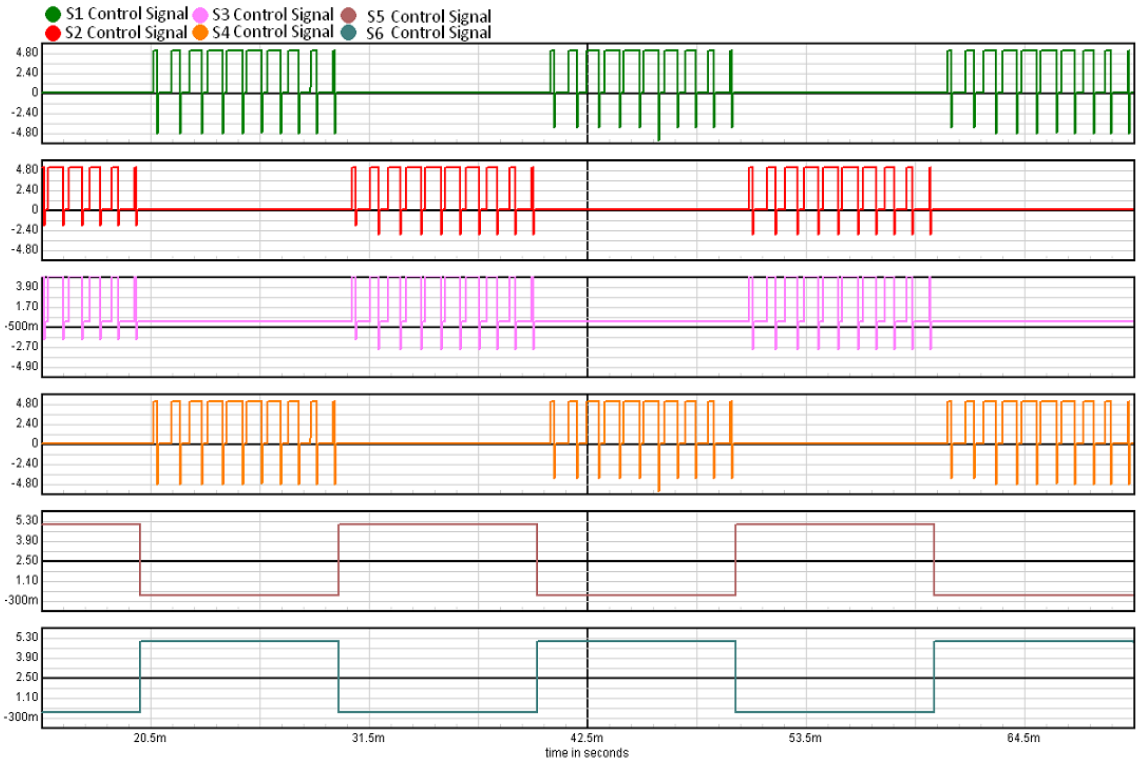

Figure 70: Control signals for a HERIC Topology Implementing at a Switching Frequency of 1 kHz

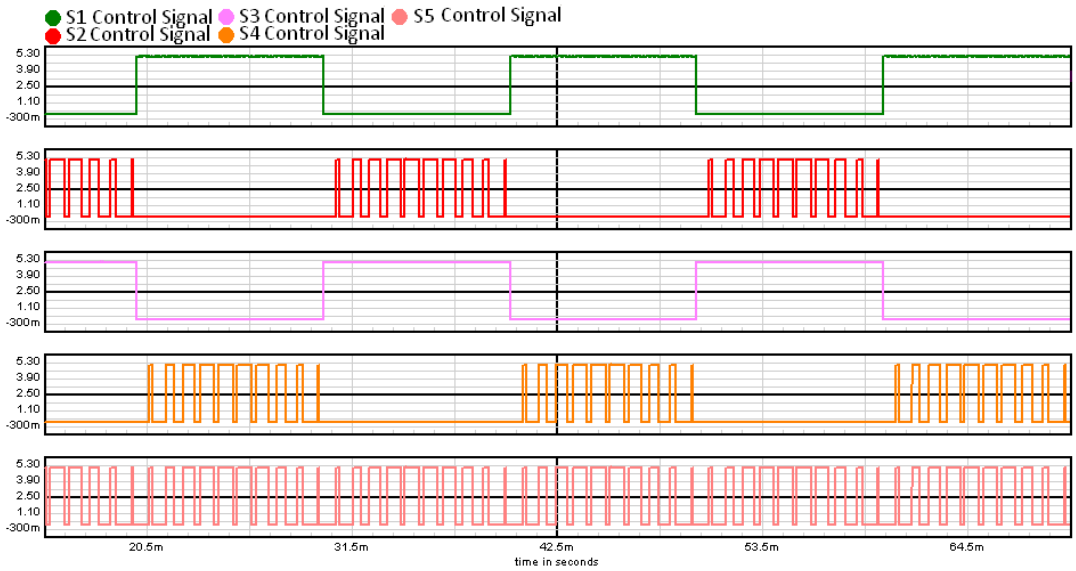

Figure 71: signals for a H5 Topology Implementing at a Switching Frequency of 1 kHz