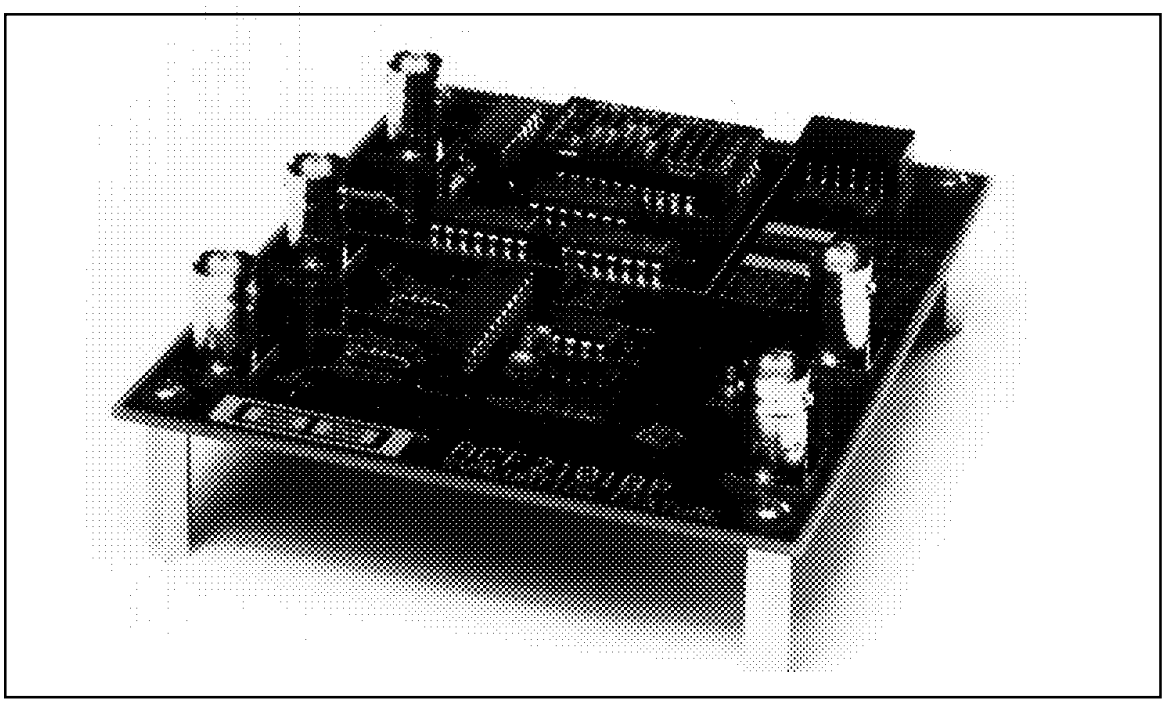
BURR-BROWN®

DEM-ACF2101BP
EVALUATION FIXTURE



FEATURES

- PROGRAMMABLE TIMING GENERATOR
- EXTERNAL INTEGRATION CAPACITOR OPTION
- FLEXIBLE INPUT FOR CURRENT OR VOLTAGE INPUTS
- OUTPUT BUFFER INCLUDED
- EXTERNAL OUTPUT HOLD CAPACITOR OPTION
- DUAL CHANNEL OPERATION

DESCRIPTION

The DEM-ACF2101BP is an evaluation fixture for the ACF2101BP dual, switched integrator. The board converts an input current to an output voltage using an ACF2101BP, with the switches of the ACF2101BP driven by a programmable timing generator.

As a complete circuit, the DEM-ACF2101BP makes it easy to do a quick evaluation of the ACF2101BP. The design and implementation of a programmable timing generator is included on the board as well as additional space for external capacitors and resistors.

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OVERVIEW

The DEM-ACF2101BP is an evaluation board designed for simultaneous operation of both channels of the ACF2101. Figure 1 illustrates the design of the board with a simplified block diagram. The user provides a positive current input signal, ±15V and +5V DC supplies, and a trigger signal ranging up to 20kHz. The ACF2101 output voltage is buffered by a unity gain op amp circuit. The trigger input controls the basic operational rate of the programmable timing generator circuit. The on-board, user controlled, timing generator provides control signals for the HOLD, RESET, and SELECT switches of the ACF2101.

Both channels of the ACF2101 are configured at the factory with a 1ms cycle time using the ACF2101's internal 100pF integration capacitor (C_{INT}). This cycle time and integration capacitor will provide a –10V output signal with an input current of 1µA.

The cycle time can be easily adjusted over a range of 50µs to 500ms by adjustment of the trigger frequency. An external capacitor can also be added to the board so that integration capacitor values larger than 100pF can be used if desired.

The on-board switch matrix allows the user to control the timing of the ACF2101 RESET, HOLD, and output SELECT switches. This board is configured at the factory for a recommended reset time of t_{PULSE} = 20µs.

The table below shows selected values of input current, cycle time, and integration capacitance needed to provide an output of –10V.

INPUT CURRENT	CYCLE TIME	INTEGRATION CAPACITANCE
0.01µA	100ms	100pF (internal)
0.1µA	10ms	100pF (internal)
1µA	1ms	100pF (internal)
10µA	100µs	100pF (internal)
10µA	1.1ms	1100pF (internal + external)
100µA	110µs	1100pF (internal + external)

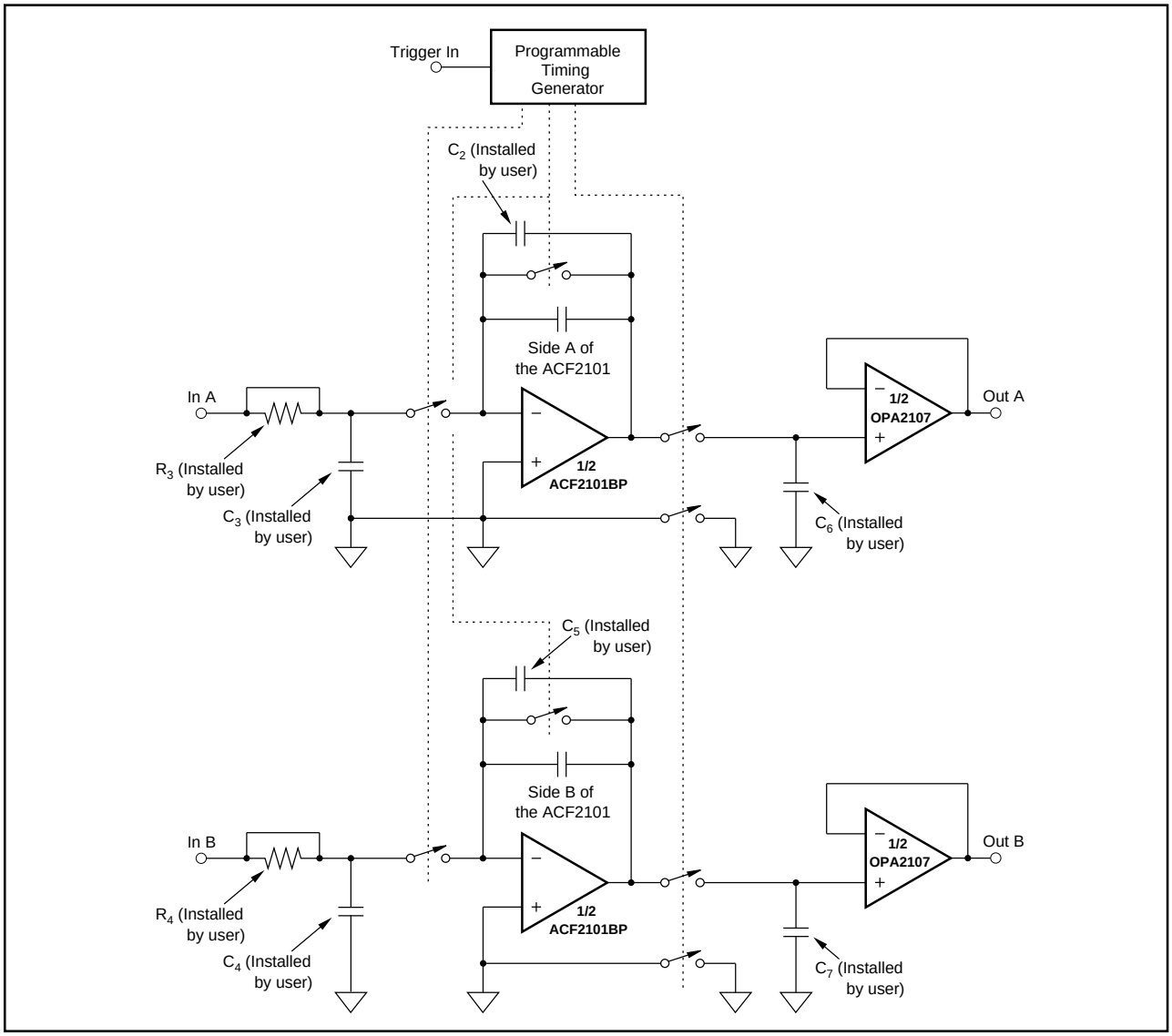


FIGURE 1. Simplified Block Diagram.

TECHNICAL DESCRIPTION

ACF2101BP Analog Circuit Configuration

The analog circuit (Figure 2) is designed for simultaneous two channel operation of the dual ACF2101. Both channels are configured at the factory for a 0 to 1µA input signal over a 1ms cycle time. This cycle time and input signal will provide a 0 to –10V output signal. A block diagram of 1/2 of the ACF2101 is shown in Figure 3. The transfer function of the ACF2101 can be calculated as:

$$\Delta V_{OUT} = -(i_{IN} \bullet \Delta t)/(C_{INT} + C_{EXT})$$

ΔV_{OUT} = the maximum output voltage (in volts)

C_{INT} = the integration capacitor on the chip (in farads)

C_{EXT} = the external capacitor, C_2 and C_5 (in farads)

i_{IN} = the input current (in amperes)

Δt = the cycle time (in seconds) see Figure 4

Note that C_{INT} can be used alone or in parallel with C_{EXT}. If an external integration capacitor is used it should have a low

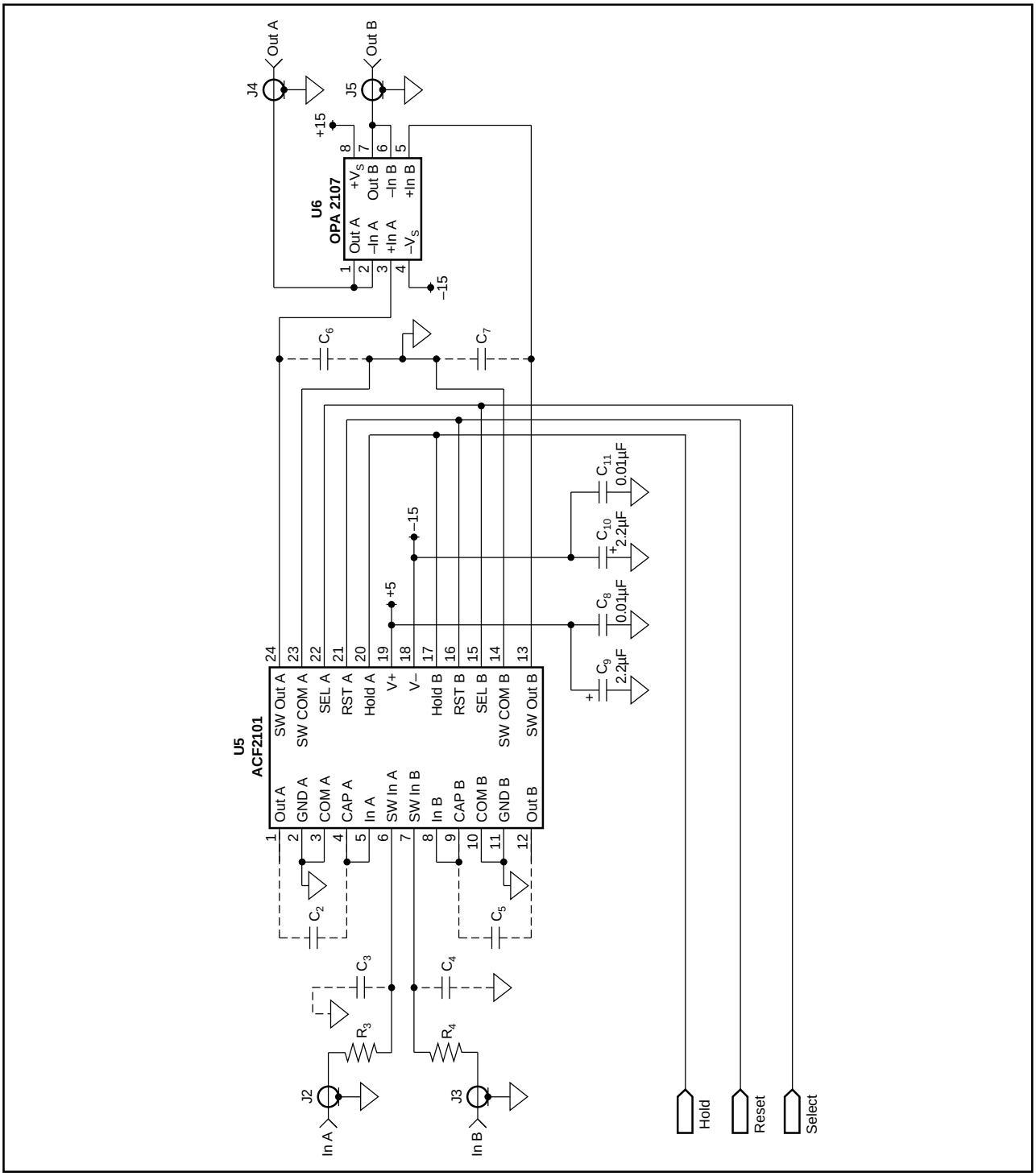


FIGURE 2. Analog Portion of DEM-ACF2101BP Evaluation Fixture.

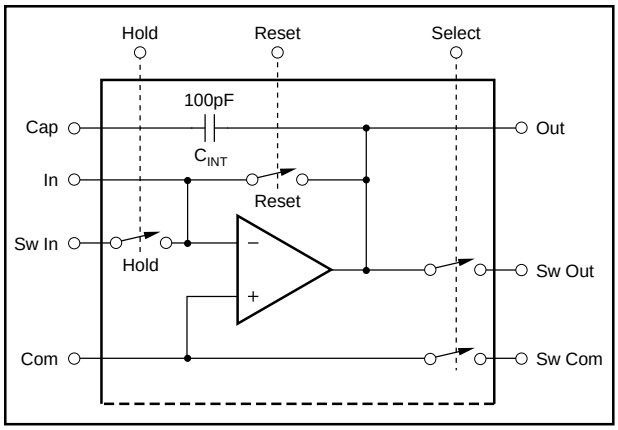
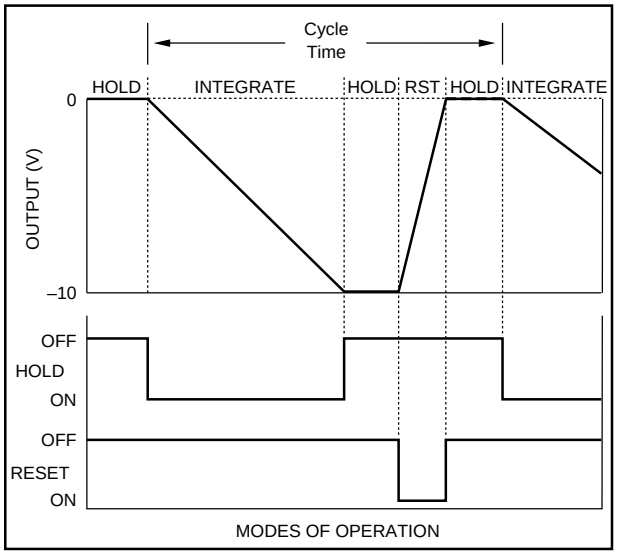


FIGURE 3. Block Diagram of 1/2 of the ACF2101BP.



SWITCH	MODE OF OPERATION		
	INTEGRATE	HOLD	RESET
Hold Switch	On	Off	On/Off
Reset Switch	Off	Off	On
On: Switch shorted; Logic 0 input. Off: Switch open; Logic 1 input.			

FIGURE 4. Modes of Operation of the ACF2101.

voltage coefficient, temperature coefficient, memory, and leakage current. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica. Space for an external integration capacitor (C_2 and C_5) is also provided on the board.

The SW OUT of both channels are connected to operational amplifiers configured as buffers (U6). A space for an output hold capacitor (C_6 and C_7) is provided on the board for each side of the dual ACF2101BP. An example of how C_6 and C_7 could be used with the help of the OPA2107 (U6) operational amplifier is shown in Figure 5. In Figure 5, the ACF2101BP is used as a programmable current to voltage converter. The output of the circuit, V_{OUT} is a dc level for a constant current input. Refer to the ACF2101 data sheet (PDS-1078) for a detailed discussion of this application.

By changing R_3 and R_4 from zero ohm (factory configured) jumpers to resistors, a voltage source can be integrated instead of a current source as shown in the schematic in Figure 6. C_3 and C_4 must be added to the circuit in this application to prevent the voltage at SW IN A and SW IN B from exceeding +0.5V when the HOLD switch is off (or open). If the voltage at SW IN A or SW IN B exceeds +0.5V, the protection circuitry will begin to conduct. This will not damage the ACF2101BP, but performance specifications will not be met. Selection of C_3 and C_4 is dependent on the time that the ACF2101BP is in the hold mode and the magnitude of i_{IN}.

$$C_3,\ C_4 \geq (t_{HOLD} \bullet i_{IN(max)}) / 0.5V$$

t_{HOLD} = time that the ACF2101BP is in the hold mode (seconds)

$i_{IN(MAX)}$ = maximum expected input current (amperes)

C_3, C_4 = capacitance (farads)

PROGRAMMABLE TIMING GENERATOR

The timing generator (Figure 7) provides the RESET, SELECT, and HOLD control signals for the operation of the ACF2101. This generator is a programmable state machine that consist of a decade counter and a few flip-flops. Each ACF2101 control signal has its own edge-triggered flip-flop.

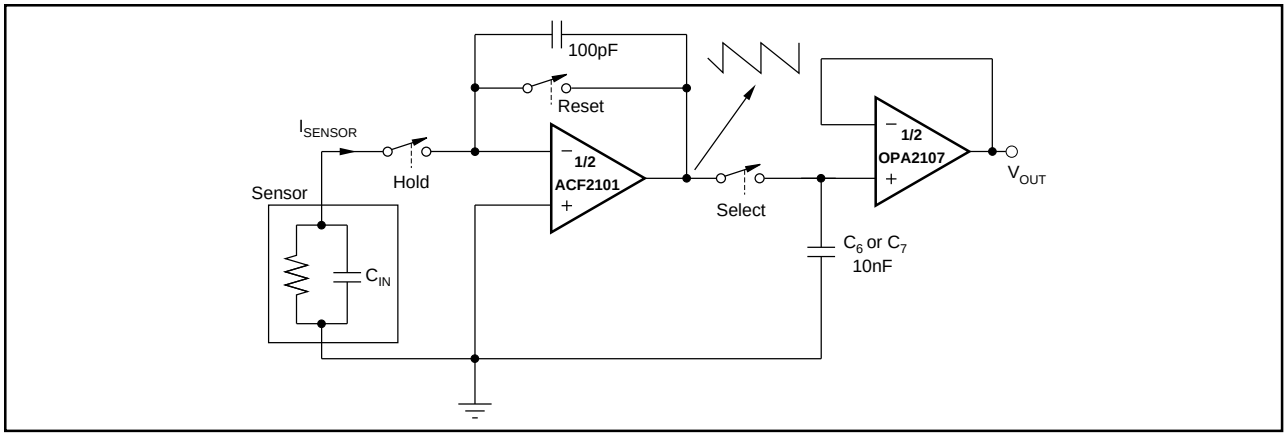


FIGURE 5. Block Diagram of a Programmable Current-to-Voltage Converter using the DEM-ACF2101BP Evaluation Fixture.

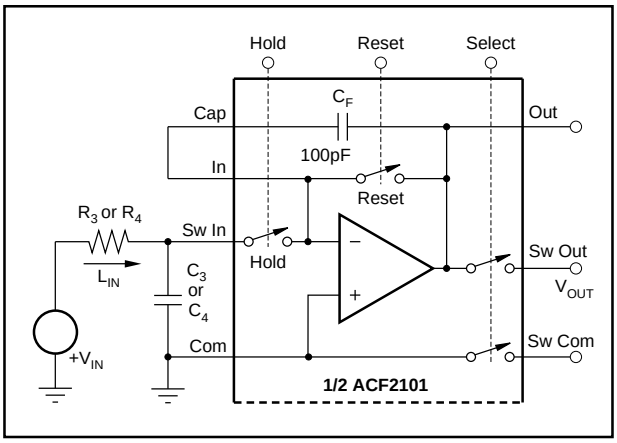


FIGURE 6. Block Diagram of Using the ACF2101BP with a Voltage Input Instead of a Current Input.

The outputs of the counter will change the state of the flip-flops depending on the settings of the matrix switches. The RESET, SELECT, and HOLD control signals are the same for both sides of the dual ACF2101BP. This is **not** a requirement for ACF2101 operation. The RESET, SELECT and HOLD control lines were hard-wired on this board to make it easier to use.

The rising edge of the trigger initiates the clocking sequence shown in Figure 8. After a delay the switching signals (row 1 through row 10) that will ultimately control the RESET, SELECT, and HOLD control pins begin. Each row follows the preceding row with a rising edge delay of t_{PULSE}. The pulse width, t_{PULSE}, is changed by adjusting the value of RV1 potentiometer on the board. The nominal range of t_{PULSE} is 6ns to 36µs. The trigger frequency ranges from 2Hz to 20kHz to give a range of cycle times from 500ms to 50µs.

All of the signals from the counter, U1, are connected to the rows of the switch matrix, SW1. The signals on the rows of SW1 can be switched into the columns by toggling the switches on the matrix. RESET is controlled by columns B and C. The rising edge of C initiates a logic low on the RESET pin, which closes the RESET switches on both sides of the dual ACF2101BP (U5). The rising edge of B initiates a logic high on the RESET pin, which opens the RESET switches of the ACF2101BP. SELECT is controlled by columns E and D. The rising edge of E initiates a logic low on the SELECT pin, which closes the SELECT switches on both sides of the dual ACF2101BP. The rising edge of D initiates a logic high on the SELECT pin, which opens the SELECT switches of the ACF2101BP. HOLD is controlled by columns G and F. A rising edge of G initiates a logic high on the HOLD pin, which opens the HOLD switches on both sides of the dual ACF2101BP. A rising edge of F initiates a logic low on the HOLD pin, which closes the HOLD switches of the ACF2101BP. The logic table is shown below.

SW1	CLOCK LOGIC EDGE	ACF2101 SWITCH AFFECTED	NEW ACF2101 SWITCH CONDITION
A	No Connect		
B	Rising Edge	RESET	OPEN
C	Rising Edge	RESET	CLOSED
D	Rising Edge	SELECT	OPEN
E	Rising Edge	SELECT	CLOSED
F	Rising Edge	HOLD	CLOSED
G	Rising Edge	HOLD	OPEN
H	No Connect		
J	No Connect		
K	No Connect		

Examples of switching arrangements for the DEM-ACF2101BP are shown in Figure 9.

FACTORY TIMING AND TEST CIRCUIT

The block diagram of the analog portion of the DEM-ACF2101BP and timing configuration used to test the board is shown in Figure 10. The setting of column A on SW1 determines the clock cycle of the counter, U1. Column A is set to Row 0 to give the longest clock cycle and the most programming flexibility. The REF102 is a 10V reference chip. Two 10MΩ resistors are used to generates two 1µA current sources, which sink into SW IN A and SW IN B of the ACF2101BP. C_3 and C_4 are used during test to prevent the hold switch input from exceeding 0.5V. The timing circuit is adjusted to a 20µs pulse width. Operation of the clock and the ACF2101 is verified.

LAYOUT CONSIDERATIONS

Care was taken in the layout of this board to ensure the best performance of the ACF2101BP. The inputs of the ACF2101BP are carefully guarded to prevent excess currents from being capacitively coupled into the summing junction of the ACF2101 amplifier. Since this is a four-layer board, we found that the power planes were critical in this case and had to be removed from the area.

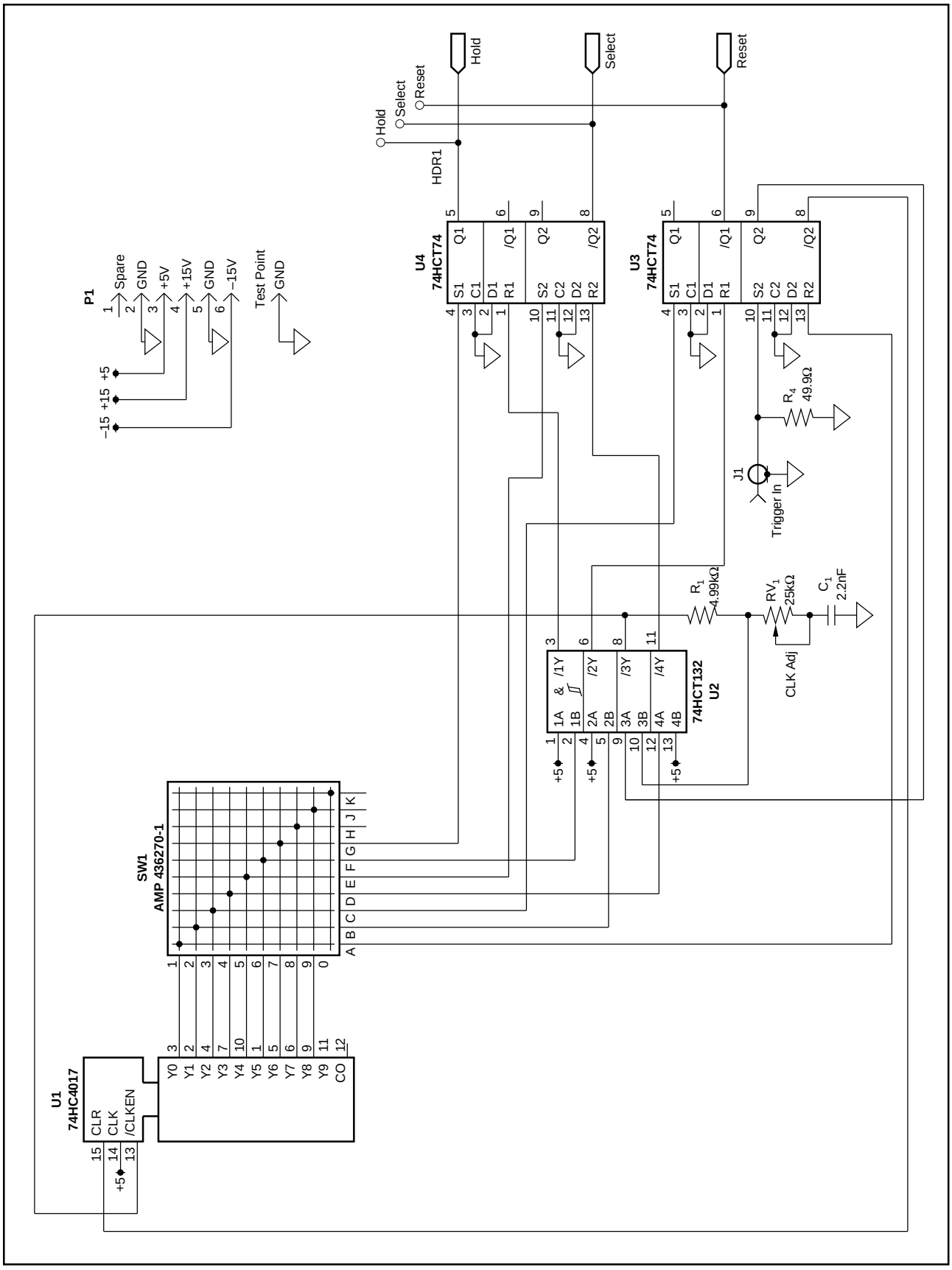
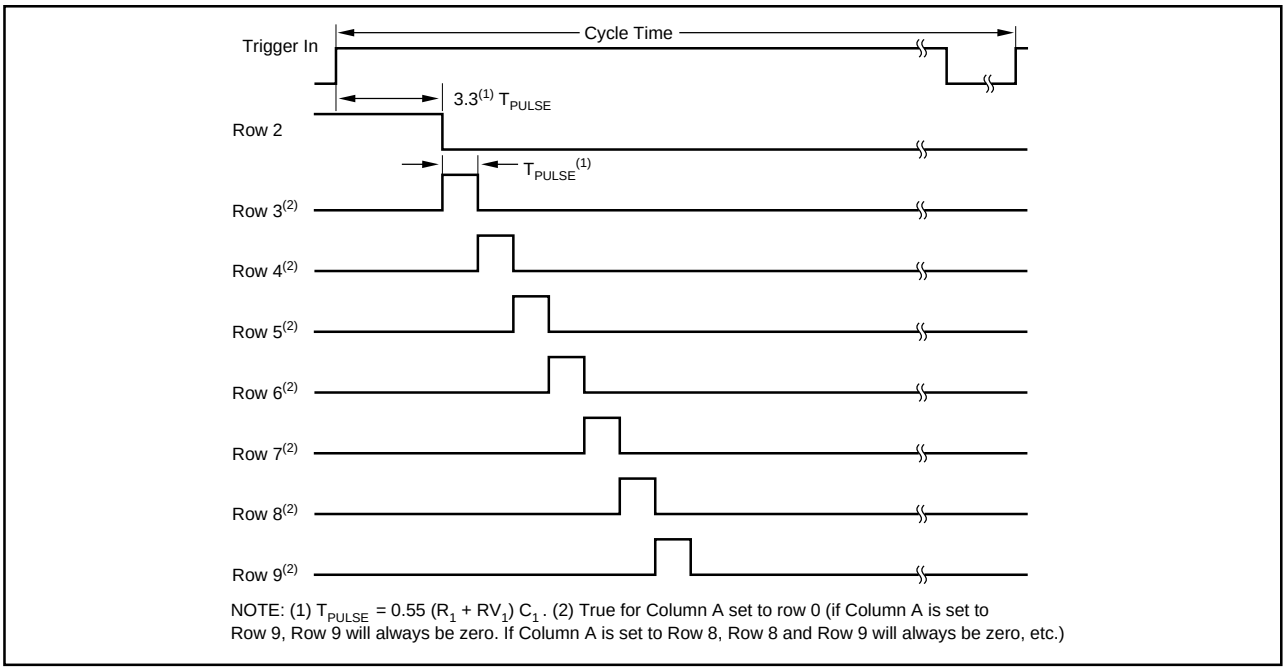
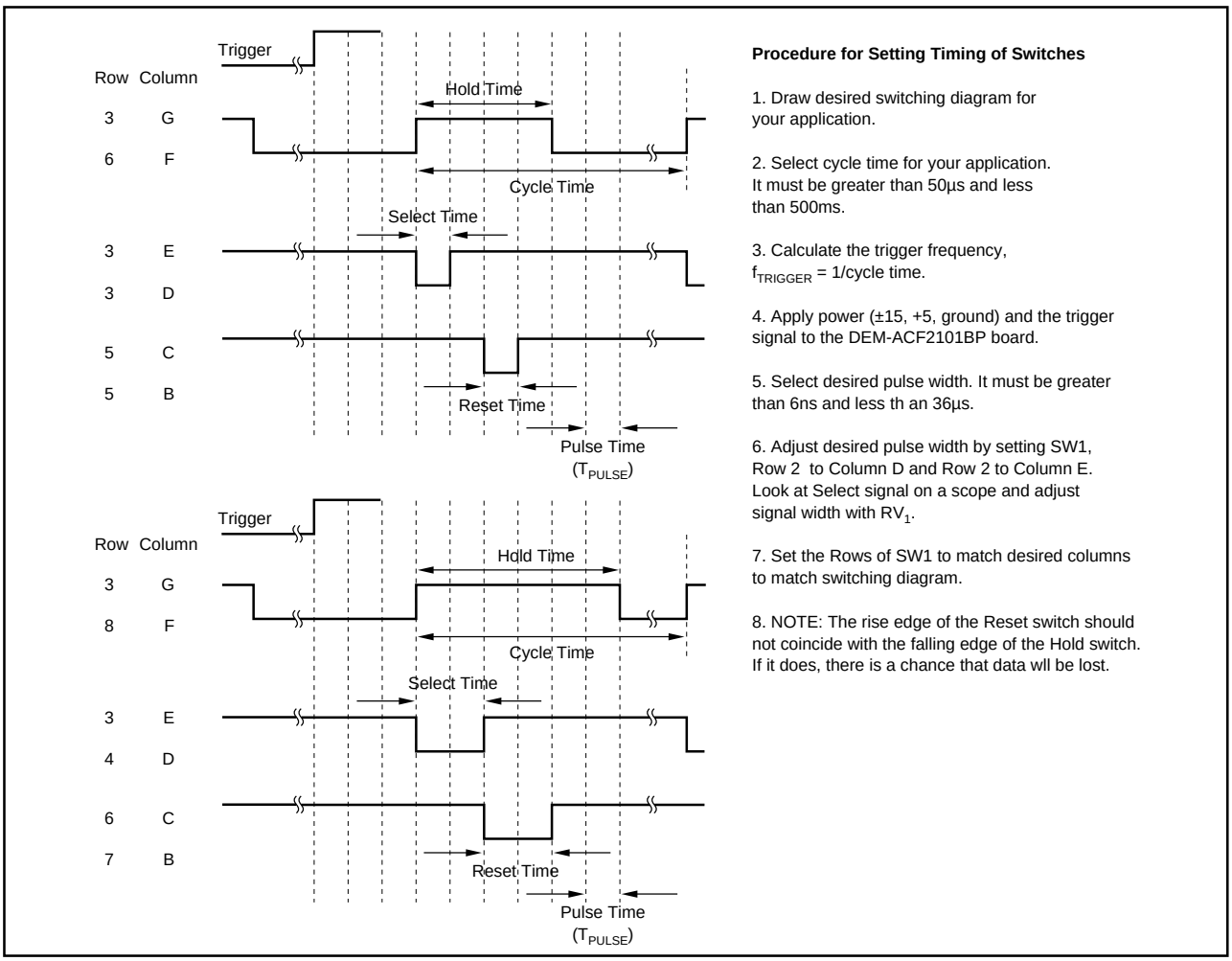


FIGURE 7. Programmable Timing Generator Portion of the DEM-ACF2101BP Evaluation Fixture.



NOTE: (1) T_{PULSE} = 0.55 (R_1 + RV_1) C_1 . (2) True for Column A set to row 0 (if Column A is set to Row 9, Row 9 will always be zero. If Column A is set to Row 8, Row 8 and Row 9 will always be zero, etc.)

FIGURE 8. Timing Sequence of the Rows of SW1 on the DEM-ACF2101BP Evaluation Fixture.



Procedure for Setting Timing of Switches

1. Draw desired switching diagram for your application.

2. Select cycle time for your application. It must be greater than 50µs and less than 500ms.

3. Calculate the trigger frequency, $f_{TRIGGER}$ = 1/cycle time.

4. Apply power (±15, +5, ground) and the trigger signal to the DEM-ACF2101BP board.

5. Select desired pulse width. It must be greater than 6ns and less th an 36µs.

6. Adjust desired pulse width by setting SW1, Row 2 to Column D and Row 2 to Column E. Look at Select signal on a scope and adjust signal width with RV_1.

7. Set the Rows of SW1 to match desired columns to match switching diagram.

8. NOTE: The rise edge of the Reset switch should not coincide with the falling edge of the Hold switch. If it does, there is a chance that data wll be lost.

FIGURE 9. Examples of Switch Settings and Procedure for Setting the Timing of the Switches for the DEM-ACF2101BP Evaluation Fixture.

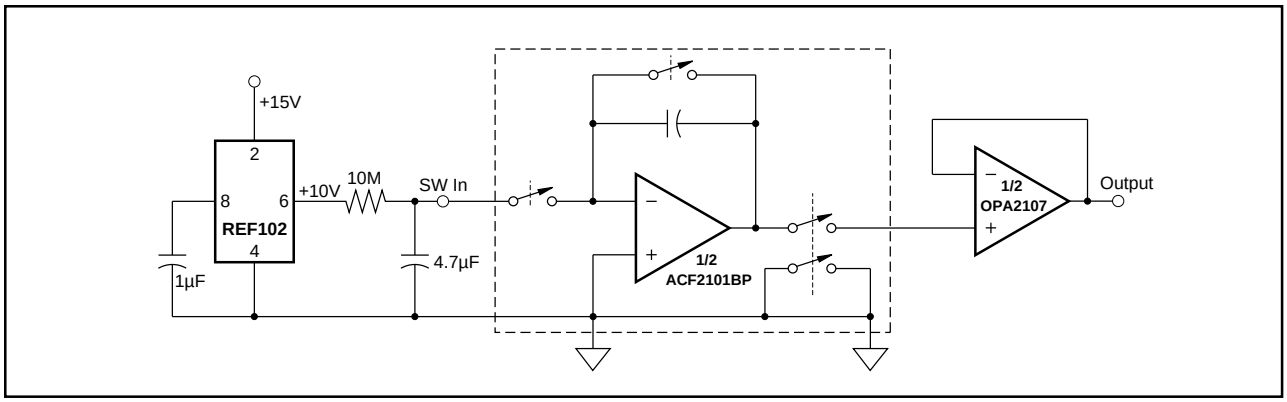


FIGURE 10a. Factory Test Circuit for the DEM-ACF2101BP.

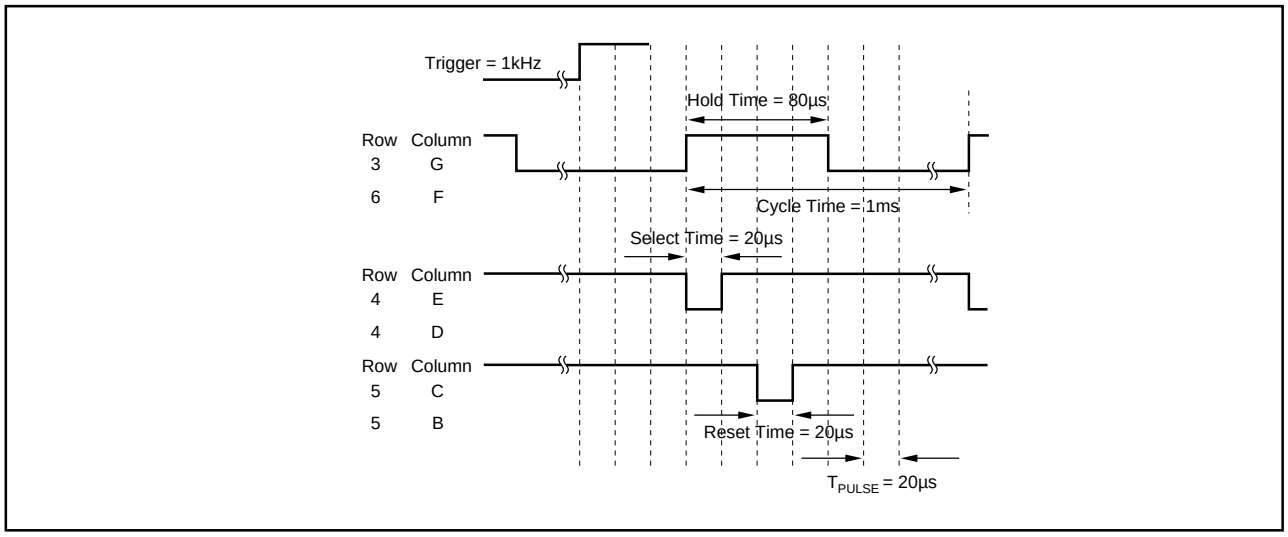


FIGURE 10b. Timing Configuration for the Factory Test of DEM-ACF2101BP.

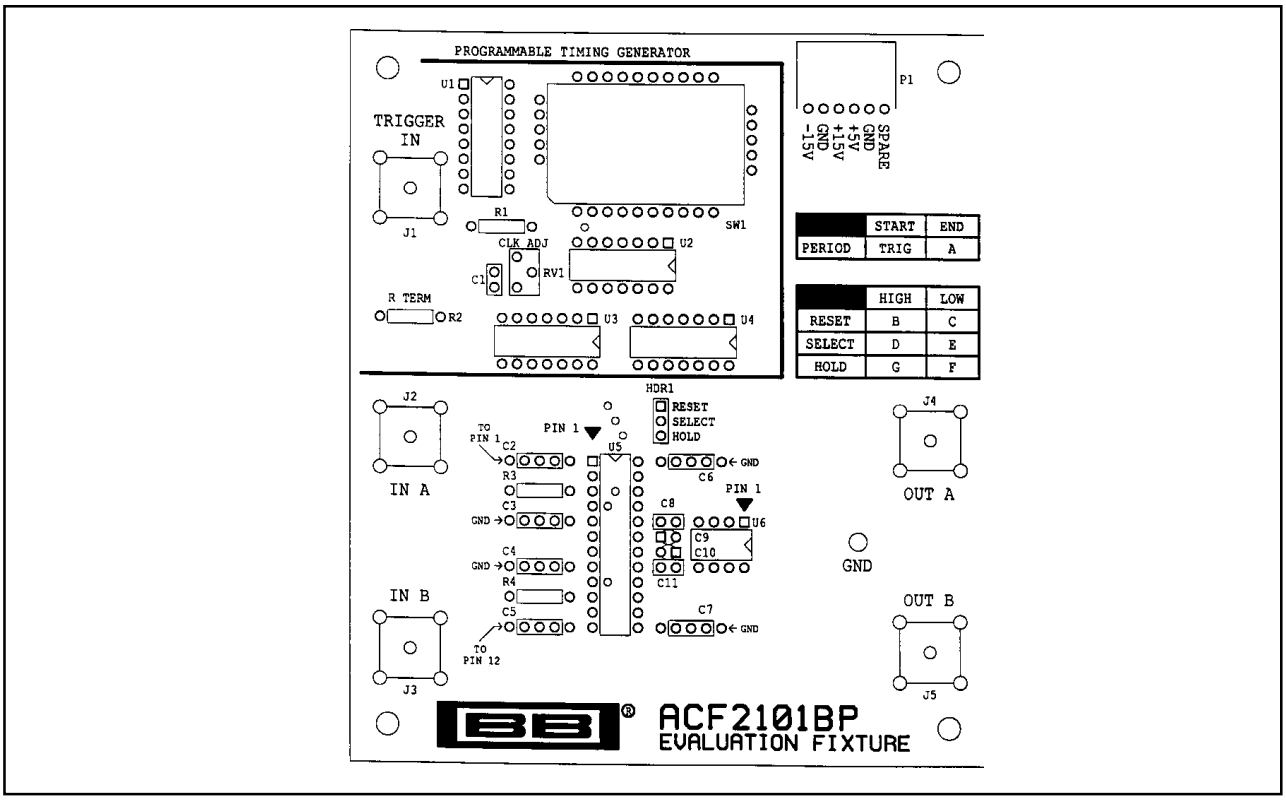


FIGURE 11. Silk Screen.

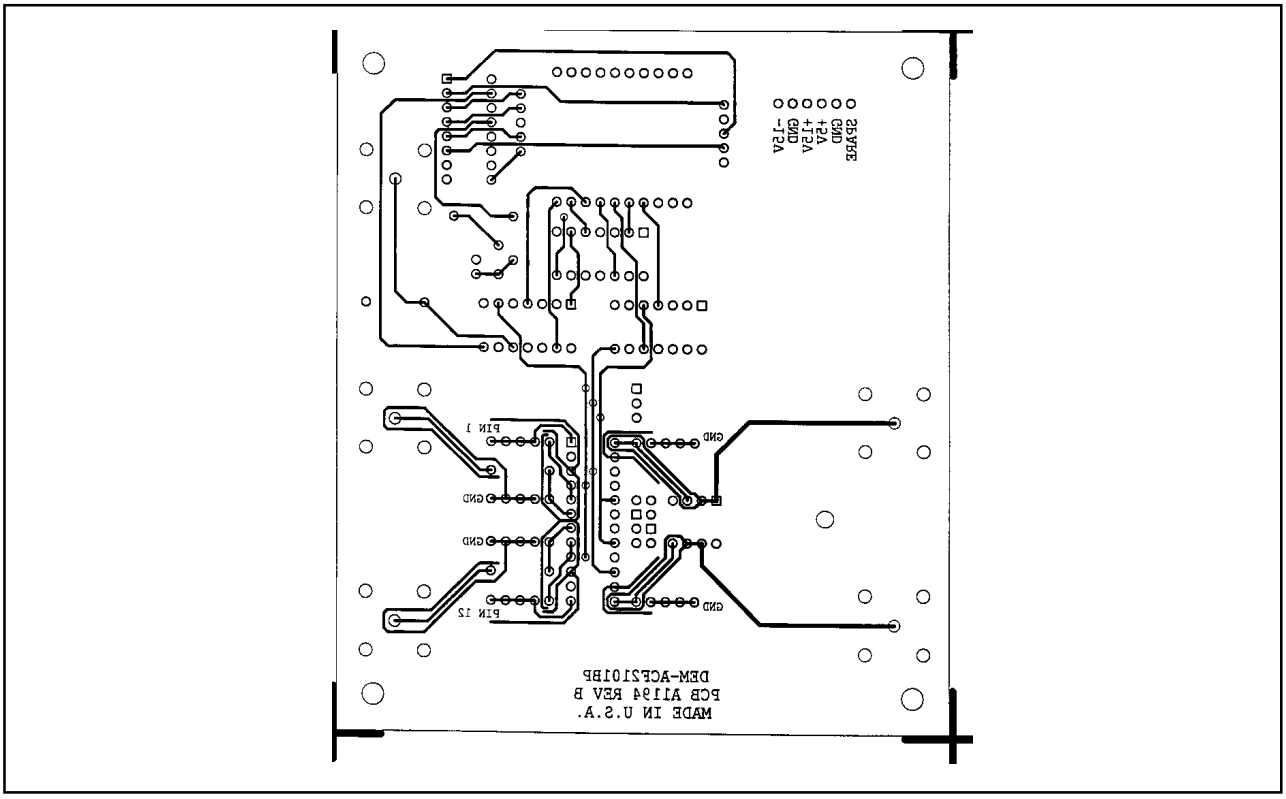


FIGURE 12. Solder Side.

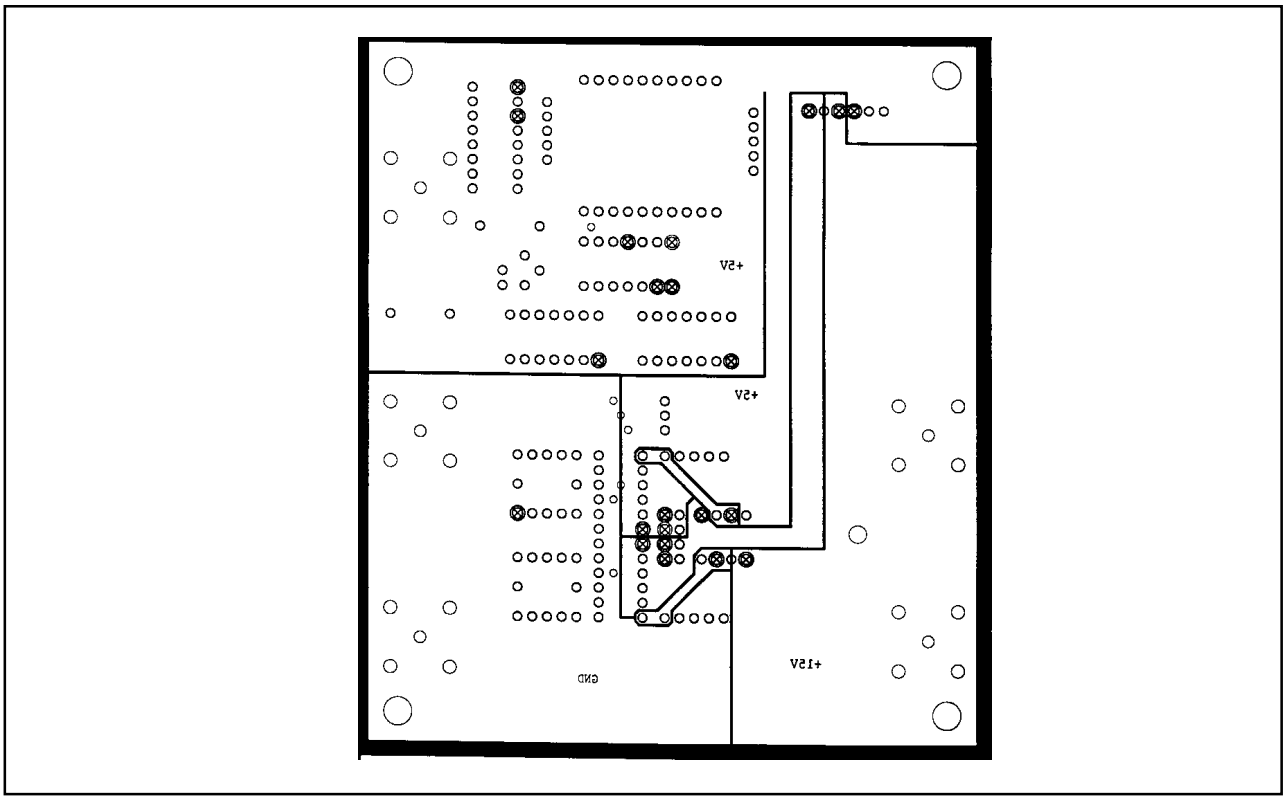


FIGURE 13. Power Plane.

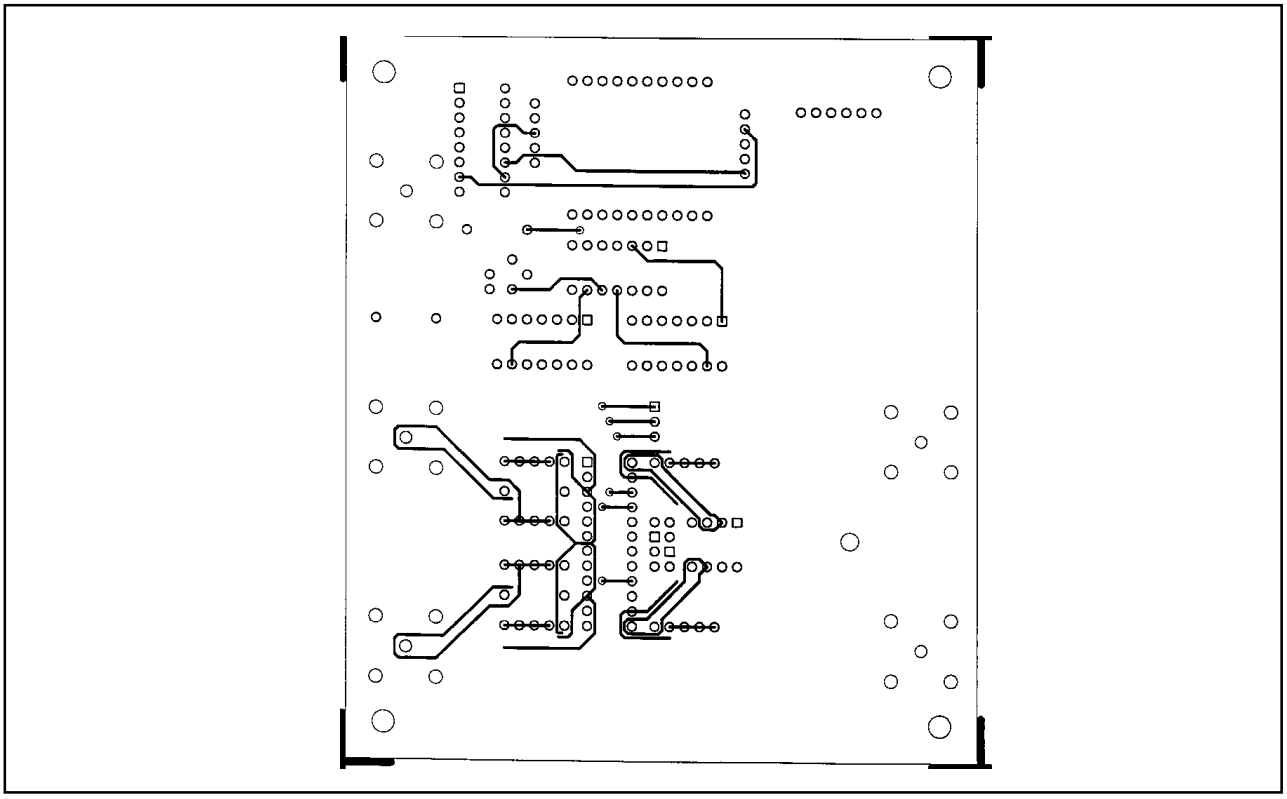


FIGURE 14. Component Side.

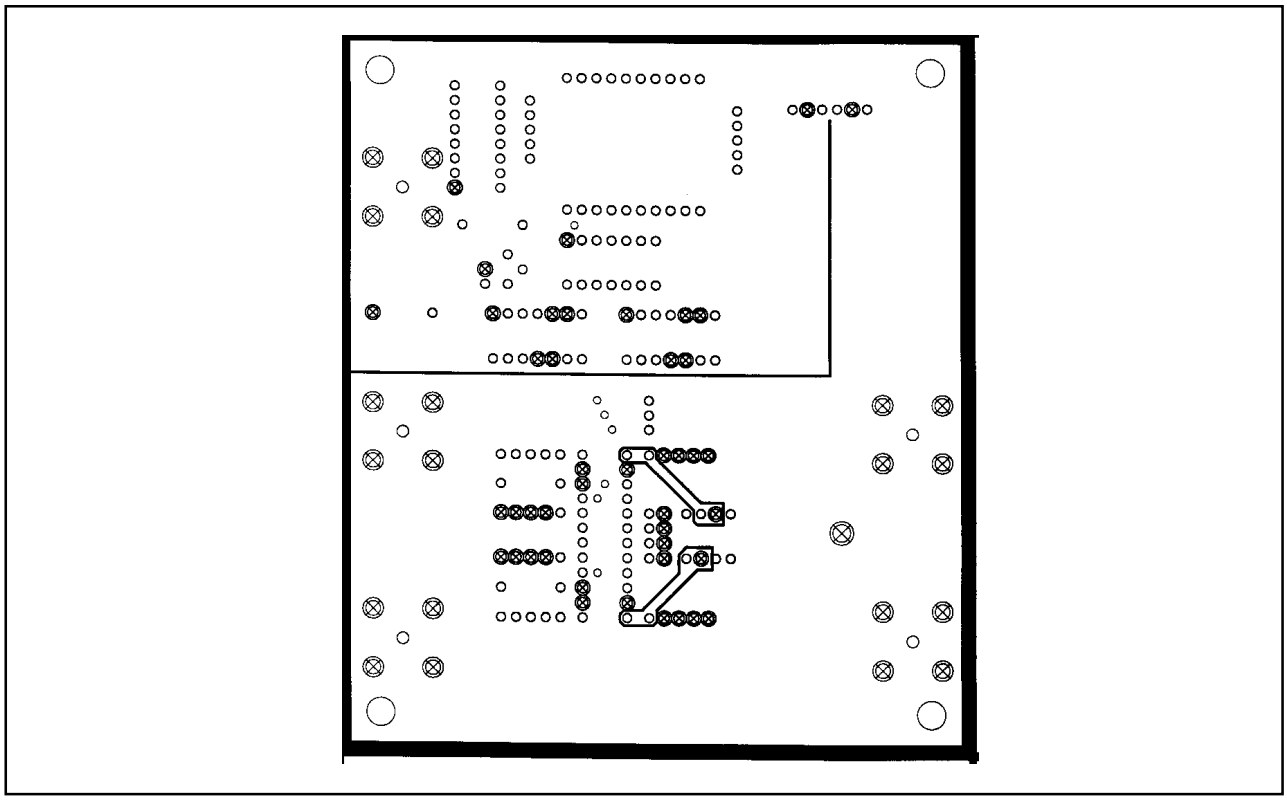


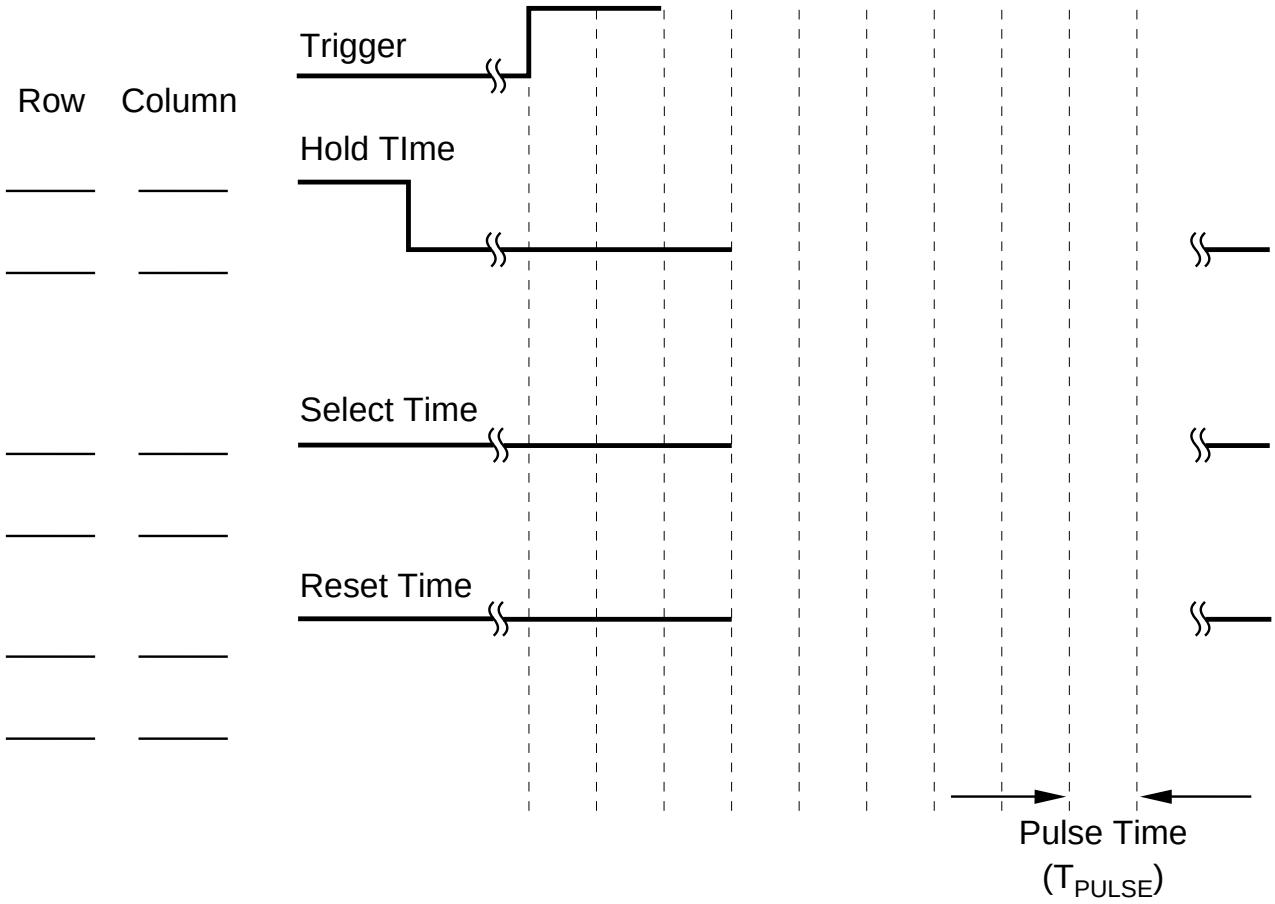
FIGURE 15. Ground Plane.

DEM-ACF2101BP PARTS LIST

QTY	PART NO.	REF DES	MANUFACTURER	DESCRIPTION	CROSS P/N	MFG
1	74HC4017	U1	Any	Decade Counter		
1	74HCT132	U2	Signetics	Quad Nand Schmitt Trigger		
2	74HCT74	U3, U4	Signetics	Flip-Flop		
1	ACF2101BP	U5	Burr-Brown	Dual Switched Integrator	N/A (1)	
1	OPA2107	U6	Burr-Brown	Dual FET Op Amp	N/A (1)	
1	824-AG31D	(U5)	Augat	24 Pin DIP 0.3 GLD/TIN	Must match specs	
1	808-AG11D	(U6)	Augat	8 Pin DIP 0.3 GLD/TIN	Must match specs	
1	4362701	SW1	Amp	10 X 10 Matrix SW	N/A (1)	
Resistors						
1	RJ26FW253	RV1	Bourns	25k Trimmer	RJRFW253 (2)	Bourns
1	RN55D4991F	R1	Dale	4.99k 1/4W 1%	N/A (1)	
2	FRJ-50	R2, R3	Philips	0 Jumper Resistor	N/A (1)	
1	RN55D49R9F	R4	Dale	49.9 1/4W 1%	N/A (1)	
Capacitors						
1	C320C222J1G5CA	C1	Kemet	2200pF 50V-200V 5% 0.1" LS	Must match specs	
2	C320C103K2R5CA	C8, C9	Kemet	0.1µF CERC RAD 0.1" LS 10%	Must match specs	
2	ECS-F1EE225K	C10, C11	Panasonic	2.2µF TANT 25V 10%	N/A (1)	
Mechanical						
5	KC-79-274-M06	J1, J2, J3, J4, J5	Kings	PCB MNT BNC	N/A (1)	
1	102203-3	P1	Amp	Pwr in Connector	N/A (1)	
1	TWS-103-07-G-S	HDR1	Samtec	3 Pin STRT HDR GLD/GLD	Must match specs	
1	2308-2-00-01-00-00-07-0	GND	Mil Max	Turret Terminal	N/A (1)	
1	678164	N/A	Precision WW	Input Pwr Cable	N/A (1)	
4	312-6473-032	N/A	EF Johnson	1" Standoffs 4-40	1450E (2)	Keystone
4		N/A	HMS	1/4-1/2" 4-40 Pan Hd Scws		

NOTE: (1) All parts with N/A in cross P/N column are not to be crossed. (2) If a part number appears in cross P/N column part can only be crossed to that alternate.

WORKSHEET


Row
Column
Trigger
Hold TIme
Select Time
Reset Time
Pulse Time
(T_{PULSE})