2.0 Specification

Section 2

4070 FAMILY SPECIFICATION

(Unless stated, the specification of the 4072 and 4074 are identical)

VERTICAL INPUT

Input

4072 - 2-Channels BNC connectors
4074 - 4-Channels BNC connectors

Bandwidth

DC: 0 – 100MHz (-3dB)
AC: 4Hz – 100MHz (-3dB)

Bandwidth Limit

20MHz (-3dB)

Sensitivity

2mV/div to 5V/div in 1-2-5 sequence.

Accuracy

±3% of full scale

Variable Sensitivity

2.5:1 range allowing continuous adjustment of sensitivity between ranges.

Input Impedance

1MΩ/20pF

Input Coupling

AC-DC-GND

Input Protection

400VDC or pk AC

Vertical Position Range

±8 div

Auto Scale Factors

Probe tip attenuation factors for x1, x10 or x100 probes are sensed by the oscilloscope, providing the probes have a suitable sensing element.

DISPLAY

CRT

10 x 12cm rectangular. Internal illuminated graticule with 10 x 8 divisions and 5 sub-divisions. Continuously variable illumination.

Display Modes

4072:

CH1, CH2, CH1 invert, CH2 invert.
CH1 + CH2, CH1 vs CH2, Reference Traces 1 through 8 (To a maximum of 8 displayed traces)

4074:

CH1, CH2, CH3, CH4, CH1 invert, CH2 invert, CH3 invert, CH4 invert, CH1 ±CH2, CH3 ± CH4, Reference Traces 1 through 8. (To a maximum of 8 displayed traces.)

Interpolation

Selectable either sine, linear or no interpolation

Screen Update Rate

Approximately 30 traces per sec

Trigger Reference

There is an on-screen indicator which shows the location of the trigger level and the trigger point

Readout

Readout characters indicate the current setting of the instrument: vertical sensitivity, timebase and cursor measurements

ACQUISITION SYSTEM

Maximum Single Event Useful Storage Bandwidth

100MHz (using internal sine interpolator)

Maximum Sample Rate

400M samples/sec on each input channel at 250ns/div timebase range decreasing with timebase range to 5 samples/sec at 20s/div.

Vertical Resolution

8-Bits (0.4%)

Record Length

1K word per input channel

ACQUISITION MODES

Refresh Mode

For stored data and display updated by trigger event.

Roll Mode

Stored data and display updated continually prior to being frozen by trigger

Pre-trigger Roll Mode

The stored data is updated continually as per the roll mode in the pre-trigger part of the display. Then the entire display is frozen as in the refresh mode upon receipt of a trigger.

Glitch Capture

Capture of either positive, negative or alternate positive and negative glitches. Typically a 5ns pulse can be captured with 80% confidence. There is a 100% confidence of capture to 95% of amplitude for a 30ns pulse.
Note: Glitch capture only operates on timebase ranges from 5μs/div. to 20s/div.

Averaging

Averaging factor is available from 2 to 256 (in a binary sequence)

NON-VOLATILE MEMORY

Waveforms

A total of 8 waveforms can be stored: any trace can be recalled to the display

Set-Ups

A total of 4 set-ups can be stored in non-volatile memory.

Retention Time

The memory is trickle charged and will last approximately 3 months with the power disconnected.

Specification

Section 2

HORIZONTAL DEFLECTION

Horizontal Display Modes
A, A alt B with A intensified by B, B only, X-Y, Refresh, Roll, Pre-Trigger Roll.

Horizontal Display Accuracy
±3%.

A and B Delayed Sweep Range
20ns/div to 20s/div in 1-2-5 sequence. Sweep speeds faster than 250ns/div use equivalent time sampling (ETS). ETS uses random sampling to achieve pre-trigger.

Horizontal Expansion
The Expansion from x2 to x20 times (in a 1-2-5 sequence) is available on all timebase ranges (except x2 to x10 on 20ns/div). This gives a fastest timebase rate of 2ns/div.

Timebase Sample Accuracy
±0.01%.

Timebase Resolution
±0.1% of Timebase range

Timebase Jitter
Less than ±200ps

Trigger Jitter
Less than ±500ps.

Trigger Delay
The A or B sweep start can be delayed from either Trigger A or Trigger B respectively. The delay can be either negative (pre-trigger), or positive (post-trigger).

Trigger Range
Pre-Trigger -0 to 100% with 0.1% resolution.
Post Trigger –

TIMEBASE RANGE	MAX DELAY
20s to 0.1ms/div	99.9s
50μs to 50ns/div	0.99s
20ns/div	0.4s

Trigger Delay Accuracy
±0.001% delay
±0.1% of timebase range
±1ns

Delay by Events
This will allow the B sweep to be delayed from the A sweep by up to 999,999 events with a maximum trigger frequency of 100MHz

TRIGGER

There are two trigger systems, A and B. Each system has similar specifications.

Trigger A:

Source
4072: CH1, CH2, EXT A. LINE,
4074: CH1, CH3, EXT A, LINE.

Couplings
AC, DC, ACHP, ACLP, DCLP.
TV Line, TV Field 2.
DCLP, ACLP -(‹15kHz)
ACHP -(›15kHz).

Trigger B

Source
As Trigger A except use EXT B.

Couplings
As Trigger A. TV Line taken from A Source.

Slope
Selectable +ve, −ve

Sensitivity

Internal:	DC-10MHz	‹0.3 div.
	10MHz-100MHz	‹1.0 div.
External:	DC-10MHz	‹ 50mV p-p (x10)
		‹500mV p-p (x1)
	10MHz-100MHz	‹100mV p-p (x10)
		‹1V p-p (x1)

Trigger Level
Variable over greater than ±4 divisions.
Level indicated on screen with marker.

External Input Impedance
1MΩ/20pF

External Input Protection
200V DC or pk AC

Trigger Combinations
A and B Timebase can be triggered independently or in any combination of the following:

'A' Trigger only
Trigger after every Nth A event
Triggered on B after every Nth A event
'B' Trigger only
'A' Trigger then after N x 'B' trigger events

CURSOR MEASUREMENTS

There is an on-screen measurement cursor which can be allocated to any trace plus horizontal and vertical datum cursors which can be moved to any screen position.

The voltage and time differences between the measurement and datum cursors are automatically displayed.

Time Accuracy
As horizontal specification ± sample interval

Voltage Accuracy
As vertical specification ± 1 least significant digit (LSD)

IEEE-488 INTERFACE

Read and Write Functions
All front panel controls are fully programmable, except:
Trace Intensity Power on/off
Alpha-Numeric Intensity
Scale Illumination

Trace Rotation
EXT A and EXT B, x1/x10 switches

Data can be read from and written to all of the memories. All on-screen alpha-numerics can be read remotely. The controller can display messages on the display in 16 lines of 32 characters each.

Recognised Controller Originated Bus Commands

DCL	Returns Intrument to idle state.
SPE	Enables serial poll.
SPD	Disables serial poll.
GTL	Returns control to front panel switches.
SDC	As DCL but only affects devices configured to listen
IFC	Clears the interface.

IEEE-488 Formal Attributes

SH1	Source Handshake	Complete
AH1	Acceptor Handshake	Complete
TE2	Talker Function	Basic Extended Talker/Listener
LE2	Listener Function	Serial poll
SR1	Service Request	Complete
RL1	Remote/Local Function	Complete
PP0	Parallel Poll	None
DC1	Device Clear	Complete
DT0	Device Trigger	Complete

Operating Modes
Addressable from bus
Talk only in Plot mode

Primary Address:
Selectable from Menu 7.

Data Format
BCD, Octal, Hex, Binary.

Transfer Rate
Approximately 5K bytes/sec in binary mode

RS-423 (RS-232) INTERFACE

Specification
All of the functions available via the IEEE-488 interface are available via the RS-423 interface

Baud Rate
50,110,300,600,1200,2400,4800,9600
selectable via menu.

DIGITAL PLOTTER INTERFACE

The instrument can directly address HPGL format plotters via either the IEEE-488 or RS-423 interface. This plots out either menus or traces. The trace plots will include cursor information, range settings, date and time.

Manual Plot
Plotting of all displayed traces or menus initiated by front panel button

Automatic Plot
On-screen traces are automatically plotted after acquisition prior to automatic re-arming of the trigger system

Color
Different colors are selected for traces and the grid when multicolor plotters are used

Date and Time
This can be set to any value and the plotter then prints the time of signal acquisition

INTERNAL PLOTTER

Direct digital plots to the internal multicolor plotter can be selected by the menu to be in the same format as above.

Plot size
89mm wide by 102mm long (approx)

No. of Pens
4 (disposable roller-ball type)

Speeds
50s per trace (approx)

ANALOG PLOTTER OUTPUT

Analog Dual

4072
Simultaneous output of X with Y1 and Y2 outputs

4074
As 4072 followed by output of X with Y3 and Y4 outputs.

Analog Single
4072: Individual plot of single Y channel plus X output (allowing 2 channels to be plotted sequentially from the socket)
4074: As 4072, but all 4 channels plotted sequentially.

Plot Rate
0.05, 0.5 or 5 div/sec and EXTERNAL clock.

Analog Plot Facilities from 15-Way D-Type Connector

Y Output
100mV/div (±10%)

X Output
100mV/div (±10%)

Pen-Lift
Isolated single pole contact closes from start of command to end of plot cycle

Ext. Plot Clock
5kHz

+5V Auxillary Supply
Less than 100mA (22 series impedance)

AUTO PLOT

Indicates a plot at end of acquisition, then re-arms instrument at end of plot.

Specification

Section 2

MISCELLANEOUS

Calibrator

1V pk-pk ±1% at 50Hz to 50kHz depending on A Timebase Range. Time accuracy as for timebase range.

Probe Power

Power connector mounted on the front panel for Gould 10-TC-02 logic probe

POWER REQUIREMENTS

Voltage

90V-260V AC. No switching required between voltage ranges

Frequency

48-440Hz

Power

200W max. (4072)
250W max. (4074)

DIMENSIONS

See Figure 5.1 – -mm (approx)

WEIGHT

Net Weight

4072: 11.4kg (25lbs) approx.
4074: 12.3kg (27lbs) approx.

Shipping Weight

4072: 15.9kg (35lbs) approx.
4074: 16.8kg (37lbs) approx.

ACCESSORIES SUPPLIED

Operating Handbook
Front Panel Cover
Pack of 4 plotter pens
2 rolls of plotter paper
Line Cord
4072: 2-off PB36 Probes
4074: 4-off PB36 Probes

OPTIONAL ACCESSORIES

Rack Mount Tray with Slides PN 04094732

Cart TR7 General-Purpose Cart

Protective Carrying Case

PN 04101172 – a strong padded case enclosing the oscilloscope with three thicknesses of material covering the front panel

ENVIRONMENTAL

Temperature

Operating

0°C to 50°C

Specified

15°C to 35°C

Humidity

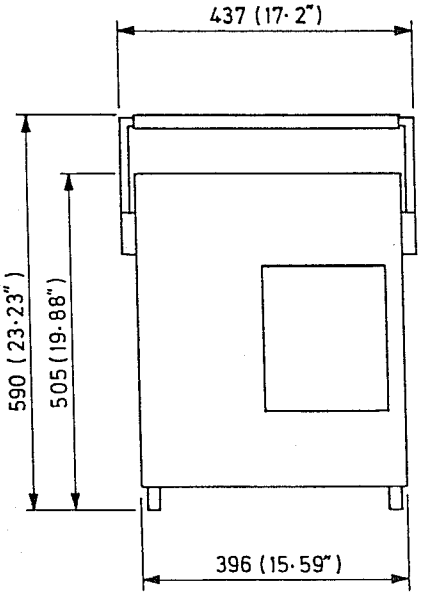
Tested to IEC 68-2-Ca operating 45°C at 95% RH
Tested to IEC-2-Dd cycling non-operating.
25°C-45°C, 95% RH cycles (144 hours).

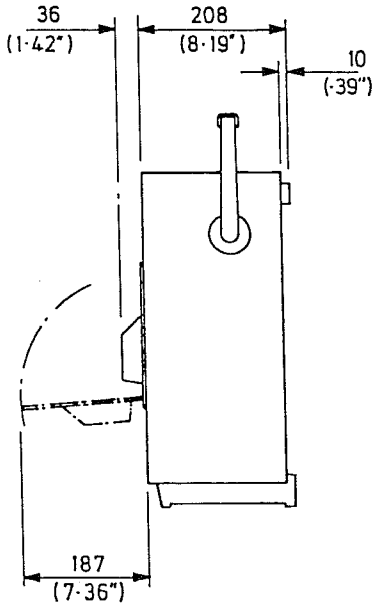
Safety

Complies with IEC-348 Cat 1 Standards.
CSA Approved.

Electromagnetic Interference (EMI)

meets VDE 0871 category A.





3.0 SYSTEM OVERVIEW

The first step in understanding the operation of the 4070 Digital Storage Oscilloscope is to gain an appreciation of how a signal is transferred from the input BNC to a trace on the display. Section 3.1 below describes the signal's path through the 4070's major circuits. Following this, microprocessor control, triggering and CCD corrections are described in detail.

3.1 FROM THE BNC TO THE SCREEN

Y Pre-Amplifier Board

The first circuit encountered by a signal after the input socket is the Input Attenuator. This performs the first step in converting the input signal, which has a wide dynamic range (from 5V/div to 2mV/div), to a signal of predetermined amplitude. This first circuit applies a 1:1, 10:1 or 100:1 attenuation to the signal. The degree of attenuation is dependent on the selected range, which is set by the operator or the Auto Setup function.

After this the signal flows through a series of attenuation/gain stages, until at a point midway through the Pre-Amplifier it is of the required amplitude. Thus, if we were to apply a sinewave of 5V pk-pk and select 5V/div we would have a signal of the same size at this point as if we had applied a 2mV pk-pk signal on the 2mV/div range.

In the above attenuator and gain stages, invert and variable gain are applied. These are produced by the same circuit (invert can be considered as an extreme form of variable gain, where gain=−1).

Having produced a signal of the required amplitude, a pickoff is fed to the trigger circuit. This is before any Y shift is added. Unlike many oscilloscopes, the 4070 controls Y shift directly from the microprocessor and not with a potentiometer on the front panel. This control is in the form of a voltage from the Voltage Generator circuit (see Section 3.2). The voltage is simply added to the input waveform before the the resultant signal is taken to the CCD board.

CCD Board

The 4074 is equipped with two identical CCD boards. The outer of the two is used for CH1 and CH3 and the inner for CH2 and CH4. The 4072 has only oneboard, fitted in the outer location.
The CCD board can operate in two completely different ways. The mode is dependent on the timebase setting: one mode is for the slow timebase ranges, 100μs/div and slower, and the other mode is for the fast timebase ranges 50μs/div to 20ns/div.

After the signal enters the board it is fed through the analog Max-Min Amplifier. In its normal mode this merely presents the signal to the input of the CCD chip. However, it can be set to detect glitches and aliases, in which case these are presented to the CCD input when they are detected. It is at this point that the operating mode of the board becomes dependent on the timebase range.

Timebase ranges of 100μs/div and slower

On these ranges each CCD chip is clocked at 2MHz and acts like an analog delay line, adding just over half a millisecond delay to the input signal.

Timebase ranges of 50μs/div and faster

On these ranges the signal is captured in the CCD chip before being replayed for digitisation. The clock rate of the capture is set by the selected timebase range. In particular, the ETS ranges, i.e. 100, 50 and 20ns/div, are all captured at the same 200MHz clock rate. The data for these ranges is interleaved to give the final apparent timebase range.

The replay rate is fixed at 500ns per sample irrespective of the rate of the capture.

The output of each CCD chip is buffered before being taken to the ADC board.

ADC Board

The ADC board takes the outputs of the CCD board(s), there are four signals in the 4074 and 2 in the 4072.
These are multiplexed together and the combined signals are presented to a sample and hold circuit prior to being digitised. The resultant digital outputs from the ADC pass to the Acquisition board via the Mother board.

Acquisition Board

At this stage in the path of the signal the samples are interleaved, one sample from each channel arrives at the acquisition board every 500ns.

The data is demultiplexed and digital Max-Min detection is applied, if selected. This circuit is only used on timebase ranges of 100μs/div and slower. On the faster ranges, up to 5μs/div, peak detection is performed by an analog Max-Min amplifier on the CCD board. Digital Max-Min is combined with the analog Max-Min to enable glitches as narrow as 5ns to be captured even on the slowest timebase range.

Data now passes to the acquisition RAM under the control of the Acquisition Gate Array. From here it is transferred directly to the display RAM over a local data bus connecting the Acquisition and Display gate arrays.

Display Board

Once the data is in the display RAM it will be presented to the display DAC sequentially in its allocated time slot. This DAC converts the digital information into an analog signal, a differential current, which is used to drive the Y output amplifier. The associated X signal is generated digitally by the Display Gate Array and converted to an analog signal by the X DAC. Again, like the Y output, this is in the form of a differential current which is used to drive the output amplifier.

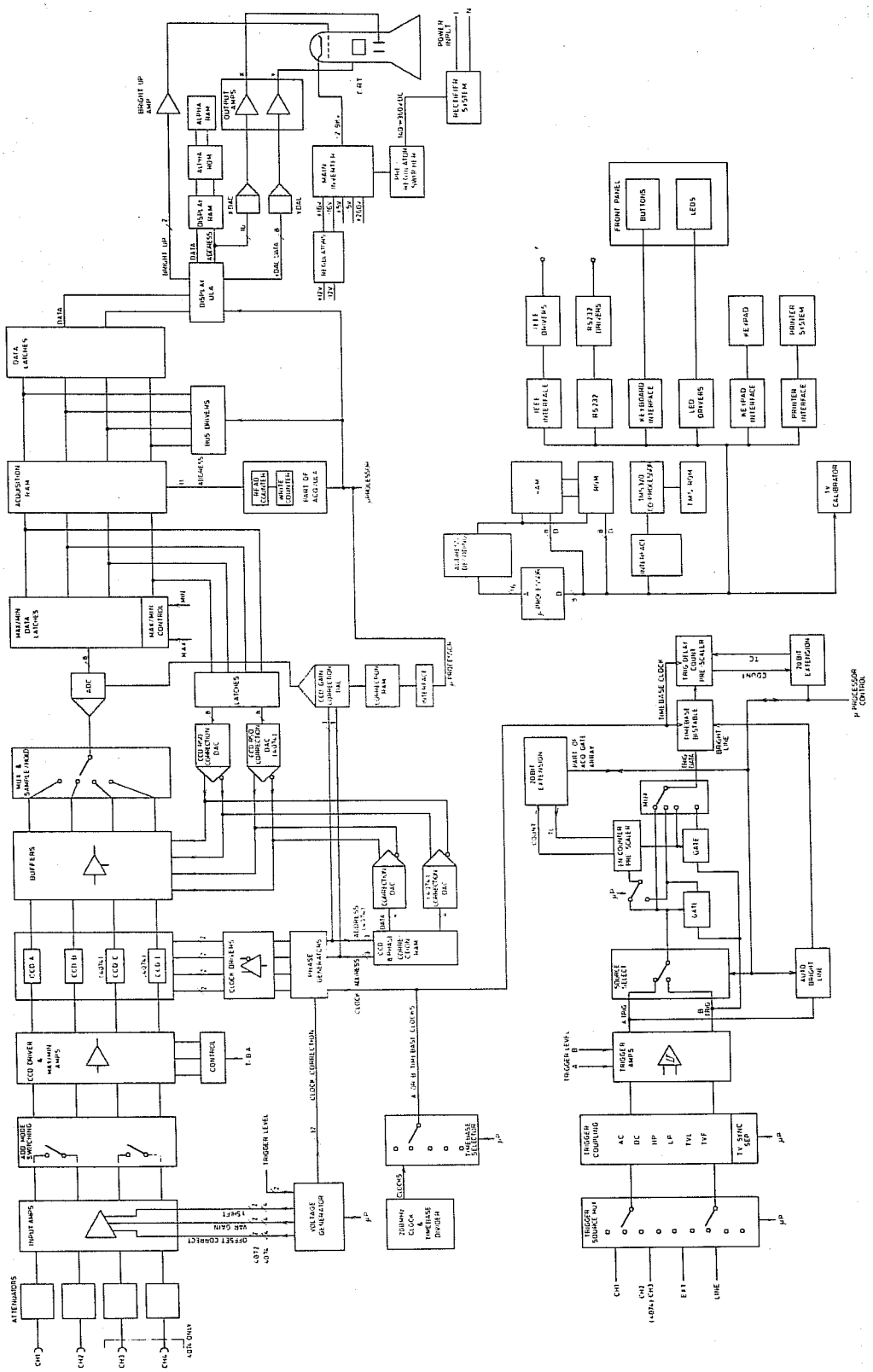


Figure 3.1 4070 Block Diagram

Y Pre-Amplifier Board

The signal ends where it began on the Y Pre-Amplifier board. Although named the Pre-Amplifier board it does in fact contain the X, Y and bright-up output drivers as well as the pre-amplifiers. These output stages drive the tube directly to produce the visible display.

3.2 MICROPROCESSOR CONTROL

Most of the circuitry in the 4070 is controlled by the 6809 microprocessor. This is implemented by three different techniques:-

8-bit Bus

The majority of functions within the system are controlled by ports that are directly attached to the processor by the 8 bit wide data bus. This covers such functions as front panel keyboard scanning, GPIB and RS423 interfaces and display control.

Serial Bus

One of the output ports on the I/O board is dedicated to controlling the serial bus. Its output consists of three clock and two data lines. To address a device one clock line and one data line become active. This allows a maximum of six devices to be addressed. Only five such devices are in fact installed, two controlling the setup of the pre-amplifiers, one controlling the setup of the trigger board and two controlling the front panel LEDs. Normally, the lines on this bus system are not active unless a control is being changed.

Voltage Generator

The remaining controls in the system are voltage controlled, the voltages being produced by the Voltage Generator. This consists of 72 voltage levels time multiplexed together. A number of these voltages are demultiplexed on the I/O board and distributed to where they are required. The Pre-Amp uses three of these lines per channel, i.e. shift, offset correction and variable gain. Most of the other controls are on the CCD board where they are demultiplexed locally. These are used to adjust the clocks for high speed acquisitions (see CCD corrections section 3.4)

3.3 TRIGGERING

As with the pre-amplifier, the trigger circuits can be more easily understood by following the path from the input BNC to the trigger output.

Two virtually identical amplifiers (CHA and CHB) exist on the trigger board. These are controlled via the trigger menu to select the trigger source and coupling selections.

Each trigger channel can take its source from one of four places:

4072 – CH1, CH2, Ext input and Line (supply frequency).
4074 – CH1, CH3, Ext input and Line.

The first circuit on the trigger board deals with selecting the source and coupling. The source selections are given above; and the coupling selections are AC, ACHP (AC high pass), ACLP (AC low pass), DC and DCLP (DC low pass). The TVL and TVF couplings are selected later in the circuit.

The signal is now fed into the trigger level comparator. Through several stages of amplification and conditioning the signal is compared with the trigger level. The resultant output is an ECL logic level indicating whether the input signal level is above or below that of the trigger level. As the input signal passes through the trigger level the logic output changes state.

The trigger output selector takes the above logic signal, plus the TV line and TV frame signals, finally passing the selected trigger signal to the Digital Timebase board.

Digital Timebase Board

This board provides the complex functions of trigger gating, time delay, trigger events delay and combinations of these. The two trigger channel outputs from the trigger board enter as differential ECL level signals which are then processed by the circuits providing the above complex triggering functions. The resultant output then initiates the acquisition. The acquisition gate array (on the acquisition PCB) is used to supplement the Digital Timebase board functions. It has for example, two very long counters which are used for the Divide by N and Delay by Time circuits. The high speed pre-scaling for these is on the Digital Timebase board. At slow timebase ranges (less than 100μs/division) the acquisition control is performed entirely by the acquisition gate array, whereas at high speeds acquisition control is performed additionally by the Digital Timebase circuitry in conjunction with the acquisition gate array.

Divide by N is provided by a free running counter, set to divide by the number N. Each time the terminal count, i.e. the Nth count, is reached, the acquisition is enabled. This same counter also provides the delay by N function: it is set with the number N and counts down to zero at which point the acquisition is enabled. In both cases only the first 5 bits of the counter are on the Digital Timebase board, the remainder being in the Acquisition Gate array.

In a similar manner to the trigger events delay, the time delay is produced by a counter. This time it is the acquisition clocks that are counted. On a normal acquisition, i.e. one with no time delay, 1024 clocks are counted. That is one clock edge for each sample. To give Pre-Trigger, or negative time delay, the counter is set to some number less than 1024. The number set represents the number of samples to be collected before acquisition is terminated. To give a positive time delay, a number greater than 1024 is entered. Although more than 1024 samples will clocked into the 4070 in this case, only the last 1024 are retained.

3.4 CCD CORRECTIONS

The CCD chip forms the heart of the 4070 acquisition system. This allows analog signals to be captured at high speeds, i.e. as quickly as one sample every 2.5ns. The signal is replayed at a slower rate for digitisation.

Each CCD, or Charge-Coupled Device, is constructed internally from eight charge-coupled lines, each of 128 cells in length. These are time multiplexed to give the appearance of one line 1024 cells long acting at eight times the speed.

Eight-Phase Offset

Each of the eight lines within a CCD chip can add a small DC offset to the signal. To remove this the instrument performs several captures to measure the effect. The microprocessor then calculates the required amount of inverse offset to remove it. The actual correction is done in the CCD output amplifier on the main CCD board.

Eight-Phase Gain

Each of the eight lines within the CCD chip can have a slightly different gain, which will be superimposed on the incoming signal. As before, the instrument performs several captures to measure the effect and a correction factor is calculated by the microprocessor. In this case the correction is applied as the signal is being digitised and the gain of the ADC is adjusted to compensate for the error.

RSO and Spatial Noise

These two very different effects are corrected by the same mechanism. They are both dependent on the position of the sample within the CCD chip, i.e. the position in the lines that form the CCD chip. Again, like the eight-phase offset, these errors appear as DC offsets superimposed on the signal waveform. The correction factors are held in 1024 bytes of RAM on the acquisition board. In other words, there is one correction factor for each cell within the CCD chip. The numbers contained in this RAM represent a correction voltage which is subtracted from the signal waveform as it enters the ADC board.

RSO (Rate of Signal Offset) This is a function of the leakage current within the CCD (Dark Current) which is dependent on the ambient temperature and the amount of time each charge packet spends in the CCD. Since the data in the first storage cell to be read out has only been in the CCD a short time it suffers least from the effect but the last cell to be read out suffers the maximum leakage. This RSO error manifests itself as a linear slope on the output data. In the 4070 the effect is minimised prior to correction by the design of the CCD chip and by using a high data rate.

Spatial Noise This effect is similar to RSO but is caused by the differential leakage between cells of the CCD which can manifest itself as a static noise pattern. This is minimised and corrected in the same way as RSO.

Clock Timing Because the CCD lines depend on eight separate clocks to perform the interleaved sampling, the time position of these must be controlled. This is calibrated in the 4070 by replacing the input signal with a 200MHz sinewave which is phase related to the timebase clock and then adjusting the phases of the CCD clocks for a static mid-scale readout for each CCD.

4.0 CALIBRATION

Many of the features of the 4070 are maintained in calibration by the internal microprocessor. However, as with any other oscilloscope, it should have a regular annual calibration. The schedule given below uses a minimum of test equipment, all of which should be readily available in any test department.

The instrument should arrive fully calibrated. This will ensure that the instrument will operate within specification for a period of not less than one year, under normal operating conditions (see Section 1.0). A few of the adjustments in the calibration procedure are interactive, i.e. the setting of one will affect the setting of others. In the schedule below it has been assumed that these controls will be set approximately correctly and require only a minor adjustment.

All controls are discussed individually with the exception of the Y Pre-Amplifiers, where only adjustments for Channel 1 are given.

The setup of other pre-amplifier channels is identical. To obtain the component number for the other channels add the following numbers to the marked references.

4072 – Channel 1 Add 200
Channel 2 Add 600

4073 – Channel 1 As shown
Channel 2 Add 200
Channel 3 Add 400
Channel 4 Add 600

It is recommended that the entire schedule is completed in order. Calibration cannot be assured if this is not done.

Equipment Required

1. Four Digit Digital Voltmeter
2. General Purpose Oscilloscope
3. Oscilloscope Calibrator
4. Fast Edge Generator, Tektronix PG506 or similar
5. Function Generator
6. High Frequency Signal Generator, Tektronix SG503 or similar
7. Capacitance Standardiser (20pF)
8. 50 Ohm input termination

4072 CALIBRATION SCHEDULE

Power Supply

These controls are accessible through the power supply assembly metalwork. See Figure 7.5 (Rear Panel Assembly).

DO NOT ADJUST SUPPLIES UNLESS REALLY NECESSARY

1. R52, −5V adjustment. Measure the −5V rail on the Mother board. This should be at the point where the lead from the power supply joins the board. Adjust R52 to give a reading of −5.0V ±50mV at this point.
2. R76, +12V adjustment. Measure the +12V rail on the Mother board. This is most easily taken at SKBC 27A. Adjust R76 to give a reading of +12V ±50mV at this point. See Figure 7.2 (Instrument Bottom View).
3. R78, −12V adjustment. Measure the −12V rail on the Mother board. This is most easily taken at SKBC 30A. Adjust R78 to give a reading of −12V ±50mV at this point. See Figure 7.2 (Instrument Bottom View).

Trace Rotation

Using a small screwdriver adjust the trace rotation control through the hole in the front panel. Set this to give a horizontal trace.

Focusing

The controls within this group are interactive, so to achieve optimum focusing it may be necessary to adjust these several times. All controls with the exception of R5 can be found on the Y Pre-Amplifier assmbly, see Figure 7.4 (Output Stage Adjustments). For R5 see Figure 7.1 (Instrument Top View).

WARNING *These controls are situated in areas containing high voltages, in some cases up to 3kV. Care should be taken to avoid touching any exposed tracks or components. All adjustments should be made with a suitably insulated tool.*

The X and Y dynamic focus controls should be set fully anticlockwise before the focusing adjustments are made.

4. R5, preset focus. Set the front panel focus control to mid travel and intensity to mid scale, then adjust R5 to the give best overall focus. This preset is located on the Tube Base board: take care whilst adjusting it as there are voltages in excess of 2kV present in this circuit.
5. R839, X mean plate. Measure the X output signal at R815 on an oscilloscope and adjust R839 to give a mean value of 120V ±5V. This may need a certain amount of extra adjustment to give the best overall focusing and geometry. Note: overall focusing may be checked by selection of the Master menu and the geometry may be checked by selecting the cursors.
6. R868, Y mean plate. Measure the Y output signal at R855 on an oscilloscope and adjust R868 to give a mean value of 120V. This may need a certain amount of extra adjustment to give the best overall focusing and geometry.
7. R826, X dynamic focus. Select the display menu and adjust R826 to equalise the focusing of the left and right edges of the screen with the centre.
8. R936, Y dynamic focus. With the display menu still selected adjust R936 to equalise the focusing of the top and bottom of the screen with the centre.

The controls are now set approximately. To achieve optimum focusing the above adjustments should be repeated, starting at number 4.

Note: *The X and Y store amplitude controls (see later) will also affect the mean plates, and hence the focusing. The focus controls may need further adjustment after the X and Y amplitudes have been set.*