

PIC16F627A/628A/648A

14.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16F627A/628A/648A family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection.

These are:

1. OSC selection
2. Reset
3. Power-on Reset (POR)
4. Power-up Timer (PWRT)
5. Oscillator Start-Up Timer (OST)
6. Brown-out Reset (BOR)
7. Interrupts
8. Watchdog Timer (WDT)
9. Sleep
10. Code protection
11. ID Locations
12. In-Circuit Serial Programming™ (ICSP™)

The PIC16F627A/628A/648A has a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low current Power-down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

14.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC16F627A/628A/648A EEPROM Memory Programming Specification" (DS41196) for additional information.

PIC16F627A/628A/648A

REGISTER 14-1: CONFIG – CONFIGURATION WORD REGISTER

$\overline{\text{CP}}$	—	—	—	—	$\overline{\text{CPD}}$	LVP	BOREN	MCLR $\overline{\text{E}}$	FOSC2	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
bit 13													bit 0

bit 13: **$\overline{\text{CP}}$** : Flash Program Memory Code Protection bit⁽²⁾
(PIC16F648A)
1 = Code protection off
0 = 0000h to 0FFFh code-protected
(PIC16F628A)
1 = Code protection off
0 = 0000h to 07FFh code-protected
(PIC16F627A)
1 = Code protection off
0 = 0000h to 03FFh code-protected

bit 12-9: **Unimplemented**: Read as '0'

bit 8: **$\overline{\text{CPD}}$** : Data Code Protection bit⁽³⁾
1 = Data memory code protection off
0 = Data memory code-protected

bit 7: **LVP**: Low-Voltage Programming Enable bit
1 = RB4/PGM pin has PGM function, low-voltage programming enabled
0 = RB4/PGM is digital I/O, HV on MCLR must be used for programming

bit 6: **BOREN**: Brown-out Reset Enable bit ⁽¹⁾
1 = BOR Reset enabled
0 = BOR Reset disabled

bit 5: **MCLR $\overline{\text{E}}$** : RA5/MCLR/VPP Pin Function Select bit
1 = RA5/MCLR/VPP pin function is MCLR
0 = RA5/MCLR/VPP pin function is digital Input, MCLR internally tied to VDD

bit 3: **$\overline{\text{PWRTE}}$** : Power-up Timer Enable bit ⁽¹⁾
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 4, 1-0: **FOSC<2:0>**: Oscillator Selection bits⁽⁴⁾
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor and Capacitor on RA7/OSC1/CLKIN
110 = RC oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor and Capacitor on RA7/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
100 = INTOSC oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

- Note**
- 1: Enabling Brown-out Reset does not automatically enable the Power-up Timer (PWRT) the way it does on the PIC16F627/628 devices.
 - 2: The code protection scheme has changed from the code protection scheme used on the PIC16F627/628 devices. The entire Flash program memory needs to be bulk erased to set the $\overline{\text{CP}}$ bit, turning the code protection off. See "PIC16F627A/628A/648A EEPROM Memory Programming Specification" (DS41196) for details.
 - 3: The entire data EEPROM needs to be bulk erased to set the $\overline{\text{CPD}}$ bit, turning the code protection off. See "PIC16F627A/628A/648A EEPROM Memory Programming Specification" (DS41196) for details.
 - 4: When MCLR is asserted in INTOSC mode, the internal clock oscillator is disabled.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = bit is set '0' = bit is cleared x = bit is unknown