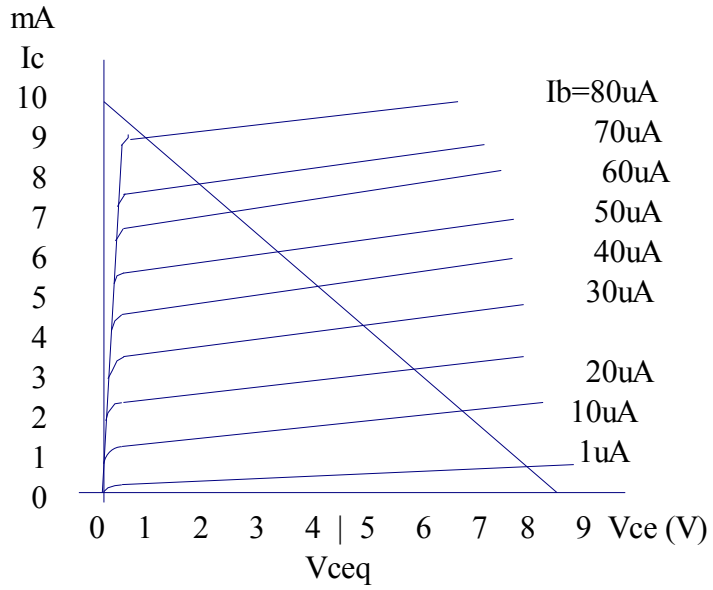
PRACTICAL CIRCUIT TUTORIALS

- **AMPLIFIERS**

Here we will first discuss BJTs and then FETs

➔ **BJT:-**



Output characteristics of a BJT

1. Select Vcq an Icq (for good class A amplifier $Vcq = \frac{Vcc}{2}$ and $Icq = \frac{Icmax}{(2)}$
2. Find Rc+Re as .... $Rc + Re = \frac{Vcc}{Icq}$
3. Set desired voltage gain as $\frac{(Rc)}{(Re)}$
4. Choose value for Re and from above equations find Rc
5. Set current through R1 and R2 as $Ibias = \frac{Icq}{10}$

   ..... Wonder why $\frac{Icq}{10}$? .. because keeping it this small will allow the R2 be in the available commercial range so that Vbe (voltage between base and emitter) remains at $Vbe = Icq * Re$ ...
6. As we already set Q point by selecting Vcq and Icq which will set some voltage as Vbe as explained in previous step we should make sure that the voltage drop across R2 is same as Vbe otherwise the transistor will deviate from our biasing point, in short ....

$Vbe = Icq * R\,e \;=\; Ibias * R2$.

7. Having found the R2 we can find R1 as $Ibias = \frac{(\ Vcc\ )}{(R1 + R2)}$.
8. Now the capacitors .....

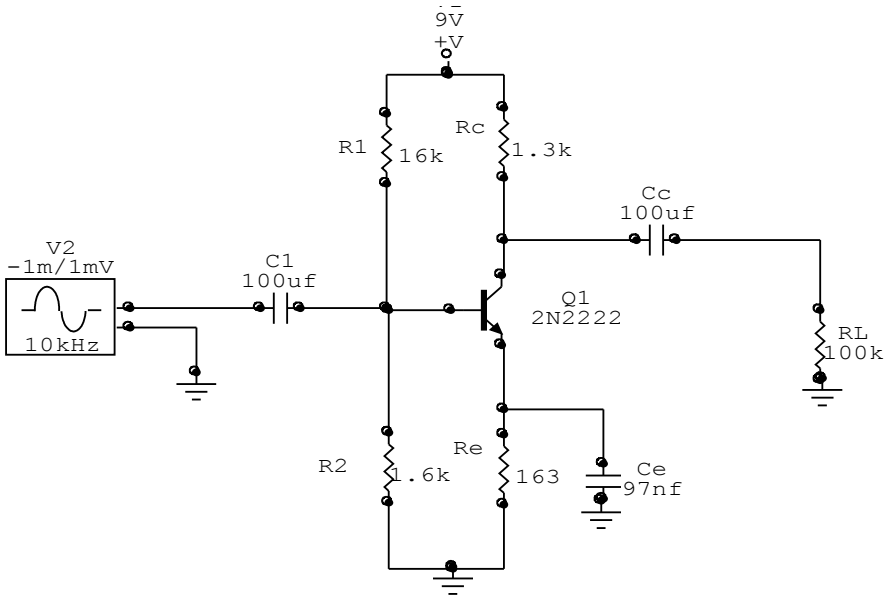
$$Ce = \frac{(\quad 1 \quad)}{(2 * pi * f * R\,e)}(peak - peak)$$

$$C1 = \frac{(\quad 1 \quad)}{(2 * pi * f * R2)}$$

$$Cc = \frac{(\quad 1 \quad)}{(2 * pi * f * RL)}$$

These are typical High Pass Filter equations.

- **Example 1.1:-**



Without Ce gain is 10 p-p and with Ce(sharply calculated as in figure) gain is 14 p-p

IF THE VALUE OF GAIN IS NOT OF IMPORTANCE THEN WE CAN SELECT Ce MUCH HIGHER THAN CALCULATED AND WE WILL GET THE HIGHEST POSSIBLE VALUE OF GAIN FOR THE PERTICULAR BJT.(In this example try setting Ce to 1uF)

Here is the Freemat (MatLab like software) code to design the common emitter amplifier. Save this script as CENPNdesign and then give the necessary parameters and you will have the values for R1, R2, Rc,Re and Capacitors.

```
function return_value=CENPNdesign(Vcc,Icmax,Gain,f)
printf 'type CENPNdesign(Vcc,Icmax,Gain,f)'
Icq=Icmax/2
Vcq=Vcc/2
printf 'a=Rc+Re'
a=Vcc/Icq
printf 'Gain=Rc/Re'
printf 'a=(Gain+1)*Re'
Re=a/(Gain+1)
Rc=(Re*Gain)-300
printf '\n\n this 300 is CB resistance (high output resistance)\n\n'
printf 'It is general considaration that .....'
Ibias=Icq/10
Vbe=Icq*Re
printf 'Vbe=Ibias*R2'
R2=Vbe/Ibias
printf 'b=R1+R2'
b=Vcc/Ibias
R1=b-R2
Ce=1/(2*pi*f*Re)
C1=1/(2*pi*f*R2)
printf 'Cc=1/(2*pi*RL)'
printf '\n\nSo the final values are...\n\n\n'
Rcfinal=Rc
Refinal=Re
R1final=R1
R2final=R2
Cefinal=Ce
C1final=C1     ;   ' THIS VALUE OF C1 WILL GIVE PEAK TO PEAK GAIN'
C1normalgain=C1*10
Ccfinal=C1
```

Here is the output for the example .

```
 CENPNdesign(9,10e-3,10,10e+3)
type CENPNdesign(Vcc,Icmax,Gain,f)
 Icq =
 5.0000e-003
Vcq =
4.5000
 a=Rc+Re
 a =
1800
Gain=Rc/Rea=(Gain+1)*Re
```

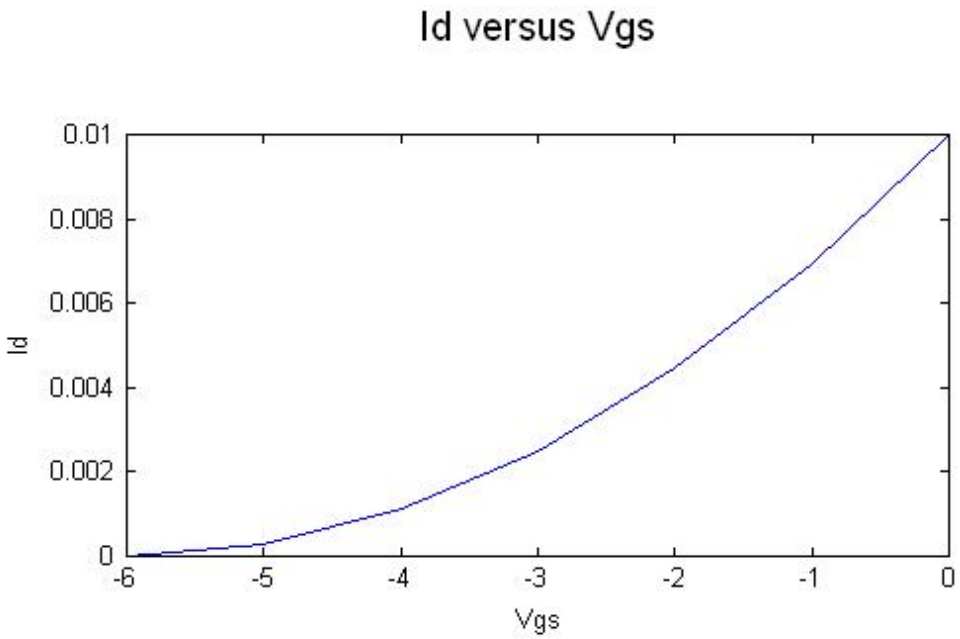
Re =
1.6364e+002
Rc =
1.3364e+003
this 300 is CB resistance (high output resistance)
It is general considaration that .....
Ibias =
5.0000e-004
Vbe =
0.8182
Vbe=Ibias*R2
R2 =
1.6364e+003
b=R1+R2
b =
18000
R1 =
1.6364e+004
Ce =
9.7261e-008
C1 =
9.7261e-009
Cc=1/(2*pi*RL)
So the final values are...
Rcfinal =
1.3364e+003
Refinal =
1.6364e+002
R1final =
1.6364e+004
R2final =
1.6364e+003
Cefinal =
9.7261e-008
C1final =
9.7261e-009
C1PtoPgain =
9.7261e-008
Ccfinal =
9.7261e-009

➔ **FET:-**

Biasing an FET is quit different from biasing a BJT. An FET takes voltage Vgs as input while a BJT takes current Ib as input, in other words FET is a voltage controlled device while BJT is a current controlled device. In BJT we set the bias point on output characteristics by the load line analysis while in FET the biasing point is selected by the study of **transfer characteristics (Id vs Vgs)** and also of the Drain characteristics**(Id vs Vds)** . The following will throw some light upon this discussion.

Note: See appendix for derivation of formula.....

$$Id = Idss\left[1 - \frac{Vgs}{Vp}\right]^2$$



Transfer characteristics of a JFET

1. First select a biasing point on the Drain characteristics by.....
   $Vdsq = \frac{Vds}{2}$ and $Idq = \frac{Idss}{2}$
2. Now having found Idq we can find $Rd + Rs = a$, as .....
   $a = \frac{Vdd}{Idq}$
3. From Idq we can also find Vgsq either from transfer characteristics or by the shorthand method as ....
   $Idq = \frac{Idss}{2}$ when $Vgsq = \frac{Vp}{4}$
4. Now let's assume that in voltage divider configuration voltgae at gate ...
   Vg = Voltage across R2 is ....say....0.006V
5. Now as we know ....
   Vth is threshold voltage = effective voltage at which change in Id start.
   $Vgs = (Vg - Vth) - Vs$
   $Vs = Idq * Rs = Vgs - Vg = \left(\frac{Vp}{4} \right) - 0.006\text{V}$
6. From above equation we can fnd Rs as .....
   $Rs = \frac{\left[\left(\frac{Vp}{4} \right) - 0.006\text{V} \right]}{(Idq)}$
7. From Rs we can calculate Rd as ....
   $Rd = a - Rs$

8. Now let the current through R1 and R2 be Ibias and let ....

$$Ibias = \frac{Idq}{100}$$ [This will alow the R1 and R2 be in avilable commercial range]

9. And we have assumed that voltage across R2 is 0.006V so.....

$$0.006 = Ibias * R2$$

$$R2 = \frac{0.006}{Ibias}$$

10. Having found R2 we can calculate R1 as ....

$$\frac{Vdd}{Ibias} = R1 + R2$$

$$R1 = \left(\frac{Vdd}{Ibias}\right) - R2$$

11. The gain (without any capacitor Cs) can be found by two method....

$$Gain = \frac{Rd}{Rs} or...$$

$$Gain = gm * Rd \; where$$

$$gm = gm0 * \left[1 - \left(\frac{Vgsq}{Vp}\right)\right], \qquad gm0 = \frac{(2 * Idss)}{(Vp)}$$

NOTE THAT THIS WILL BE THE HIGHEST POSSIBLE GAIN FOR SELECTED R1,R2, Rs AND Rd..GAI CAN BE IMPROVED BY ADDING Cs OF HIGHER VALUE THAN CALCULATED.(<u>Even calculated value of Cs will give slight higher gain than that of without Cs)</u>

12. Now the capacitors .....

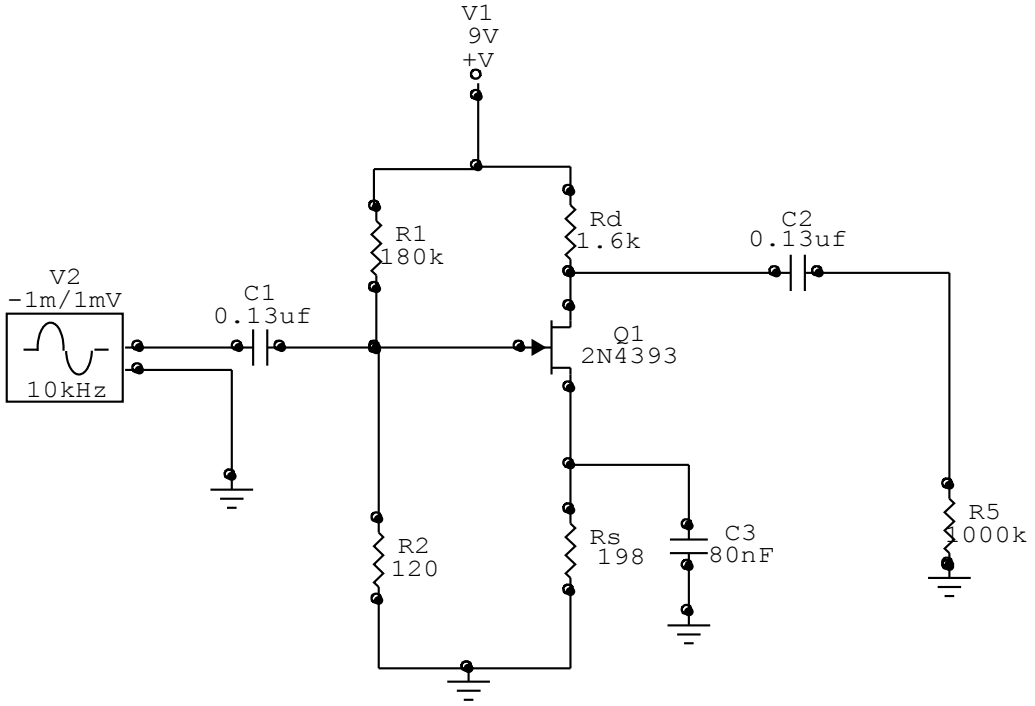
$$Ce = \frac{(1)}{(2 * pi * f * R\,e)}(peak - peak)$$

$$C1 = \frac{(1)}{(2 * pi * f * R2)}$$

$$Cc = \frac{(1)}{(2 * pi * f * RL)}$$

These are typical High Pass Filter equations.

- **Example 1.2 :-**



Without Cs gain is 8 p-p , with Cs (sharply calculated as in figure) gain is 10 p-p

IF THE VALUE OF GAIN IS NOT OF IMPORTANCE THEN WE CAN SELECT Cs MUCH HIGHER THAN CALCULATED AND WE WILL GET THE HIGHEST POSSIBLE VALUE OF GAIN FOR THE PERTICULAR JFET

Here is the Freemat code for calculation of component values.

```
function return_value = JFETCSdesign(Vdd,Idss,Vp,Vth,f)
printf 'JFETCSdesign (Vdd,Idss,Vp,Vth,f)'
Vpx=-1*Vp
'this -1 multiplication is to make |Vp|';
Vdsq=Vdd/2
Vdsq=(Vdd/2)-Vth
Idsq=Idss/2
a = Vdd/Idsq
'a = Rd+Rs';
Vgsq=Vpx/4
printf 'ASSUMED THAT IN VOLTAGE DIVIDER CONFIG. Vg = 0.006 = 6mV'
Vs=(Vgsq-Vth)-0.006
Rs=Vs/Idsq
'AS Rd+Rs = A, THEN...';
Rd=a-Rs
'As assumed before..... Vg = 6mV therefore,';
Ibias = Idsq/100
b=Vdd/Ibias
'b = R1+ R2';
R2 = 0.006/Ibias
R1 = b - R2
C1=1/[2*pi*R2*f]
'C2=1/[2*pi*RL*f]'; 'if RL is given ';
Cs=1/[2*pi*Rs*f]
printf '\n\n\nSO THE FINAL VALUES ARE ....\n\n\n'
R1final = R1
R2final = R2
printf '\n\nNOW THE FOLLOWING Rd IS FOR MAXIMUM POSSIBLE GAIN WITH THIS Rs
AND R1,R2 (WITHOUT Cs)\n\n'
Rdfinal = Rd
Rsfinal = Rs
C1final = C1
C2final = C1
Csfinal = Cs
GainPtoPmax = Rd/Rs
printf 'Even with exact value of Cs, gain will be slightly higher than Rd/Rs '
printf '\n\n\n VERIFY THIS BY TYPING JFETCS(Vdd,Idss,Vp,Vgs,R1,R2,Rs,) \n\n\n';
```

The following code will generate plots of Drain characteristics and Gm Versus Id so that we can verify our biasing mode. (Specify Vgs as Range , e.g. :- Vgs = -4:0)

```
function return_value=JFETCS(Vdd,Idss,Vp,Vgs,R1,R2,Rs)
printf 'type JFETCS(Vdd,Idss,Vp,Vgs,R1,R2,Rs)'
a=(1-(Vgs/Vp))
Id=Idss*(a.*a)
b=R2/(R1+R2)
Vg=(Vdd*b)
Idx=(Vg-Vgs)/Rs
gm0=(2*Idss)/(Vp)
printf '\n\ngm0 is gm at Vgs=0\n\n'
gm=gm0.*[1-((Vgs)/(Vp))]
'or gm = gm0.* [sqrt(Id/Idss)] because [1-(Vgs/(-Vp))] = sqrt(Id/Idss)';
'Note this (-Vp) so overall -(-Vp) = +Vp because gm cannot be NEGATIVE';
subplot (2,2,1)
'this (1,2,1) is (Vertical,width,number)';
plot(Vgs,Id,Vgs,Idx)
'Idx is Id with some Vg';
xlabel('Vgs');
ylabel ('Id');
title ('Id Versus Vgs','fontsize',15);
subplot (2,2,2)
plot(Id,-gm)
xlabel ('Id');
ylabel ('gm');
title ('gm Versus Id','fontsize',15);
```

Here is the output for calculation and characteristics for Example 1.2 :

Calculation:

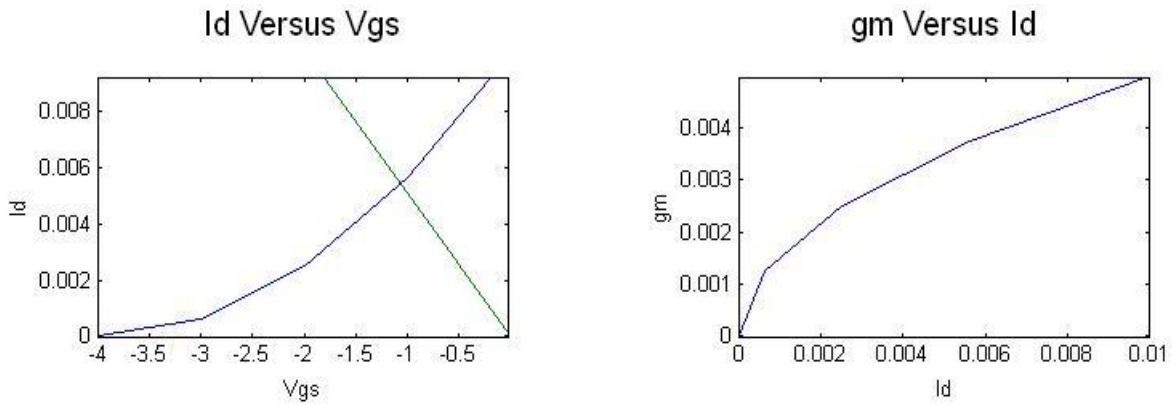
```
JFETCSdesign  (Vdd,Idss,Vp,Vth,f)
Vpx =     4
Vdsq =    4.5000
Vdsq =    4.5000
Idsq =    5.0000e-003
a =       1800
Vgsq =    1

ASSUMED THAT IN VOLTAGE DIVIDER CONFIG. Vg = 0.006 = 6mV

 Vs =      0.9940
Rs =      1.9880e+002
Rd =      1.6012e+003
Ibias =   5.0000e-005
b =       180000
```

R2 = 120
R1 = 179880
C1 = 1.3263e-007
Cs = 8.0058e-008
SO THE FINAL VALUES ARE ....
R1final = 179880
R2final = 120
NOW THE FOLLOWING Rd IS FOR MAXIMUM POSSIBLE GAIN WITH THIS Rs AND R1,R2 (WITHOUT Cs)
Rdfinal = 1.6012e+003
Rsfinal = 1.9880e+002
C1final = 1.3263e-007
C2final = 1.3263e-007
Csfinal = 8.0058e-008
GainPtoPmax = 8.0543

Even with exact value of Cs, gain will be slightly higher than Rd/Rs
VERIFY THIS BY TYPING JFETCS(Vdd,Idss,Vp,Vgs,R1,R2,Rs,)
The characteristics for Example 1.2 are .....

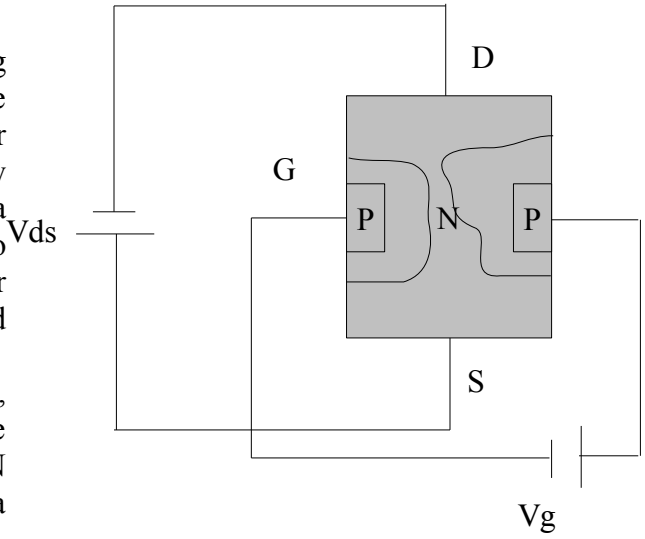


Note that the green line intersects the transfer characteristics at the set Vs ~ 1V

APPENDIX

Derivation of Id :-

The figure shows a typical JFET with biasing sources. As we know and shown in figure, negative gate voltage increases the width of depletion layer and hence decreases the width of channel. Now remember the very basic concept of capacitor that a capacitor is a dielectric or insulator separated by two plates of conductor. The capacitance of any capacitor depends upon the space between the conductors and the "conductivity of dielectric or insulator"
Looking to the figure it is evident that here in JFET , the depletion layers works as insulator or more like dielectric which is "separated" by two sides of N substrate namely D side and S side, So we can treat a JFET as variable capacitor.

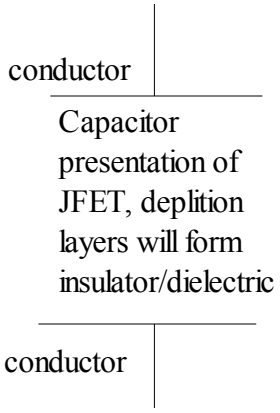


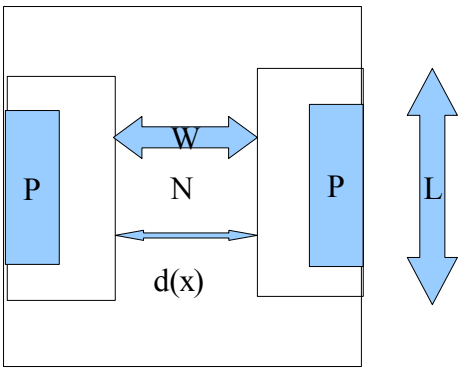
We know that .....

$$Vds = Vdd - Vgs$$

Now let the length of the channel be L and width W, we want to find the charge stored in the capacitor formed by channel, so first we will find the charge stored at width dx, which is infinitesimal width of the channel and then that charge will be integrated for length L.
As we know general equation for charge is .....

$$q = c*v$$





Therefore, for W(dx).....

$$dq(x)=[CW(dx)]*[Vds]$$
$$dq(x)=C*W(dx)*[Vdd-Vgs]$$

But, the maximum effective Vdd = Vp, for Vdd>Vp it's effect will still be that of Vdd on the drain current (current through capacitor, in this context) so, we can replace Vdd for Vp

$$dq(x)=C*W(dx)*[Vp-Vgs]$$

Now, the drain current (current through capacitor) will generate electric field, and its field strength is given by .....

$$E(x)=\frac{-[dV(x)]}{[\ dx\ ]}$$

(Electric field at point x, V(x)is the voltage at point x)
The negative sign shows that electron moves reverse than current Id, these electrons are pushed by the field strength E(x).

and, the dirft velocity by which the elctron moves is given by .....

$$\frac{dx}{dt}=-\mu_n E(x) \qquad where,\ \mu_n\ \ is\ \ mbility\ \ of\ \ electrons$$
$$\frac{dx}{dt}=\mu_n\frac{(dVx)}{(dx)}$$

Now the current at x is given by .....

$$I(x)=\frac{(dq(x))}{(dt)}=\frac{[dq(x)]}{[\ dx\ ]}*\left[\frac{dx}{dt}\right]$$
$$I(x)=\left[\frac{[CW(dx)[Vp-Vgs]]}{(\qquad dx\qquad)}\right]*\left[\mu_n\frac{(dV(x))}{(\quad dx\quad)}\right]$$
$$I(x)dx=CW\ (Vp-Vgs)(\mu_n dV(x))$$

Therefore, for the total of the channel current .....

$$\int_0^L Ixdx=\int_0^{Vds} CW(Vp-Vgs)*\mu_n dV(x)$$
$$[Ix*X]_0^L=[C\ W\ \mu_n(Vp-Vgs)]\left[\int_0^{Vds}(dV(x))\right]$$
$$[Id(L)-Id(0)]=C\ W\ \mu_n(Vp-Vgs)[x]_0^{Vds}$$
$$Id\ \ L=C\ W\ \mu_n(Vp-Vgs)(Vds-0)$$

As stated before Vds = Vdd -Vss = Vdd – Vgs (for Vg =0)

$Vds = Vp - Vgs$ (because maximum effct that Vdd can have on Id is that of $|Vp|$)

$Id\ L = CW\,\mu_n (Vp - Vgs)(Vp - Vgs)$

$$Id = C\left(\frac{W}{L}\right)\mu_n (Vp - Vgs)^2$$

$$\boxed{Id = \left[C\left(\frac{W}{L}\right)\mu_n Vp^2\right]\left[\left(1 - \frac{Vgs}{Vp}\right)^2\right]}$$

$$but,\quad C\left(\frac{W}{L}\right)\mu_n Vp^2 = \frac{(\quad Vp \quad)}{\left[\frac{(\quad 1 \quad)}{\left[C\left(\frac{W}{L}\right)\mu_n Vp\right]}\right]}$$

$but, Voltage * mobility = drift\ velocity$ therefore,

$$C\left(\frac{W}{L}\right)\mu_n Vp^2 = \frac{(\quad Vp \quad)}{\left[\frac{(\quad 1 \quad)}{\left(Vdirft * C\left(\frac{W}{L}\right)\right)}\right]}$$

$$C\left(\frac{W}{L}\right)\mu_n Vp^2 = \frac{(\quad Vp \quad)}{\left[\frac{(\quad 1 \quad)}{(Vdrift * charge)}\right]}$$

$$\boxed{C\left(\frac{W}{L}\right)\mu_n Vp^2 = \frac{(\quad Vp \quad)}{\left[\frac{(\quad 1 \quad)}{conductance}\right]} = \frac{Vp}{resistance} = \frac{Vp}{rd} = Idss}$$

So, finally we have .....

$$\boxed{Id = Idss\left(1 - \frac{Vgs}{Vp}\right)^2}$$