Edited by Bill Travis

Circuit provides ISFET-sensor bias

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ISFETs (ion-sensitive field-effect transistors) are useful for measuring the acidity of fluids. Accurate measurements require that the ISFET's bias conditions (I_D and V_{DS}) be held constant while the gate is exposed to the fluid under test. The acidity of the fluid changes the channel width, resulting in a gate-source voltage, V_{GS}, that is proportional to the fluid's pH. A recently published Design Idea shows a biasing circuit for the ISFET (**Reference 1**). The circuit in **Figure 1** provides a simpler and more accurate implementation. Voltage V_A sets I_D, the drain current, through ISFET Q_1, while voltage V_B sets V_{DS}, the drain-source voltage across Q_1. Both AD8821 high-precision instrumentation amplifiers, IC_1 and IC_2, are configured for unity gain. IC_3, the AD8627 precision JFET-input amplifier, buffers the drain voltage, V_D, ensuring that all of the current flowing through R_1 flows through Q_1.

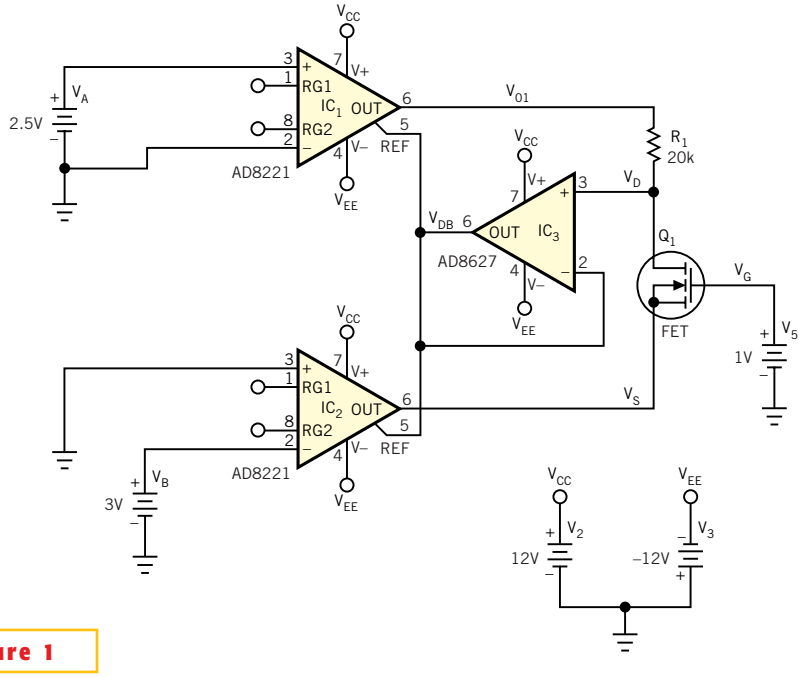

Figure 1

This circuit provides ideal bias for an ISFET, a sensor used to measure fluid acidity.

To control I_D, amplifier IC_1 forces the differential voltage between its output and the reference input to equal its differential input voltage, V_A. Because the sensed differential voltage is equal to the voltage across R_1, $I_D = V_A / R_1$. With R_1 set to 20 kΩ, I_D scales to 50 µA/V. Similarly, amplifier IC_2 forces the differential voltage between its output and the reference input to equal its differential input voltage, V_B, thus forcing V_{DS} to equal V_B. (Note: If your design does not require independent adjustment of V_{DS} and I_D, the circuit can operate from a single control voltage. Tie V_A and V_B together and drive it with the desired voltage V_{DS}. R_1 is then equal to V_{DS}/I_D.) The voltage of interest, V_{GS}, appears between the gate voltage and the output of IC_2. A useful feature of this circuit is that the current source floats, enabling the gate voltage to connect to any voltage within the common-mode range of the circuit. For this circuit, the range of V_G is $(V_A+2-V_{EE}) < V_G < (V_{CC}-2-V_A)$.

Figure 2 shows the advantage of the

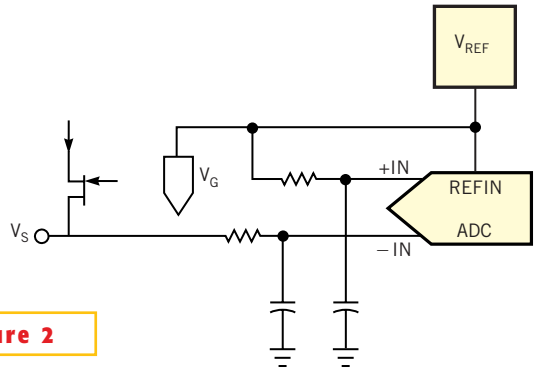

Figure 2

This configuration shows the advantage of the floating gate when the circuit of Figure 1 connects to an ADC.

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floating gate when the circuit is connected to the AD7790 differential-input sigma-delta ADC. The gate voltage connects directly to the ADC's reference. The only signal-conditioning circuitry required between V_S or V_G and the ADC's input is a simple RC filter. The 0.1% error in resistor R_1 dominates the current-source errors for currents higher than 1 µA and, therefore, are less than 250 nA for drain currents as high as 250 µA. The V_{DS} errors originate from the gain error of IC_3 and input offset voltages of IC_2 and IC_3. The error in drain-source voltage is less than 450 µV for drain-source voltage as high as 2V.□

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Microprocessor supervisor and regulator form in-range voltage monitor

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Low-cost microprocessor supervisors reset controllers when power-supply voltages fall below given levels. As added protection, you can also reset the microcontroller when the power supply is too high by combining a low-cost shunt-voltage regulator with a supervisor that has a manual reset input. A simple overvoltage/undervoltage-protection circuit is easy to make (**Figure 1**). The circuit's output is active (low) when the monitored supply voltage, V_{CC}, is outside a predefined range. After the supply voltage returns to within the functioning limits, the reset output, $\overline{RST}$, remains active for a minimum of 140 msec. This interval gives the system time to stabilize before you remove the reset. The threshold voltage of the CAT811 microprocessor reset circuit, IC_2, sets the lower limit of the voltage range, V_{LOW}. This threshold can be 2.32 to 4.63V using standard products. Custom threshold devices with thresholds as low as 1.8V are also available. The 1.24V CAT431L shunt regulator, IC_1, and two resistors, R_1 and R_2, set the upper limit, V_{HIGH}: $V_{HIGH}=V_{REF}(1+R_1/R_2)$, where V_{REF} is the internal reference voltage of IC_1 ($V_{REF}=1.24V$). The maximum V_{HIGH} that you can set is 5.5V, and the maximum supply voltage is 9V.

This design uses the CAT811 supervisor with a threshold voltage of 4.63V

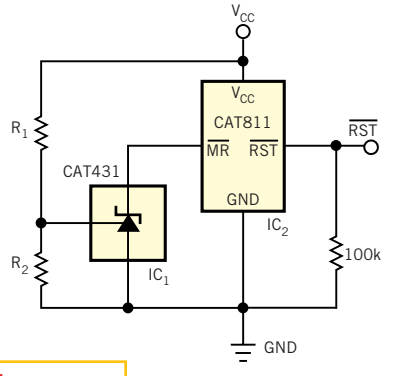


Figure 1

This simple circuit uses a microprocessor supervisor and a shunt regulator to form an overvoltage/undervoltage-protection circuit.

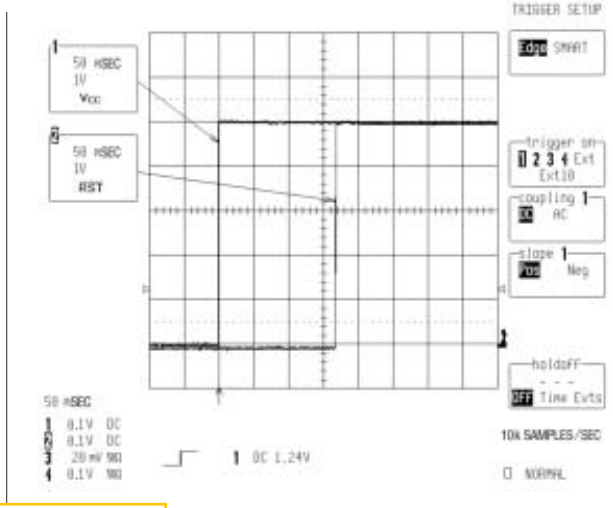


Figure 2

As the supply voltage rises into range, the reset pin in Figure 1 becomes active low.

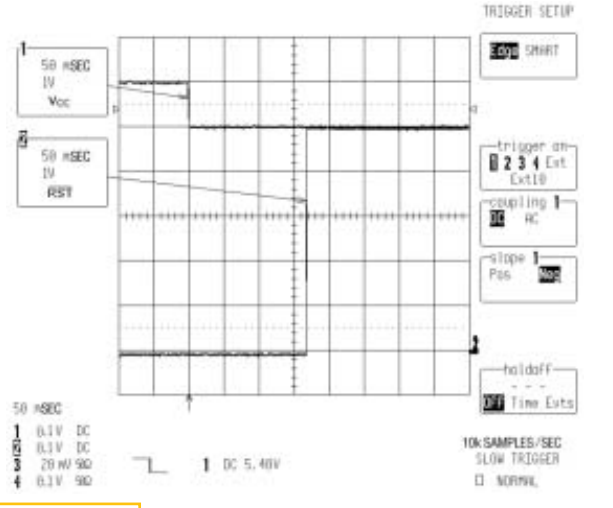


Figure 3

As the supply voltage falls into range, the reset pin in Figure 1 becomes active low.

for tests. The upper limit of the voltage range is 5.5V using a 10-kΩ potentiometer with R_1=7.75 kΩ and R_2=2.25 kΩ. As the supply voltage rises into range, the reset pin becomes active (low) for a minimum of 140 msec (**Figure 2**). When the supply voltage falls into range, the reset pin also becomes active (low) for a minimum of 140 msec (**Figure 3**). A reset signal asserts when the supply voltage increases out of range (**Figure 4**). A reset signal also asserts when the supply voltage falls out of range (**Figure 5**).□

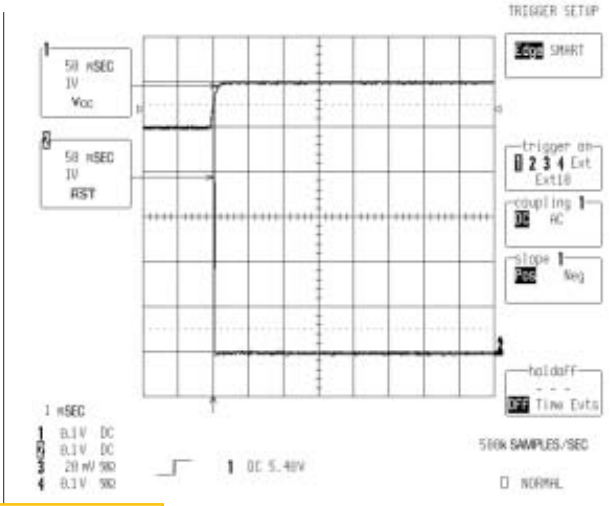


Figure 4

The reset signal in Figure 1 asserts when the supply voltage increases out of range.

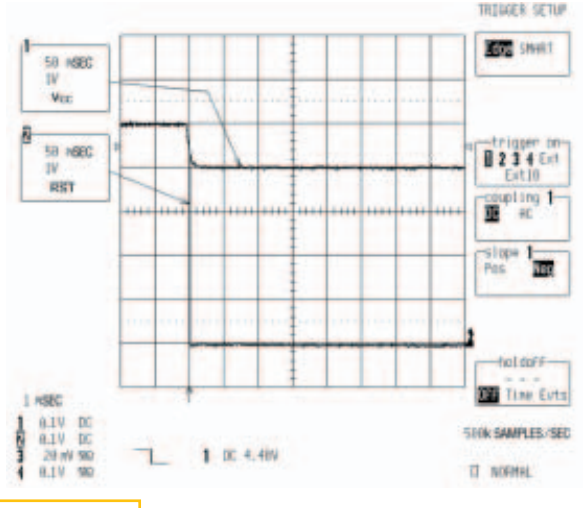


Figure 5

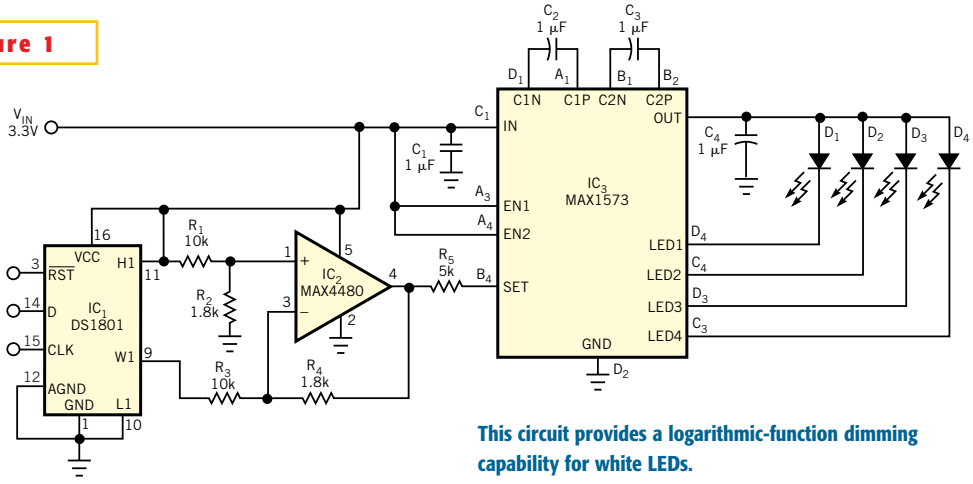
The reset signal in Figure 1 asserts when the supply voltage falls out of range.

White-LED driver provides 64-step logarithmic dimming

William Hadden, Maxim Integrated Products, Sunnyvale, CA

The circuit of **Figure 1** is designed for portable-power applications that require white LEDs with adjustable, logarithmic dimming levels. The circuit drives as many as four white LEDs from a 3.3V source and adjusts the total LED current from 1 to 106 mA in 64 steps of 1 dB each. The driver is a charge pump that mirrors the current I_{SET} (sourced from IC_3's SET terminal) to produce a current of (215•I_{SET}±3%) through each LED. Internal circuitry maintains the SET terminal at 0.6V. To control the LED brightness, op amp IC_2 monitors the difference between the high-side voltage and the wiper voltage of digital potentiometer IC_1. The op amp then multiplies that voltage by a gain to set the maximum output current. Zero resistance at the potentiometer's W1 terminal corresponds to minimum LED current and, therefore, minimum brightness. Because the SET voltage is fixed at 0.6V, any voltage change at the left side of R_5 changes I_{SET}, and the resulting change in LED

Figure 1



This circuit provides a logarithmic-function dimming capability for white LEDs.

currents alters their brightness level. R_5 sets the maximum LED current: $R_5 = 215 \times 0.6/I_{LED(DESIRED)}$, where I_{LED} is the current through one LED.

IC_1 is a digital potentiometer with a logarithmic taper and an analog-voltage wiper. Each wiper tap corresponds to 1 dB of attenuation between H1 and W1 (pins 11 and 9). The IC contains two potentiometers controlled by a 16-bit code via a three-wire serial interface. To set the LED current, drive $\overline{RST}$ high and clock 16 bits into the D terminal of IC_1, starting with the LSB. Each pulse at CLK enters a bit into the register. The circuit uses only one potentiometer, so bits 0 through 7 are "don't-care" bits. Bits 8 through 14 determine the wiper position: Bits 8 through 13 set the code, and bit 14 is "mute." (Logic one at bit 14 produces the lowest possible output current by setting the left side of R_5 at approximately 0.599V.) After entering all 16 bits, enter the code and change the brightness level by driving $\overline{RST}$ high. **Figure 2** shows the logarithmic relationship between an LED current and the potentiometer's input code.□

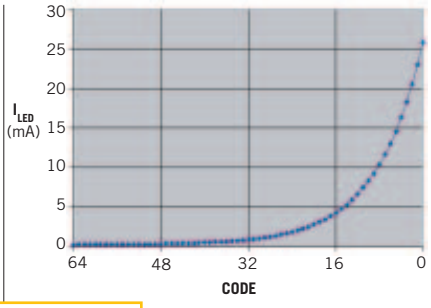


Figure 2 LED current versus input code changes for the circuit in Figure 1.

Switcher improves overvoltage-protection circuit

Jason Rubadue, National Semiconductor, Thornton, CO

Overvoltage-protection circuits often protect electronic devices from power-supply transients, such as a rise from plugging in batteries or an external power adapter. Although these devices traditionally find use as hysteretic switching controllers, you can reconfigure the LM3485 (**Figure 1**) to provide a robust overvoltage-protection circuit.

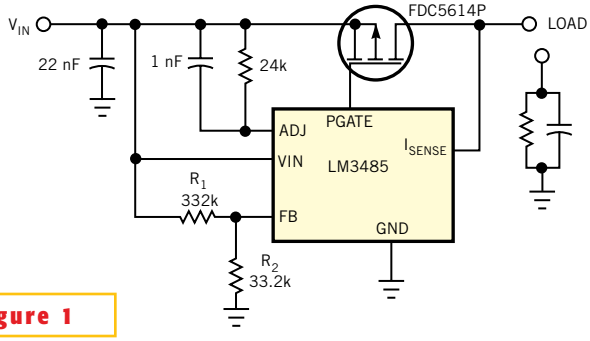


Figure 1 A hysteretic switching controller can do double duty as an overvoltage-protection circuit.

By selecting the feedback resistors using the formula $V_{IN} = 1.252(R_1+R_2)/R_2$, you can program the IC to trip off at any level from 4.5 to 35V. In **Figure 1**, R_1 and R_2 turn off the PFET when V_{IN} exceeds 13.8V. You can calculate the hysteresis using the formula $V_{HYS} = 0.01(R_1+R_2)/R_2$. In this example, the expression calculates a hysteresis of 110 mV. The accompanying oscilloscope plot of V_{OUT} versus V_{IN} shows the sample circuit with a hysteresis of roughly 800 mV (2V/division, 0V level at lowest line, 500 nsec/division). Why isn't it 110 mV as calculated? We measured the turn-off propagation delay of the sample circuit at approximately 450 nsec, almost one complete time division, whereas the turn-on propagation delay was only 70 nsec (all measured using a 40Ω load). By taking these propagation delays into account, the scope plot approaches the calculated hysteresis and 13.8V trip level. However, compare these times with competing ICs with larger typical propagation delays of 500- to 6000-nsec turn-off times and 1800- to 7000-µsec turn-on times. The improved propagation delay is a result of the LM3485's driver, which can sink 320 mA and source 440 mA, as opposed to other overvoltage-protection circuits, which sink only approximately 60 mA.

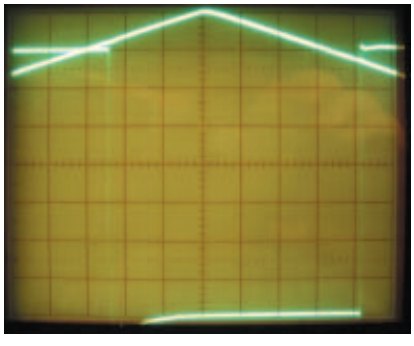


Figure 2 This plot shows the hysteresis and the overvoltage trip point.

The LM3485 also has an adjustable overcurrent-protection feature. In the sample circuit, when the current exceeds 1.1A, the LM3485 turns off the FET. After 9 µsec, the LM3485 turns back on the FET and begins sensing the current again through the FET's on-resistance. For more precise current sensing, add an external current-sense resistor between the FET and V_{IN} and then move the I_{SENSE} line of the LM3485 over to the source of the FET. The sample circuit in **Figure 1** is derived from the standard LM3485 evaluation board. You can easily modify this board to create an overvoltage-protection circuit by removing a few components—the inductor, the diode, and the C_{FF} capacitor—by moving the feedback line from V_{OUT} to V_{IN}, and by selecting suitable resistor values.□

Precision peak detector uses no precision components

Jim McLucas, Longmont, CO

When you need a precision peak detector, you would usually implement it with one or several op amps and a few other associated components. This technique usually works well unless your design requires operation higher than a few kilohertz. In designs requiring such operation, the accuracy of the circuit severely deteriorates unless at least one of the amplifiers has a high slew rate and frequency response extending to tens or even hundreds of megahertz. Performance depends on the desired frequency response and peak-to-peak input-voltage range of the peak detector (**Reference 1**). The circuit in **Figure 1** uses a moderately fast, inexpensive comparator instead of a high-slew-rate op amp to implement the peak detector. This circuit provides wide bandwidth and high accuracy without the use of precision components, and it's simple and inexpensive—about $3.50 (1000).

The high-input-impedance FET source follower, Q_1, and the associated circuitry enclosed by the dotted line in **Figure 1** buffer the input to the comparator. This buffer is essentially the design published in **Reference 2**. Op amp IC_{2D} forces the dc voltage at the input to the comparator at the junction of D_1 and R_3 to be equal within a few millivolts to the dc voltage at the FET gate. If the peak detector has a driver with an impedance of less than approximately 150Ω, you can eliminate the buffer in the dotted-line box. However, as the source impedance increases, the accuracy of the peak detector decreases if you don't use the buffer. An LM306 comparator, IC_1, provides sufficient speed and current to charge the holding capacitor, C_3, over an input range of 25 Hz to more than 1 MHz, with an input-voltage range of 500 mV peak to more than 4V peak. The comparator exhibits a few millivolts of hysteresis, which improves its switching speed and prevents random oscillation when its input voltage is in its linear range.

This circuit works by essentially creating its own reference for the negative input of the comparator. If the voltage on the positive input of the comparator is greater than the voltage at the negative input, the comparator's output goes high and charges capacitor C_3 until the voltage on the capacitor is a few millivolts greater than the voltage on the positive input. Then, the comparator stops charging C_3 until the cycle repeats. This action ensures that the voltage on holding capacitor C_3 is nearly equal to the peak voltage at the input to the comparator. Schottky diodes D_2 and D_3 couple the output to the holding capacitor, C_3. The feedback from the output of IC_{2A} to the junction of D_2 and D_3 keeps D_3 biased to 0V when it is off, thereby preventing reverse leakage through D_3 (**Reference 2**). The feedback

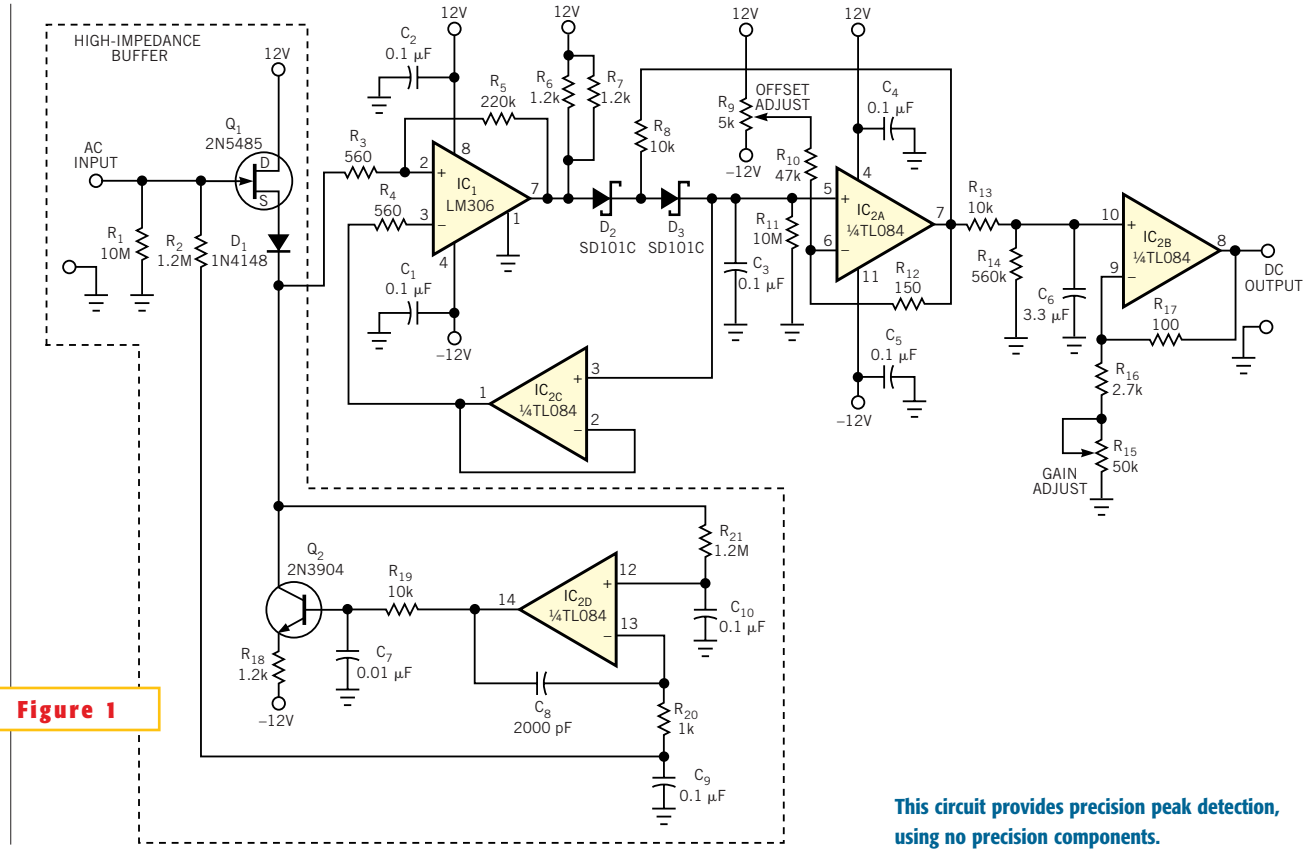


Figure 1

This circuit provides precision peak detection, using no precision components.

also provides reverse bias to D_2 when the output of the comparator is pulled low. The IC_{2A} FET-input op amp has low input-bias current, so it does not discharge C_3 between charging pulses. IC_{2C} buffers the negative input of the comparator for the same reason. The 10-MΩ resistor, R_{11}, provides sufficient discharging of C_3 so that the dc output from IC_{2B} decay to a negligible level in two to three seconds after removal of the ac-input signal.

R_{13} and C_6 filter the dc output to remove most of the noise that the comparator causes. R_{14} provides a small amount of attenuation of the dc output, so that R_{15} can provide approximately ±2% adjustment of the dc output. For best precision, set R_{15} for minimum gain and apply a 500-mV, 10-kHz signal to the input. Adjust R_9 for 500-mV dc output. Then, apply a 4V, 10-kHz signal and adjust R_{14} for 4.010V-dc output. Check and repeat these two adjustments if necessary. If a precision ac source is not available, you can use an accurate dc source and a high-impedance voltmeter for calibrating the circuit. Apply 500-mV dc to the input and adjust R_9 for 499 mV at Pin 10 of IC_2. Then, apply 4V dc to the input and adjust R_{15} for 3.980V output (Pin 8 of IC_2). The maximum peak input voltage is approximately 5V, because the maximum input-voltage specification for the LM306 is ±7V. The accuracy of the circuit decreases when the input peak is higher than 4V. Remember to use a blocking capacitor in series with the input if the signal to be measured includes a dc offset that can cause the peak input voltage to exceed approximately 5V. **Table 1** shows measured results for the circuit. If desired, you can delete R_9, R_{10}, R_{14}, R_{15}, and R_{16} from the circuit and still obtain good performance.□

TABLE 1–MEASURED RESULTS FOR PEAK-DETECTOR CIRCUIT

Frequency (Hz)	**25**	**50**	**100**	**1000**	**10K**	**100K**	**1M**	**2M**	**3M**
% error (500 mV peak input)	2	0.6	0.2	0	1	0.8	−0.5	−3.2	−5.4
% error (1V peak input)	1.8	0.4	0	0.1	0.8	0.7	−1.3	−3	−5.2
% error (2V peak input)	2.1	0.4	0.1	0.3	1.0	1.4	−0.6	−2	−3.8
% error (4V peak input)	2	0.8	0.5	0.5	0.8	0.8	−0.5	−1.8	−3.5

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