

## EE455

### Design Project # 2

Due 11/17/03

1. Design a MOS differential amplifier to meet the following specifications;

$$R_{idm} > 500k\Omega$$

$$R_{odm} < 1k\Omega$$

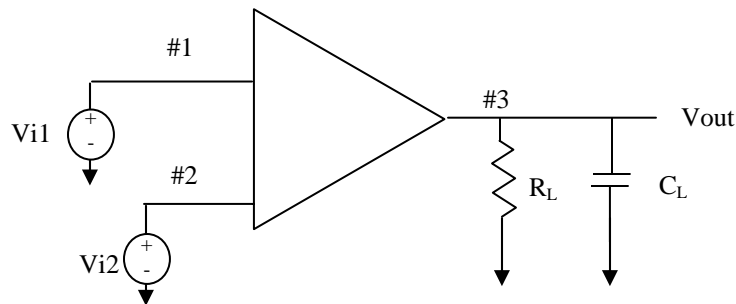
$$A_{vdm} > +/-4000$$

$$A_{vcm} < +/-1$$

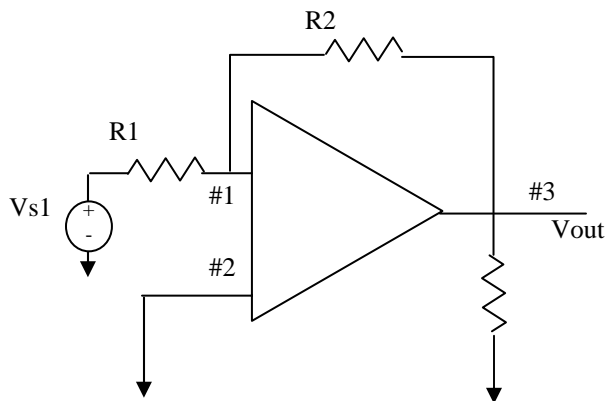
Bandwidth from dc to as large as possible.

The small-signal input will have an amplitude of  $50 \mu V$ .

Show all hand calculations !



2. Let  $V_{DD}=10V$ ,  $V_{EE}=-10V$  and the load resistor  $R_L=2K$  and  $C_L = 10pF$
3. Begin with hand calculations and calculate the desired operating point and bias conditions of each transistor. (i.e. design on paper first !)
4. Use SPICE to verify your design. Verify the final OP point of each transistor. Clearly put your name in the heading and mark clearly your final results. The inputs must be labeled as Node#1 and Node#2 and the output Node#3.
5. Include as graphs:
  - (a) DC transfer curve of  $V_{out}$  vs. differential input voltage  $V_{id}$ .
  - (b) AC gain  $V_{out}/V_{in}$ , vs. frequency.
6. Verify the operation of the differential amplifier as an OP AMP in SPICE to gain of 50. (you need to choose the values of  $R_1$  and  $R_2$ ).



- Use the following parameters for the simulation and hand calculation.

```
.model nfet nmos
+vto=0.8 kp=90.0e-6 gamma=0.5 lambda=0.08 phi=0.7
+cbd=0.02e-12 cbs=0.02e-12
+cgsO=2e-10 cgdO=2e-10 cgbO=2e-10
+tox=300e-10
```

```
.model pfet pmos
+vto=-0.9 kp=30.0e-6 gamma=0.8 lambda=0.05 phi=0.7
+cbd=0.02e-12 cbs=0.02e-12
+cgsO=2e-10 cgdO=2e-10 cgbO=2e-10
+tox=300e-10
```

- Hint, on the SPICE verifications of  $A_{vd}$ ,  $A_{cm}$ ,  $R_{in}$  and  $R_{out}$ , you may use the .TF command since the amplifier is DC coupled. To simulate differential and common-mode input signals, you could use the voltage controlled voltage source. This has the general form:

EXXX N+ N- NC+ NC- VALUE

N+ is the positive node, and N- is the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the voltage gain.

For example E1 2 0 1 0 -1 is a voltage source between nodes 2 and 0 whose output is the negative of the voltage between nodes 1 and 0.

- Design Vbias and Ibias sources as needed
- Calculate CMRR from hand calculations and compare to the results from SPICE.
- Prepare a formal Engineering report consisting of a cover page and the following sections.

- (I) Executive summary
- (II) The designed circuit. List any specifications and your final designed circuit labeled with the Spice nodes.
- (III) Show a summary of your spice simulation consisting of input deck, graphs as specified above and some numerical output.
- (IV) Summary/Conclusions. (Sometimes a good table is useful in the data summary.)
- (V) Technical appendix including hand calculations of operating point, gain, input impedance, output impedance, and  $\omega_{-3dB}$

Sections I-IV should be typed; section V may be hand-written. This is an individual project.