



RA6963

Dot Matrix LCD Controller Specification

Version 1.7

May 5, 2011

RAiO Technology Inc.

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| Update History | | |
|----------------|--------------------|--|
| Version | Date | Description |
| 1.0 | May 29, 2007 | Formal Release |
| 1.1 | September 27, 2007 | Update Figure 9-4 |
| 1.2 | November 15, 2007 | Update < Table 8-2 > Max. f_{OSC} to 18MHz. Update < Table 8-4 > Max. f_{SCP} to 9MHz. Update the Chapter 5-4 "Misc Interface" – the description of pin "MDS" and MD[1:0]. |
| 1.3 | February 26, 2008 | Update the description of pin "X1" in Section 5-4. Update Figure 6-13, 6-14, 9-5 and 9-6. |
| 1.4 | March 27, 2009 | Update < Table 6-5 > Command Definition Description. Update Figure 6-10. Update < Table 6-31 > Package Description in Section 6-21. Update < Table 8-2 > |
| 1.5 | July 07, 2009 | Update Figure 9-6 |
| 1.6 | March 02, 2010 | Update the Section 7-1 : Die Form |
| 1.7 | January 20, 2011 | Update <Table 5-4> : delete the description of FONTSEL Update <Table 6-1> : the description of CDATA Update <Table 6-15> Delete Section 6-16 : Screen Reverse Delete Section 6-17 : Blink Time Delete Section 6-18 : Cursor Auto Moving Delete Section 6-19 : CGROM Font Select Delete Section 6-21 : RA6963 vs T6963C Delete Section 7-1 : Die Form Delete Section 7-2 : Part Number Delete Section 7-3 : XY Coordinate |
| | May 5, 2011 | Modify feature description - 256 word ROM -> 128 word ROM Delete feature description – Bold and Display reverse |

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1. Overview

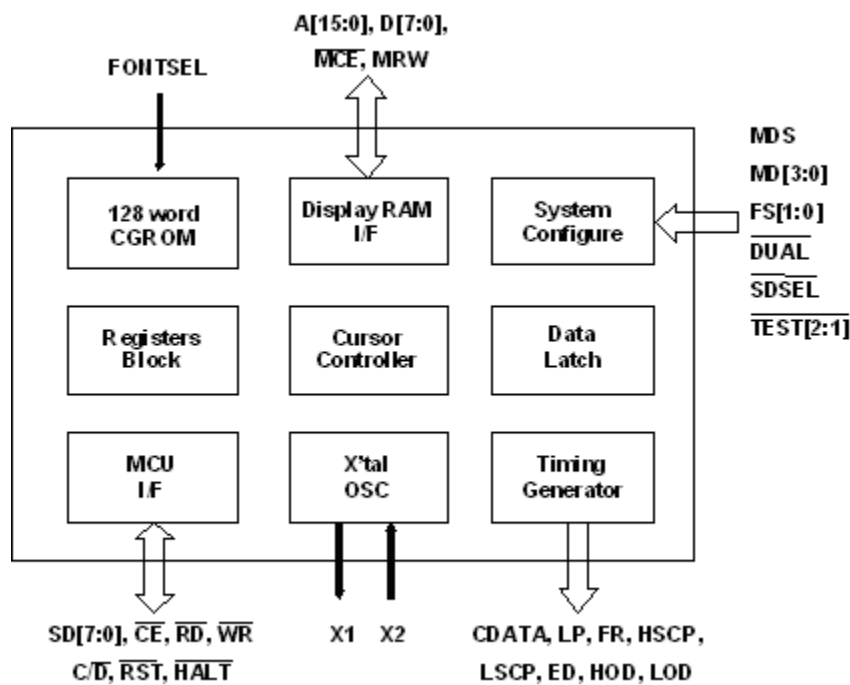
The RA6963 is a dot matrix LCD Controller which fully compatible with T6963C. It supports various LCD Driver for standard or custom-made LCD module. The RA6963 built-in a 128-word CG(Character Generator) ROM that for ASCII, Japanese or numeric display in text mode. It also supports Graphics mode and mixed display with Text. The supported maximum external display RAM is 64Kbyte and the display Window can be moved freely within the allocated memory range. The RA6963 has an 8-bit parallel data bus that can be directly connected to an 8080 series MPU.

The RA6963 supports a very broad range of LCD formats by allowing selection of different combinations via a set and combination text-and-graphic modes, and includes various attribute functions.

2. Features

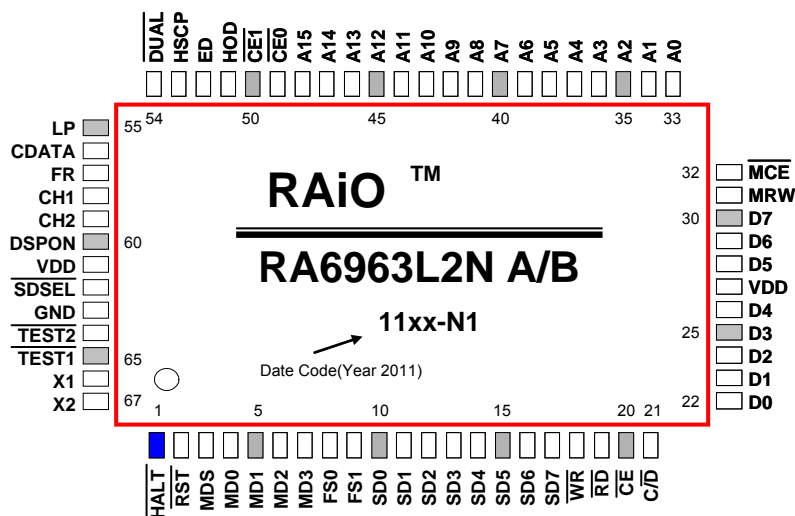
- ◆ Support Display Range:
Columns → 32, 40, 64, 80
Rows → 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32
- ◆ Support 8080 8-bit MPU Interface
- ◆ Built-in 128-word Font ROM: Basic ASCII、
Japanese、Numeric
- ◆ Support Max. 64Kbyte External Display SRAM
- ◆ Display Mode : Character、Graphics and Mixed Mode
- ◆ Font Size :
Horizontal → 5, 6, 7, 8 Pixels
Vertical → 8 Pixels
- ◆ Support Various LCD Driver
- ◆ Support 1/16 ~ 1/128 Duty
- ◆ Built-in X'tal Oscillator or Using External Clock
- ◆ Power Supply Range: 3.0~5.5V
- ◆ Package: LQFP-67Pin (RoHS Compliance)

3. Block Diagram



< Figure 3-1 >

4. Package



< Figure 4-1 >

RA6963L2NA : LQFP-67 Pin, RoHS Compliance Package, Font-01 (Refer to Chapter 6-16)
RA6963L2NB : LQFP-67 Pin, RoHS Compliance Package, Font-02 (Refer to Chapter 6-16)

5. Pin Descriptions

5-1 MPU Interface

< Table 5-1 >

| Pin Name | I/O | Description | | | | | | | | | |
|-------------------|-----------------------|---|-------------------|-----------------------|-----------------------|------|---------------|-------------|-----|------------|-----------|
| SD[7..0] | I/O | Data Bus This is bus for data transfer between MPU and RA6963. | | | | | | | | | |
| \overline{RD} | I | Read Control \overline{RD} is a data read signal. When Low, MPU read data from RA6963. | | | | | | | | | |
| \overline{WR} | I | Write Control \overline{WR} is a data write signal. When Low, MPU write data into RA6963. | | | | | | | | | |
| C/ \overline{D} | I | Command/Data Select or Register Select This is a Data or Command select signal. <table border="1"> <tr> <th>C/ \overline{D}</th><th>\overline{WR} = Low</th><th>\overline{RD} = Low</th></tr> <tr> <td>High</td><td>Command Write</td><td>Status Read</td></tr> <tr> <td>Low</td><td>Data Write</td><td>Data Read</td></tr> </table> | C/ \overline{D} | \overline{WR} = Low | \overline{RD} = Low | High | Command Write | Status Read | Low | Data Write | Data Read |
| C/ \overline{D} | \overline{WR} = Low | \overline{RD} = Low | | | | | | | | | |
| High | Command Write | Status Read | | | | | | | | | |
| Low | Data Write | Data Read | | | | | | | | | |
| \overline{CE} | I | Chip Enable This s chip enable of RA6963. When MPU communicate with RA6963, this pin must be Low. | | | | | | | | | |

5-2 LCD Driver Interface

< Table 5-2 >

| Pin Name | I/O | Description |
|----------|-----|--|
| FR | O | Frame |
| LP | O | Latch Latch pulse for column driver. Shift clock pulse for Row Driver |
| CDATA | O | Synchronous Data Synchronous Data for Row Driver. |
| HSCP | O | Shift Clock Pulse Shift clock pulse for Column Driver in upper area of LCD. |
| HOD | O | Data Output Data output for Odd Columns in upper area of LCD. |
| ED | O | Data Output SDSEL = High → Data output for even columns in both upper and lower area of LCD. SDSEL = Low → Data output for columns in both upper and lower area of LCD. |
| DSPON | O | Display On Display On/Off control signal. When $\overline{\text{HALT}}$ or $\overline{\text{RST}}$ is Low, DSPON output Low (LCD Display Off). |

5-3 Memory Interface

< Table 5-3 >

| Pin Name | I/O | Description |
|---------------------------------|-----|---|
| A[15:0] | O | Address Output for External Memory |
| D[7:0] | I/O | Data Bus for External Memory |
| $\overline{\text{MCE}}$ | O | Memory Chip Enable $\overline{\text{MCE}}$ = Low → Memory Enable. $\overline{\text{MCE}}$ = High → Memory Disable. |
| MRW | O | Memory Read/Write Control MRW = Low → Memory Write Enable. MRW = High → Memory Read Enable. |
| $\overline{\text{CE0}}$ LOD | O | Memory Chip Enable 0 If $\overline{\text{DUAL}}$ = High → Chip enable pin for display memory in the address range 0000~07FFh. If $\overline{\text{DUAL}}$ = Low → Serial data output for odd columns in lower area of LCD. |
| $\overline{\text{CE1}}$ LSCP | O | Memory Chip Enable 1 If $\overline{\text{DUAL}}$ = High → Chip enable pin for display memory in the address range 0800~0FFFh. If $\overline{\text{DUAL}}$ = Low → Shift clock output for Column Driver in lower area of LCD. |
| VDD | P | Power |
| GND | P | Ground |

5-4 Misc. Interface

< Table 5-4 >

| Pin Name | I/O | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|-------|---|--------------------------|-------|-----|-----|-----|-----|---|---|---|-----|---------|-------|-------|-------|-------|---|---|---|-----|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|-------|---|---|---|---|----|----|----|----|--------|----|----|----|----|----|----|-----|-----|--------------------------|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|-------|---|---|----|----|----|----|----|----|--------|----|----|----|-----|-----|-----|-----|-----|
| $\overline{\text{DUAL}}$ | I | Scan Select $\overline{\text{DUAL}}$ = Low → Dual-Scan Mode. $\overline{\text{DUAL}}$ = High → Signal-Scan Mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MDS MD[1:0] | I | LCD Size Selection One Screen <table><tr><td>$\overline{\text{DUAL}}$</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr><tr><td>MDS</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr><tr><td>MD1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>MD0</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>Lines</td><td>2</td><td>4</td><td>6</td><td>8</td><td>10</td><td>12</td><td>14</td><td>16</td></tr><tr><td>V-Dots</td><td>16</td><td>32</td><td>48</td><td>64</td><td>80</td><td>96</td><td>112</td><td>128</td></tr></table> Two Screens <table><tr><td>$\overline{\text{DUAL}}$</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr><tr><td>MDS</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr><tr><td>MD1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>MD0</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>Lines</td><td>4</td><td>8</td><td>12</td><td>16</td><td>20</td><td>24</td><td>28</td><td>32</td></tr><tr><td>V-Dots</td><td>32</td><td>64</td><td>96</td><td>128</td><td>160</td><td>192</td><td>224</td><td>256</td></tr></table> | $\overline{\text{DUAL}}$ | H | H | H | H | H | H | H | H | MDS | L | L | L | L | H | H | H | H | MD1 | H | H | L | L | H | H | L | L | MD0 | H | L | H | L | H | L | H | L | Lines | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | V-Dots | 16 | 32 | 48 | 64 | 80 | 96 | 112 | 128 | $\overline{\text{DUAL}}$ | L | L | L | L | L | L | L | L | MDS | L | L | L | L | H | H | H | H | MD1 | H | H | L | L | H | H | L | L | MD0 | H | L | H | L | H | L | H | L | Lines | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | V-Dots | 32 | 64 | 96 | 128 | 160 | 192 | 224 | 256 |
| $\overline{\text{DUAL}}$ | H | H | H | H | H | H | H | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MDS | L | L | L | L | H | H | H | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD1 | H | H | L | L | H | H | L | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD0 | H | L | H | L | H | L | H | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Lines | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V-Dots | 16 | 32 | 48 | 64 | 80 | 96 | 112 | 128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{DUAL}}$ | L | L | L | L | L | L | L | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MDS | L | L | L | L | H | H | H | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD1 | H | H | L | L | H | H | L | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD0 | H | L | H | L | H | L | H | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Lines | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V-Dots | 32 | 64 | 96 | 128 | 160 | 192 | 224 | 256 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X1 | I | Crystal Oscillator Input A crystal / ceramic oscillator circuit is built in. The oscillation frequency is adjusted according to the display size. If using an external clock, use the X1 pin as the clock input. (X2 open.) External capacitors 15 to 20pF for Crystal or Ceramic oscillator. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X2 | O | Crystal Oscillator Output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FS[1:0] | I | Font Selection <table><tr><td>FS0</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>FS1</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>Font</td><td>5 X 8</td><td>6 X 8</td><td>7 X 8</td><td>8 X 8</td></tr></table> | FS0 | H | L | H | L | FS1 | H | H | L | L | Font | 5 X 8 | 6 X 8 | 7 X 8 | 8 X 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FS0 | H | L | H | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FS1 | H | H | L | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Font | 5 X 8 | 6 X 8 | 7 X 8 | 8 X 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD[3:2] | I | Columns Selection <table><tr><td>MD2</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>MD3</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>Columns</td><td>32</td><td>40</td><td>64</td><td>80</td></tr></table> | MD2 | H | L | H | L | MD3 | H | H | L | L | Columns | 32 | 40 | 64 | 80 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD2 | H | L | H | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MD3 | H | H | L | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Columns | 32 | 40 | 64 | 80 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{SDSEL}}$ | I | Data Transfer Mode $\overline{\text{SDSEL}}$ = Low → Sending data by simple serial mode. $\overline{\text{SDSEL}}$ = High → Sending data by odd/even separation mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Pin Name | I/O | Description |
|-------------------------------|-----|---|
| $\overline{\text{HALT}}$ | I | Halt Signal $\overline{\text{HALT}}$ = Low → Stop the Clock. $\overline{\text{HALT}}$ = High → Normal Mode. |
| $\overline{\text{RST}}$ | I | Reset Signal $\overline{\text{RST}}$ = Low → RA6963 will be reset. $\overline{\text{RST}}$ = High → Normal mode. RA6963 built-in a Pull-Hi resistor. |
| $\overline{\text{TEST}}[2:1]$ | I | Test Pins These are test pins. No need for connection(NC). |
| CH1, CH2 | O | Check Signals |

6. Functions Description

6-1 Functional Definition

- ◆ After power on, it is necessary to reset. The $\overline{\text{RST}}$ is kept Low between 5 clocks up (oscillation clock).
- ◆ When $\overline{\text{HALT}}$ = Low, the oscillation stops. The power supply for the LCD must be turned off, to protect the LCD from DC bias.
- ◆ The HALT function($\overline{\text{HALT}}$ = Low) includes the RESET function($\overline{\text{RST}}$ = Low).
- ◆ The column/line counter and display register are cleared by $\overline{\text{RST}}$. (Other registers are not cleared.) Disable the display using the clear-display register
- ◆ The status must be checked before data or commands are sent. The MSB=0 status check must be done in particular. There is a possibility of erroneous operation due to a hard interrupt.
- ◆ STA0 and STA1 must be checked at the same time. When a command is executed, data transmission errors may occur.
- ◆ The RA6963 can only handle one byte per machine cycle (16 clocks). It is impossible to send more than two data in a machine cycle.
- ◆ When using a command with operand data, it important to send the data first, and then executes the command.
- ◆ The character fonts used by the RA6963 are different from ASCII codes.

6-2 State After RESET/HALT

< Table 6-1 >

| Pins | HALT | RESET |
|-----------|-------------|-------------|
| SD[7:0] | Floating | Floating |
| D[7:0] | Floating | Floating |
| MRW | Hi | Hi |
| MCE | Hi (Note 1) | Hi (Note 1) |
| A[15:0] | Hi (Note 2) | Hi (Note 2) |
| CE0 , CE1 | Hi (Note 1) | Hi (Note 1) |
| ED, HOD | Final data | Final data |
| HSCP | Low | Low |
| LP | Low | Low |
| CDATA | Low | Low |
| FR | Hi | Hi |
| CH1 | Low | Test Signal |
| CH2 | Low | Test Signal |
| DSPON | Low | Low |
| X2 | Hi | OSC Clock |

Note 1 : In Attribute mode, Hi or Low according to state of graphic pointer

Note 2 : In Attribute mode, data to graphic pointer

6-3 Row / Column and Oscillation Clock

The frequency of the crystal oscillator is adjusted by the following formula.

- f_{OSC} : Frequency of oscillation
 f_{SCP} : Frequency of shift clock ($f_{SCP} = f_{OSC} / 2$)
 f_R : Frequency of Frame
M : Number of characters on one line (number of dots on one line 8M)
 For all font sizes (e.g. 7 x 8, 7 x 8, 5 x 8) the oscillation frequency remains constant.
N : Number of rows (Duty=1/8N)

$$\frac{8M}{f_{SCP}} \times 8N = \frac{1}{f_R}$$

$$f_{OSC} = f_R \times 64 \times 2 \times M \times N$$

($f_R = 60\text{Hz}$)

< Table 6-2 >

Unit: MHz

| N \ M | | 32 | 40 | 64 | 80 | Duty |
|-------|-------|-------|-------|--------|--------|-------|
| 2 | Upper | 0.492 | 0.614 | 0.983 | 1.229 | 1/16 |
| | Lower | 0.983 | 1.229 | 1.966 | 2.458 | |
| 4 | Upper | 0.983 | 1.229 | 1.966 | 2.458 | 1/32 |
| | Lower | 1.966 | 2.458 | 3.932 | 4.915 | |
| 6 | Upper | 1.475 | 1.843 | 2.949 | 3.688 | 1/48 |
| | Lower | 2.949 | 3.688 | 5.898 | 7.372 | |
| 8 | Upper | 1.966 | 2.458 | 3.932 | 4.915 | 1/64 |
| | Lower | 3.932 | 4.915 | 7.864 | 9.830 | |
| 10 | Upper | 2.458 | 3.072 | 4.915 | 6.144 | 1/80 |
| | Lower | 4.915 | 6.144 | 9.830 | 12.288 | |
| 12 | Upper | 2.949 | 3.686 | 5.898 | 7.373 | 1/96 |
| | Lower | 5.898 | 7.373 | 11.776 | 14.746 | |
| 14 | Upper | 3.440 | 4.300 | 6.881 | 8.602 | 1/112 |
| | Lower | 6.881 | 8.601 | 13.763 | 17.203 | |
| 16 | Upper | 3.932 | 4.915 | 7.864 | 9.830 | 1/128 |
| | Lower | 7.864 | 9.830 | 15.729 | 19.660 | |

Note 1: Upper → Single-Scan. Lower → Dual-Scan at $f_R = 60\text{Hz}$

6-4 RAM Interface

The external RAM is used to store display data (text, graphic and external CG data).

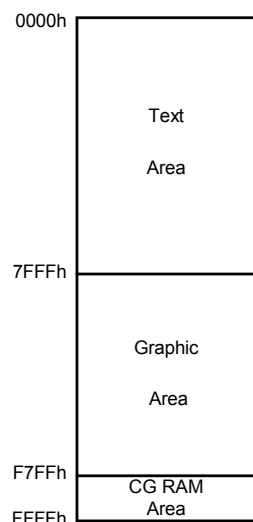
With single-scan, text data, graphic data and external CG data can be freely allocated to the memory area (64 KB max).

With dual-scan, LCD-I is allocated to 0000h to 7FFFh (32 KB max), LCD-II is allocated to 8000h to FFFFh (32-KB Max). Text data, graphic data and external CG data can be freely allocated in LCD-I. In LCD-II, the same addresses must be allocated as in LCD-I, except A15. A15 determines selection of LCD-I or LCD-II.

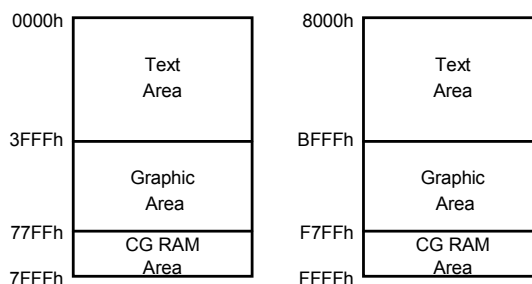
It can be used the address-decoded signals $\overline{CE0}$ (0000h to 07FFh), $\overline{CE1}$ (0800h to 0FFFh) within 4 KB. $\overline{CE0}$ and $\overline{CE1}$ allow decoding of addresses in the ranges (0000h to 07FFh) and (0800h to 0FFFh) respectively within a 4-KB memory space.

(Example)

(1) Single-Scan



(2) Dual-Scan



< Figure 6-1 >

6-5 Communications with MPU

6-5-1 Status Read

A status check must be performed before data is read or written.

Status Check

The Status of RA6963 can be read from the data lines.

< Table 6-3 >

| \overline{RD} | \overline{WR} | \overline{CS} | C/\overline{D} | SD[7:0] |
|-----------------|-----------------|-----------------|------------------|-------------|
| L | H | L | H | Status Word |

The RA6963 status word format is as follows:

| MSB | | | | LSB | | | |
|------|------|------|------|------|------|------|------|
| SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |
| STA7 | STA6 | STA5 | STA4 | STA3 | STA2 | STA1 | STA0 |

< Table 6-4 >

| | | |
|------|--|-------------------------------------|
| STA0 | Check command execution capability | 0: Disable 1: Enable |
| STA1 | Check data read/write capability | 0: Disable 1: Enable |
| STA2 | Check Auto mode data read capability | 0: Disable 1: Enable |
| STA3 | Check Auto mode data write capability | 0: Disable 1: Enable |
| STA4 | Not used | |
| STA5 | Check controller operation capability | 0: Disable 1: Enable |
| STA6 | Error flag. Used for Screen copy commands. | 0: No error 1: Error |
| STA7 | Check the blink condition | 0: Display off 1: Normal display |

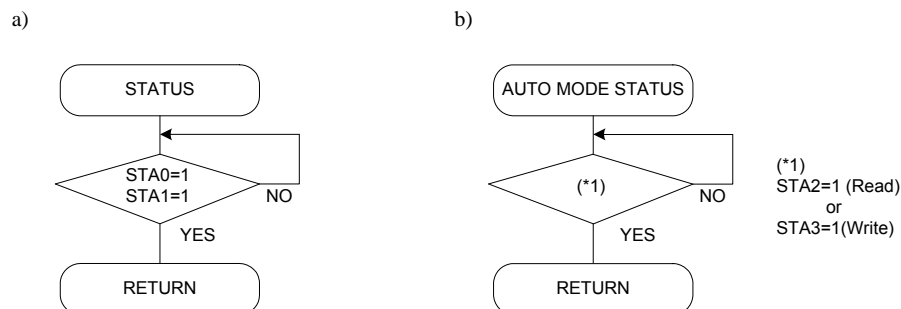
Note 1: It is necessary to check STA0 and STA1 at the same time.

There is a possibility of erroneous operation due to a hardware interrupt.

Note 2: For most modes STA0 /STA1 are used as a status check.

Note 3: STA2 and STA3 are valid in Auto mode; STA0 and STA1 are invalid.

Status Checking Flow



< Figure 6-2 >

Note 4: When using the MSB=0 command, a Status Read must be performed.

If a status check is not carried out, the RA6963 cannot operate normally, even after a delay time.

The hardware interrupt occurs during the address calculation period (at the end of each line).

If a MSB=0 command is sent to the RA6963 during this period, the RA6963 enters Wait status.

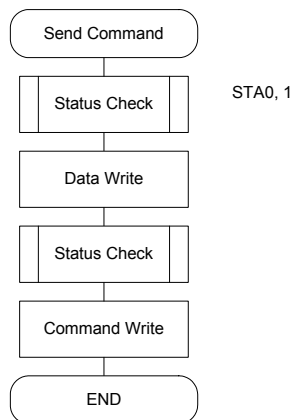
If a status check is not carried out in this state before the next command is sent, there is the possibility that the command or data will not be received.

6-5-2 Setting Data

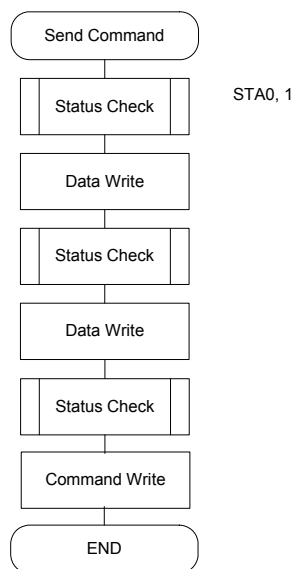
When using the RA6963, first set the data, then set the command.

Procedure for Sending a Command

a) The case of 1 data



b) The case of 2 data



< Figure 6-3 >

Note : When sending more than two data, the last datum (or last two data) is valid.

6-5-3 Command Definitions

< Table 6-5 >

| Command | Code | D1 | D2 | Function |
|------------------------------|----------|-------------|--------------|---------------------------------|
| Registers Setting | 00100001 | X address | Y address | Set cursor pointer |
| | 00100010 | Data | 00h | Set Offset Register |
| | 00100100 | Low address | High address | Set Address pointer |
| Set Control Word | 01000000 | Low address | High address | Set Text Home Address |
| | 01000001 | Columns | 00h | Set Text Area |
| | 01000010 | Low address | High address | Set Graphic Home Address |
| | 01000011 | Columns | 00h | Set Graphic Area |
| Mode Set | 1000X000 | -- | -- | OR mode |
| | 1000X001 | -- | -- | EXOR mode |
| | 1000X011 | -- | -- | AND mode |
| | 1000X100 | -- | -- | Text Attribute mode |
| | 10000XXX | -- | -- | Internal CG ROM mode |
| | 10001XXX | -- | -- | External CG RAM mode |
| Display Mode | 10010000 | -- | -- | Display off |
| | 1001XX10 | -- | -- | Cursor on, blink off |
| | 1001XX11 | -- | -- | Cursor on, blink on |
| | 100101XX | -- | -- | Text on, graphic off |
| | 100110XX | -- | -- | Text off, graphic on |
| | 100111XX | -- | -- | Text on, graphic on |
| Cursor Pattern Select | 10100000 | -- | -- | 1-line cursor |
| | 10100001 | -- | -- | 2-line cursor |
| | 10100010 | -- | -- | 3-line cursor |
| | 10100011 | -- | -- | 4-line cursor |
| | 10100100 | -- | -- | 5-line cursor |
| | 10100101 | -- | -- | 6-line cursor |
| | 10100110 | -- | -- | 7-line cursor |
| | 10100111 | -- | -- | 8-line cursor |
| Data auto Read/Write | 10110000 | -- | -- | Set Data Auto Write |
| | 10110001 | -- | -- | Set Data Auto Read |
| | 10110010 | -- | -- | Auto Reset |
| Data Read/Write | 11000000 | Data | -- | Data Write and Increment ADP |
| | 11000001 | -- | -- | Data Read and Increment ADP |
| | 11000010 | Data | -- | Data Write and Decrement ADP |
| | 11000011 | -- | -- | Data Read and Decrement ADP |
| | 11000100 | Data | -- | Data Write and Non-variable ADP |
| | 11000101 | -- | -- | Data Read and Non-variable ADP |
| Screen Peek | 11100000 | -- | -- | Screen Peek |
| Screen Copy | 11101000 | | | Screen Copy |
| Bit Set/Reset | 11110XXX | -- | -- | Bit Reset |
| | 11111XXX | -- | -- | Bit Set |
| | 1111X000 | -- | -- | Bit 0 (LSB) |
| | 1111X001 | -- | -- | Bit 1 |
| | 1111X010 | -- | -- | Bit 2 |
| | 1111X011 | -- | -- | Bit 3 |
| | 1111X100 | -- | -- | Bit 4 |
| | 1111X101 | -- | -- | Bit 5 |
| | 1111X110 | -- | -- | Bit 6 |
| | 1111X111 | -- | -- | Bit 7 (MSB) |

6-6 Setting Registers

< Table 6-6 >

| Code | Hex. | Function | D1 | D2 |
|----------|------|---------------------|----------|-----------|
| 00100001 | 21h | Set Cursor Pointer | X-Adrs | Y-Adrs |
| 00100010 | 22h | Set Offset Register | Data | 00h |
| 00100100 | 24h | Set Address Pointer | Low Adrs | High Adrs |

6-6-1 Set Cursor Pointer

The X-Adrs and Y-Adrs specify the position of the cursor. The cursor position can only be moved by this command. Data read /write from the MPU never changes the cursor pointer. X-Adrs and Y-Adrs are specified as follows.

X-Adrs 00h to 4Fh (lower 7 bits are valid)
Y-Adrs 00h to 1Fh (lower 5 bits are valid)

a) Single-Scan
X-Adrs 00h to 4Fh

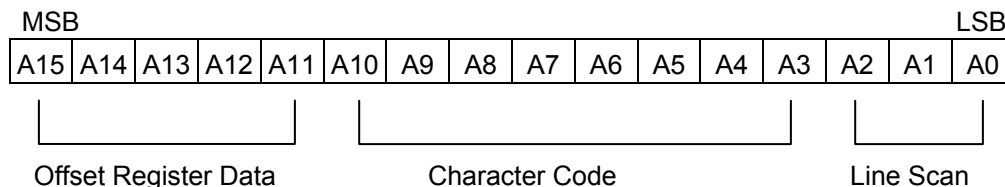
| |
|-------------------|
| Y-Adrs 00h to 0Fh |
|-------------------|

b) Dual-Scan
X-Adrs 00h to 4Fh

| |
|-----------------------------------|
| Y-Adrs 00h to 0Fh Upper Screen |
| Y-Adrs 10h to 1Fh Lower Screen |

6-6-2 Set Offset Register

The offset register is used to determine the external character generator RAM area. The RA6963 has a 16-bit address bus as follows:



RA6963 assign External character generator, when character code set 80h to FFh in using Internal character generator. Character code 00h to 80h assign External character generator, when External generator mode.

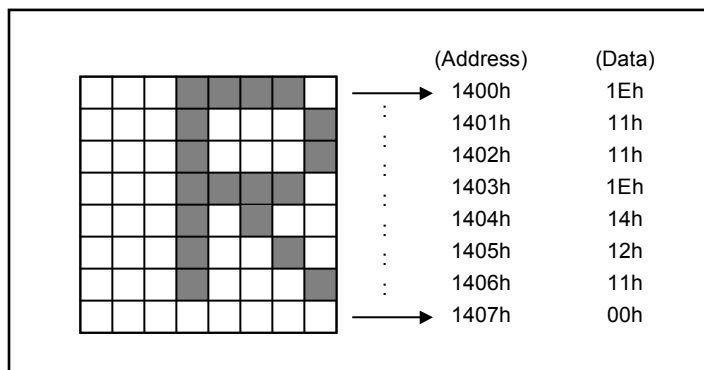
The senior five bits define the start address in external memory of the CG RAM area. The next eight bits represent the character code of the character. In internal CG ROM mode, character Codes 00h to 7Fh represent the predefined "internal" CG ROM characters, and codes 80h to FFh Represent the user's own "external" characters. In external CG RAM mode, all 256 codes from 00h to FFh can be used to represent the user's own characters. The three least significant bits indicate one of the eight rows of eight dots that define the character's shape.

The Relationship between Display RAM Address and Offset Register

| Offset Register Data | CG RAM hex. Address (Start to End) |
|----------------------|------------------------------------|
| 00000 | 0000 to 07FFh |
| 00001 | 0800 to 0FFFh |
| 00010 | 1000 to 17FFh |
| | |
| 11100 | E000 to E7FFh |
| 11101 | E800 to EFFFh |
| 11110 | F000 to F7FFh |
| 11111 | F800 to FFFFh |

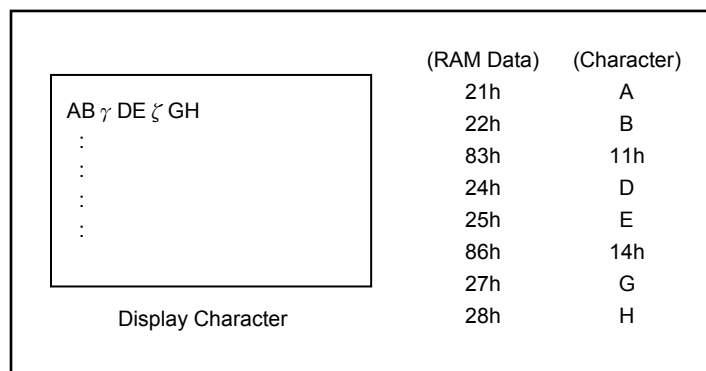
(Example 1)

| | | | | | |
|---------------------------------------|------|------|------|------|---|
| Offset Register | 02h | | | | |
| Character Code | 80h | | | | |
| Character Generator RAM Start Address | 0001 | 0100 | 0000 | 0000 | |
| | 1 | 4 | 0 | 0 | h |



< Figure 6-4 >

(Example 2) The relationship between Display RAM data and display characters



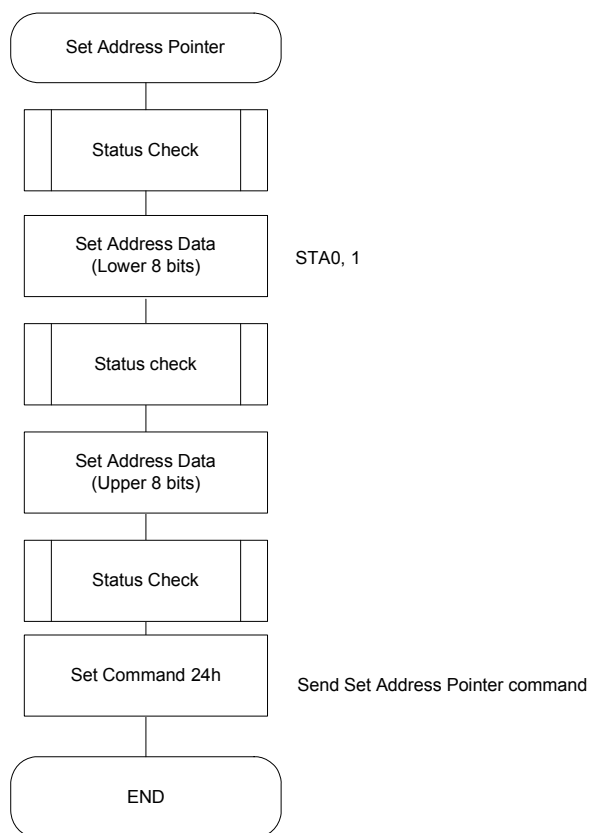
< Figure 6-5 >

The “γ” and “ζ” are displayed by character generator RAM.

6-6-3 Set Address Pointer

The Set Address Pointer command is used to indicate the start address for writing to (or reading from) External RAM.

The Flowchart for Set Address Pointer Command



< Figure 6-6 >

6-7 Set Control Word

< Table 6-7 >

| Code | Hex. | Function | D1 | D2 |
|----------|------|--------------------------|-------------|--------------|
| 01000000 | 40h | Set Text Home Address | Low Address | High Address |
| 01000001 | 41h | Set Text Area | Columns | 00h |
| 01000010 | 42h | Set Graphic Home Address | Low Address | High Address |
| 01000011 | 43h | Set Graphic Area | Columns | 00h |

The home address and column size are defined by this command.

6-7-1 Set Text Home Address

The starting address in the external display RAM for text display is defined by this command. The text home address indicates the leftmost and uppermost position.

The Relationship between Display RAM Address and Display Position

< Table 6-8 >

| | | |
|-----------------|-------|--------------------|
| TH | | TH + CL |
| TH + TA | | TH + TA + CL |
| (TH + TA) + TA | | TH + 2TA + CL |
| (TH + 2TA) + TA | | TH + 3TA + CL |
| ⋮ | ⋮ | ⋮ |
| TH + (n-1) TA | | TH + (n-1) TA + CL |

TH: Text home address

TA: Text area number (columns)

CL: Columns are fixed by hardware (pin-programmable).

(Example)

| | |
|------------------------------|--------------|
| Text Home Address | : 0000h |
| Text Area | : 0020h |
| MD2=H, MD3=H | : 32 Columns |
| DUAL =H, MDS=L, MD0=L, MD1=H | : 4 Lines |

< Table 6-9 >

| | | | | |
|-------|-------|-------|-------|-------|
| 0000h | 0001h | | 001Eh | 001Fh |
| 0020h | 0021h | | 003Eh | 002Fh |
| 0040h | 0041h | | 005Eh | 005Fh |
| 0060h | 0061h | | 007Eh | 007Fh |

6-7-2 Set Graphic Home Address

The starting address of the external display RAM used for graphic display is defined by this command. The graphic home address indicates the leftmost and uppermost position.

The Relationship between External Display RAM Address and Display Position

< Table 6-10 >

| | | |
|-----------------|-------|--------------------|
| GH | | GH + CL |
| GH + GA | | GH + GA + CL |
| (GH + GA) + GA | | GH + 2GA + CL |
| (GH + 2GA) + GA | | GH + 3GA + CL |
| ⋮ | ⋮ | ⋮ |
| GH + (n-1) GA | | GH + (n-1) GA + CL |

GH: Graphic Home Address

GA: Graphic Area Number (columns)

CL: Columns are fixed by hardware (pin-programmable).

(Example)

| | |
|-----------------------------|--------------|
| Graphic Home Address | : 0000h |
| Graphic Area | : 0020h |
| MD2=H, MD3=H | : 32 columns |
| DUAL=H, MDS=L, MD0=H, MD1=H | : 2 lines |

< Table 6-11 >

| | | | | |
|-------|-------|-------|-------|-------|
| 0000h | 0001h | | 001Eh | 001Fh |
| 0020h | 0021h | | 003Eh | 003Fh |
| 0040h | 0041h | | 005Eh | 005Fh |
| 0060h | 0061h | | 007Eh | 007Fh |
| 0080h | 0081h | | 009Eh | 009Fh |
| 00A0h | 00A1h | | 00BEh | 00BFh |
| 00C0h | 00C1h | | 00DEh | 00DFh |
| 00E0h | 00E1h | | 00FEh | 00FFh |
| 0100h | 0101h | | 011Eh | 011Fh |
| 0120h | 0121h | | 013Eh | 013Fh |
| 0140h | 0141h | | 015Eh | 015Fh |
| 0160h | 0161h | | 017Eh | 017Fh |
| 0180h | 0181h | | 019Eh | 019Fh |
| 01A0h | 01A1h | | 01BEh | 01BFh |
| 01C0h | 01C1h | | 01DEh | 01DFh |
| 01E0h | 01E1h | | 01FEh | 01FFh |

6-7-3 Set Text Area

The display columns are defined by the hardware setting. This command can be used adjust the columns of the display.

(Example)

LCD Size : 20 columns, 4 lines
Text Home Address : 0000h
Text Area : 0014h
MD2=H, MD3=H : 32 columns
DUAL =H , MDS =L, MD0= L, MD1=H : 4 lines

< Table 6-12 >

| | | | | | | |
|------|------|-------|------|------|-------|------|
| 0000 | 0001 | | 0013 | 0014 | | 001F |
| 0014 | 0015 | | 0027 | 0028 | | 0033 |
| 0028 | 0029 | | 003B | 003C | | 0047 |
| 003C | 003D | | 004F | 0050 | | 005B |



6-7-4 Set Graphic Area

The display columns are defined by the hardware setting. This command can be used to adjust the columns of the graphic display.

(Example)

LCD Size : 20 columns, 2 lines
 Graphic Home Address : 0000h
 Graphic Area : 0014h
 MD2=H, MD3=H : 32 columns
 $\overline{\text{DUAL}}$ =H, MDS=L MD0=H, MD1=H : 2 lines

< Table 6-13 >

| | | | | | | |
|------|------|-------|------|------|-------|------|
| 0000 | 0001 | | 0013 | 0014 | | 001F |
| 0014 | 0015 | | 0027 | 0028 | | 0033 |
| 0028 | 0029 | | 003B | 003C | | 0047 |
| 003C | 003D | | 004F | 0050 | | 005B |
| 0050 | 0051 | | 0063 | 0064 | | 006F |
| 0064 | 0065 | | 0077 | 0078 | | 0083 |
| 0078 | 0079 | | 008B | 008C | | 0097 |
| 008C | 008D | | 009F | 00A0 | | 00AB |
| 00A0 | 00A1 | | 00B3 | 00B4 | | 00BF |
| 00B4 | 00B5 | | 00C7 | 00C8 | | 00D3 |
| 00C8 | 00C9 | | 00DB | 00DC | | 00E7 |
| 00DC | 00DD | | 00EF | 00F0 | | 00FD |
| 00F0 | 00F1 | | 0103 | 0104 | | 011F |
| 0104 | 0105 | | 0127 | 0128 | | 0123 |
| 0128 | 0129 | | 013B | 013C | | 0147 |
| 013C | 013D | | 014F | 0150 | | 015B |



If the graphic area setting is set to match the desired number of columns on the LCD, the addressing scheme will be automatically modified so that the start address of each line equals the end address of the previous line +1.

6-8 Mode Set

< Table 6-14 >

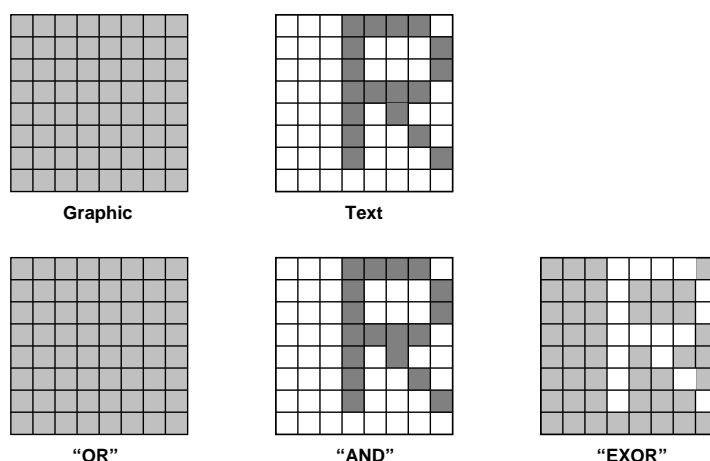
| Code | Function | Operand |
|----------|-----------------------------------|---------|
| 1000X000 | OR Mode | — |
| 1000X001 | EXOR Mode | — |
| 1000X011 | AND Mode | — |
| 1000X100 | Text Attribute Mode | — |
| 10000XXX | Internal Character Generator Mode | — |
| 10001XXX | External Character Generator Mode | — |

X: Invalid

The display mode is defined by this command. The display mode does not change until the next command is sent. The logical OR, EXOR, AND of text or graphic display can be displayed.

In internal Character Generator mode, character codes 00h to 7Fh are assigned to the built-in Character generator ROM. The character codes 80h to FFh are automatically assigned to the external character generator RAM.

(Example)



< Figure 6-7 >

Note: Attribute functions can only be applied to text display, since the attribute data is placed in the graphic RAM area.

Attribute Function

The attribute operations are Reverse display, Character blink, bold and Inhibit. The attribute data is written into the graphic area, which was defined by the Set Control word command. Only text display is possible in Attribute Function mode; graphic display is automatically disabled. However, the Display Mode command must be used to turn both Text and Graphic on that in order to for the Attribute function available.

The attribute data for each character in the text area is written to the same address in the graphic area.

The Attribute function is defined as follows.

Attribute RAM 1byte

| | | | | | | | |
|---|---|---|---|----|----|----|----|
| X | X | X | X | d3 | d2 | d1 | d0 |
|---|---|---|---|----|----|----|----|

X: Invalid

< Table 6-15 >

| d3 | d2 | d1 | d0 | Function |
|----|----|----|----|--------------------------|
| 0 | 0 | 0 | 0 | Normal Display |
| 0 | 1 | 0 | 1 | Reverse Display |
| 0 | 0 | 1 | 1 | Inhibit Display |
| 1 | 0 | 0 | 0 | Blink of Normal Display |
| 1 | 1 | 0 | 1 | Blink of Reverse Display |
| 1 | 0 | 1 | 1 | Blink of Inhibit Display |

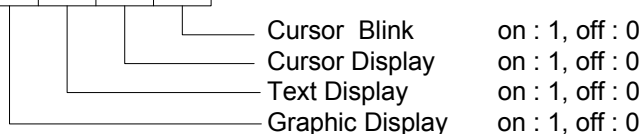
6-9 Display Mode

< Table 6-16 >

| Code | Function | Operand |
|----------|----------------------|---------|
| 10010000 | Display off | — |
| 1001XX10 | Cursor on, Blink off | — |
| 1001XX11 | Cursor on, Blink on | — |
| 100101XX | Text on, Graphic off | — |
| 100110XX | Text off, Graphic on | — |
| 100111XX | Text on, Graphic on | — |

X: Invalid

| | | | | | | | |
|---|---|---|---|----|----|----|----|
| 1 | 0 | 0 | 1 | D3 | D2 | D1 | D0 |
|---|---|---|---|----|----|----|----|



Note: It is necessary to turn on “Text Display” and “Graphic Display” in the following cases.

- Combination of text /graphic display
- Attribute function

6-10 Cursor Pattern Select

< Table 6-17 >

| Code | Function | Operand |
|----------|---------------|---------|
| 10100000 | 1-line cursor | — |
| 10100001 | 2-line cursor | — |
| 10100010 | 3-line cursor | — |
| 10100011 | 4-line cursor | — |
| 10100100 | 5-line cursor | — |
| 10100101 | 6-line cursor | — |
| 10100110 | 7-line cursor | — |
| 10100111 | 8-line cursor | — |

When cursor display is ON, this command selects the cursor pattern in the range 1 line to 8 lines. The cursor address is defined by the Cursor Pointer Set command.

6-11 Data Auto Read/Write

< Table 6-18 >

| Code | Hex. | Function | Operand |
|----------|------|---------------------|---------|
| 10110000 | B0h | Set Data Auto Write | — |
| 10110001 | B1h | Set Data Auto Read | — |
| 10110010 | B2h | Auto Reset | — |

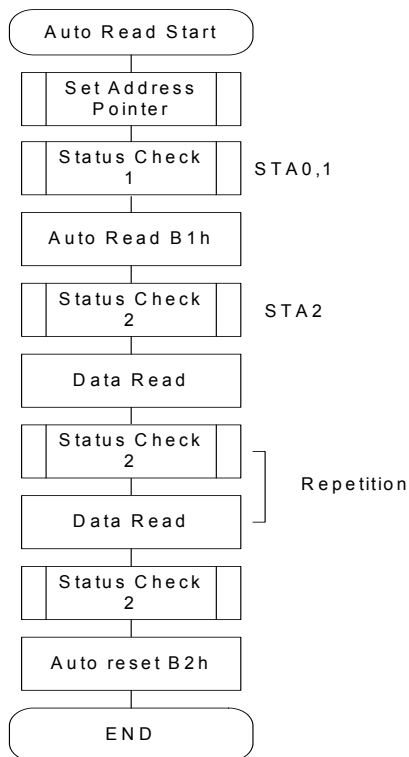
This command is convenient for sending a full screen of data from the external display RAM. After Setting Auto mode, a Data Write (or Read) command does not need sent between each datum. A Data Auto Write (or Read) command must be sent after a Set Address Pointer command. After this Command, the address pointer is automatically incremented by 1 after each datum. In Auto mode, the RA6963 cannot accept any other commands.

The Auto Reset command must be sent to the RA6963 after all data has been sent, to clear Auto Mode.

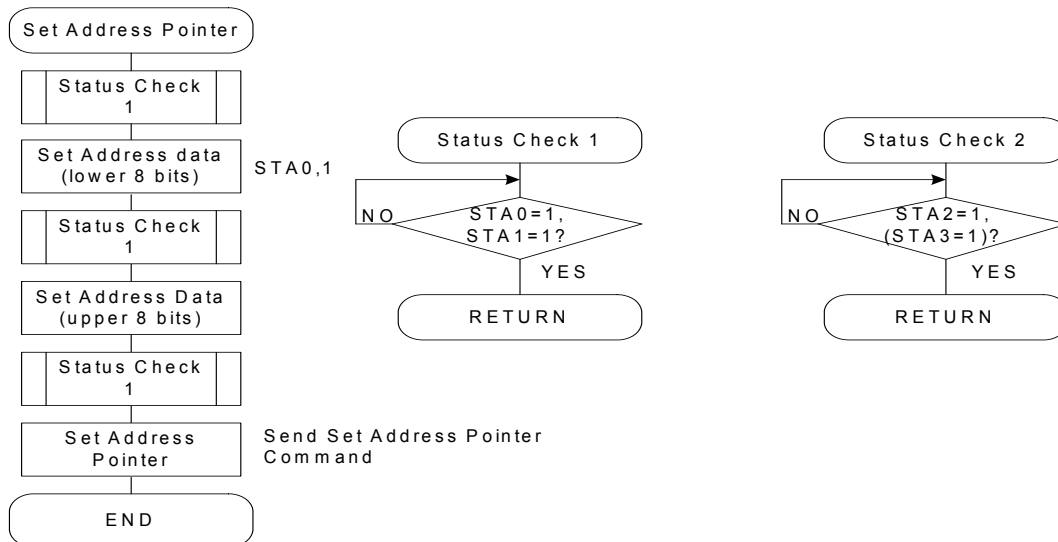
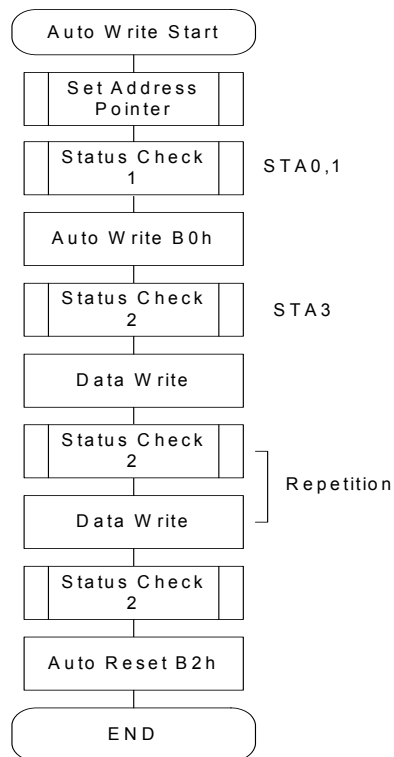
Note : A Status Check for Auto Mode

STA2, STA3 should be checked between sending of each datum. Auto Reset should be performed after checking STA3=1 (STA2=1). Refer to the following flowchart.

a) Auto Read mode



b) Auto Write mode



< Figure 6-8 >

6-12 Data Read/Write

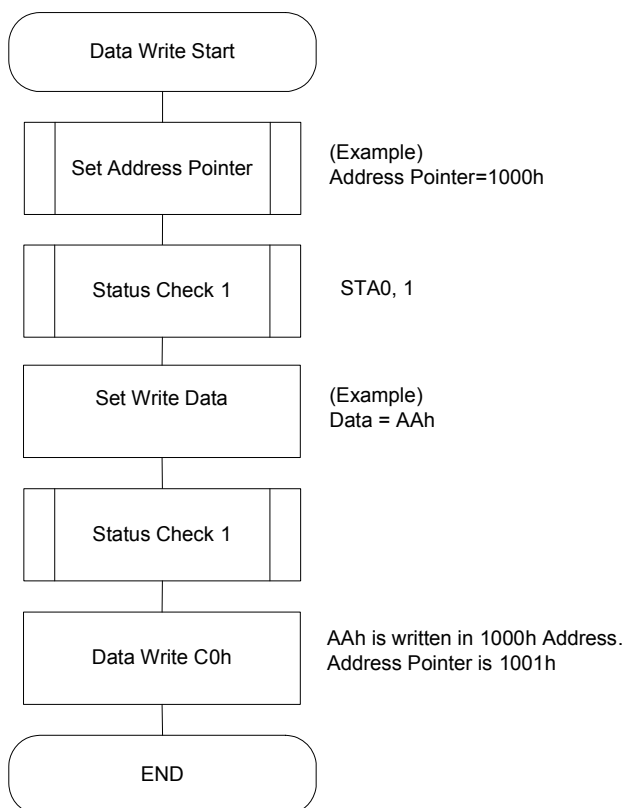
< Table 6-19 >

| Code | Hex. | Function | Operand |
|----------|------|---------------------------------|---------|
| 11000000 | C0h | Data Write and Increment ADP | Data |
| 11000001 | C1h | Data Read and Increment ADP | — |
| 11000010 | C2h | Data Write and Decrement ADP | Data |
| 11000011 | C3h | Data Write and Decrement ADP | — |
| 11000100 | C4h | Data Write and Non-variable ADP | Data |
| 11000101 | C5h | Data Read and Non-variable ADP | — |

This command is used for writing data from the MPU to external display RAM, and reading data from external display RAM to the MPU. Data Write / Data Read should be executed after setting address using Set Address Pointer command, The address pointer can be automatically incremented or decremented using this command.

Note: This command is necessary for each 1-byte datum.

Refer to the following flowchart.



< Figure 6-9 >

6-13 Screen Peek

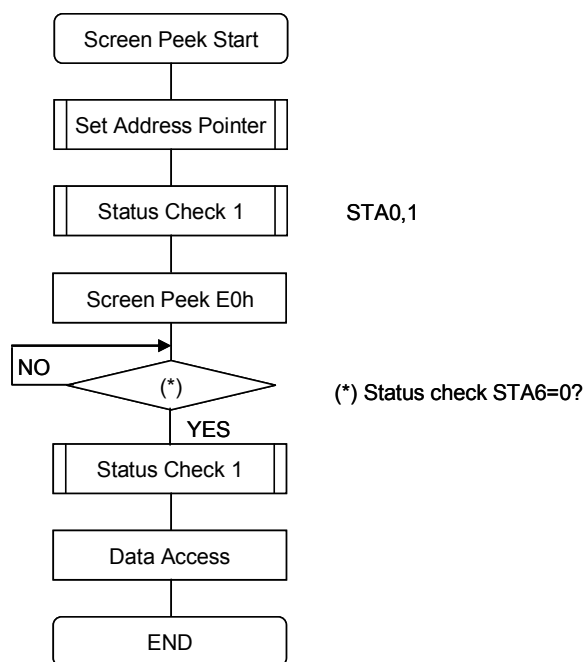
< Table 6-20 >

| Code | Hex. | Function | Operand |
|----------|------|-------------|---------|
| 11100000 | E0h | Screen Peek | — |

This command is used to transfer 1 byte of displayed data to the data stack; this byte can be read from the MPU by data access. The logical combination of text and graphic display data on the LCD screen can be read by this command.

The status (STA6) should be checked just after the Screen Peek command. If the address determined by the Set Address Pointer command is not in the graphic area, this command is ignored and a status flag (STA6) is set.

Refer to the following flowchart.



< Figure 6-10 >

Note: This command is available when hardware column number and software column number are the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

6-14 Screen Copy

< Table 6-21 >

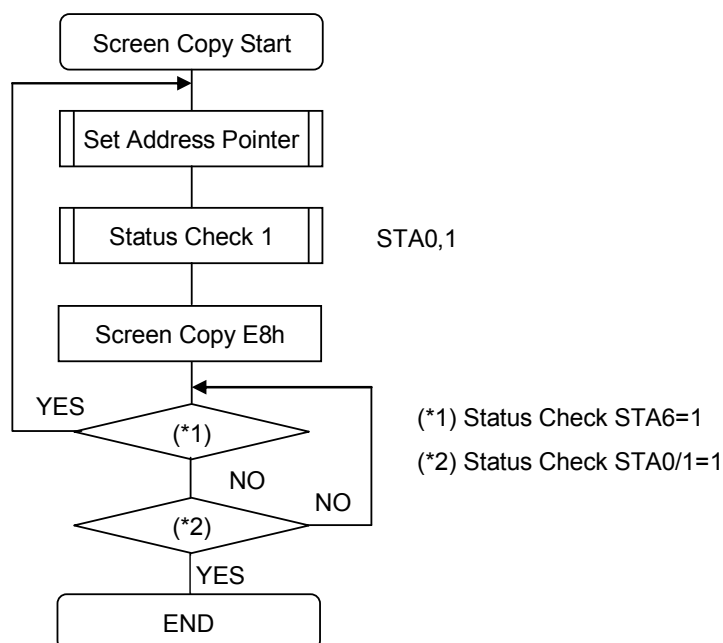
| Code | Hex. | Function | Operand |
|----------|------|-------------|---------|
| 11101000 | E8h | Screen Copy | — |

This command copies a single raster line of data to the graphic area.
The start point must be set using the Set Address Pointer command.

Note 1: If the attribute function is being used, this command is not available. (With Attribute data is graphic area data.)

Note 2: With Dual-Scan, this command cannot be used (because the RA6963 cannot separate the upper screen data and lower screen data).

Refer to the following flowchart.



< Figure 6-11 >

Note : This command is available when hardware column number and software column number are the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

6-15 Bit Set/Reset

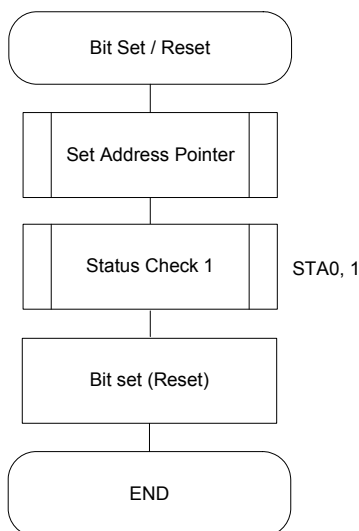
< Table 6-22 >

| Code | Function | Operand |
|----------|-------------|---------|
| 11110XXX | Bit Reset | — |
| 11111XXX | Bit Set | — |
| 1111X000 | Bit 0 (LSB) | — |
| 1111X001 | Bit 1 | — |
| 1111X010 | Bit 2 | — |
| 1111X011 | Bit 3 | — |
| 1111X100 | Bit 4 | — |
| 1111X101 | Bit 5 | — |
| 1111X110 | Bit 6 | — |
| 1111X111 | Bit 7 (MSB) | — |

X: Invalid

This command used to set or reset a bit of the byte specified by the address pointer. Only one bit can be set / reset at time.

Refer to following flowchart.



< Figure 6-12 >

6-16 Character Font Map

CGROM Font - 01

| LSB \ MSB | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|-----------|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / |
| 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 2 | a | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 3 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| 4 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 5 | p | q | r | s | t | u | v | w | x | y | z | { | | } | ~ | |
| 6 | Q | ü | ë | ä | å | ä | ä | ö | ë | ë | ë | i | i | i | Ä | ä |
| 7 | E | æ | Æ | ö | ö | ö | ö | ö | ö | ö | ö | ö | ö | ö | ö | f |

< Figure 6-13 >

CGROM Font - 02

| LSB \ MSB | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|-----------|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / |
| 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 2 | a | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 3 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| 4 | 千 | 万 | 月 | 夕 | 夕 | ■ | ヲ | ア | イ | ウ | エ | オ | カ | ユ | ヨ | ツ |
| 5 | 一 | ア | イ | ウ | エ | オ | カ | キ | ク | ケ | コ | サ | シ | ス | セ | ソ |
| 6 | タ | チ | ツ | テ | ト | ナ | ニ | ヌ | ネ | ノ | ハ | ヒ | フ | ヘ | ホ | マ |
| 7 | ミ | ム | メ | モ | ヤ | ユ | ヨ | ラ | リ | ル | レ | ロ | ワ | ウ | ヴ | フ |

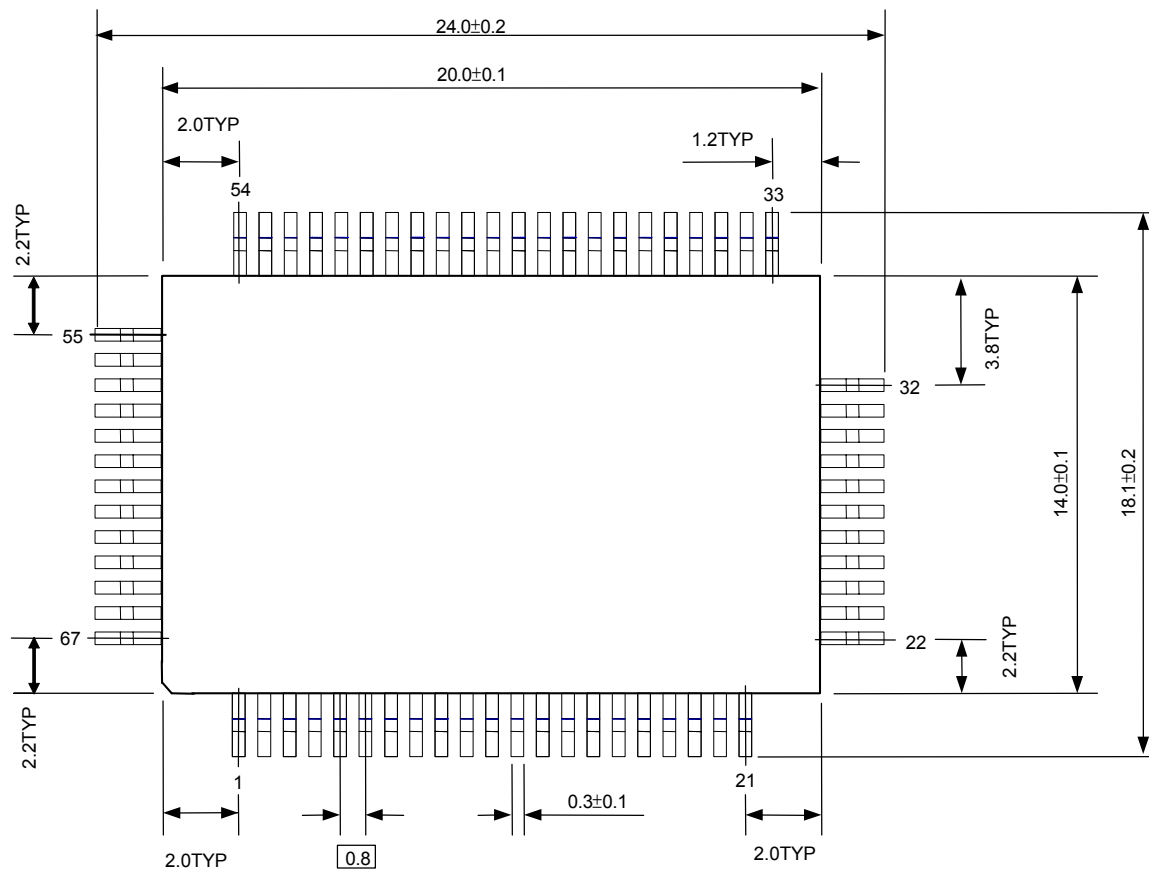
< Figure 6-14 >

The RA6963 has two part number - RA6963L2NA and RA6963L2NB. The RA6963L2NA is compatible to T6963C(code 0101) and the default font is Figure 6-13 as above. The RA6963L2NB is compatible to T6963C(code 0201) and the default font is Figure 6-14 as above.

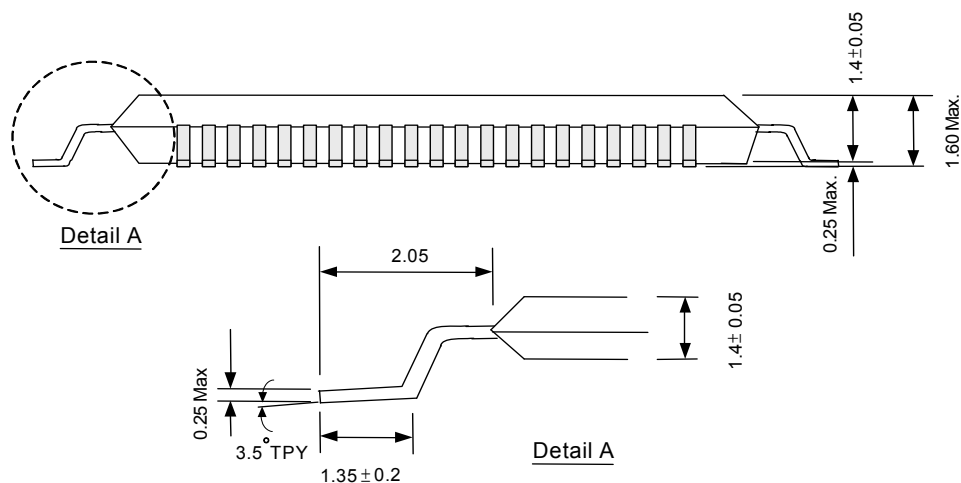
7. Package Dimensions

7-1 Outline Drawing

LQFP-67Pin



< Figure 7-1 >



< Figure 7-2 >

8. Specifications

8-1 Absolute Maximum Ratings

< Table 8-1 >

Ta=25°C

| Parameter | Symbol | Rating | Unit |
|-----------------------------|---------------------------|------------------------------|------|
| Supply Voltage Range | V _{DD} (Note 1) | -0.3 to +7.0 | V |
| Input Voltage Range | V _{in} (Note 1) | -0.3 to V _{DD} +0.3 | V |
| Operating Temperature Range | T _{op} | -30 to +85 | °C |
| Storage Temperature Range | T _{stg} | -55 to +125 | °C |
| Solder Temperature Range | T _{sdt} (Note 2) | 400 | °C |

Note 1 : Gnd = 0V.

Note 2 : Solder Time = 8 Minutes.

< Table 8-2 >

(V_{DD}=+5V / +3.3V±10%, GND=0V, Ta= -20 to +70°C)

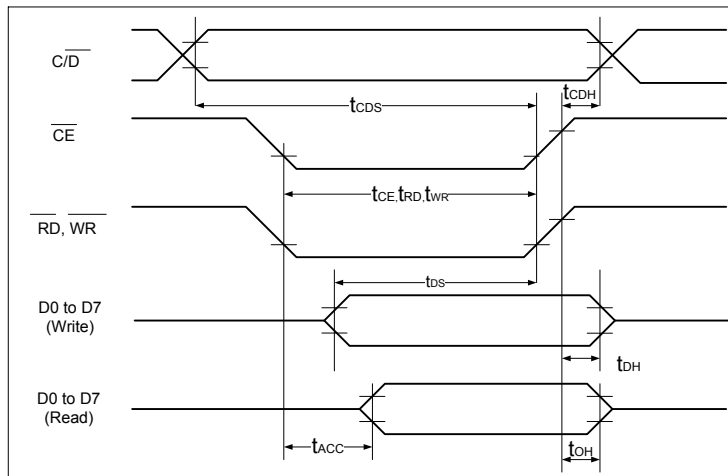
| Item | Symbol | Test Conditions | Min. | Typ. | Max. | Unit | Pin Name |
|--------------------------|------------------|---------------------|--|----------------------|--------------------|------|----------|
| Operating Voltage | V _{DD} | V _{DD} | -- | 3.0 | 5.5 | V | VDD |
| Input | "H" | V _{IH} | -- | 0.8V _{DD} | V _{DD} | V | I/P |
| | "L" | V _{IL} | -- | 0 | 0.2V _{DD} | V | I/P |
| Output | "H" | V _{OH} | -- | V _{DD} -0.3 | V _{DD} | V | O/P |
| | "L" | V _{OL} | -- | 0 | 0.3 | V | O/P |
| Output Resistance | "H" | R _{OH} | V _{OUT} =V _{DD} -0.5 | -- | 400 | Ω | O/P |
| | "L" | R _{OL} | V _{OUT} =0.5 | -- | 400 | Ω | O/P |
| Current Consumption | Operating | I _{DD} (1) | V _{DD} =5.0V (Note 2) f _{OSC} =4.0MHz | -- | 3.0 | 5 | mA |
| | Halt | I _{DD} (2) | V _{DD} =5.0V | -- | 1 | 2 | μA |
| Input Pull Up Resistance | RPU | -- | 50 | 100 | 300 | KΩ | (Note 1) |
| Operating Frequency | f _{OSC} | -- | 0.4 | 6 / 8 | -- | MHz | |
| Solder Temperature | T _{SDT} | (Note 3) | -- | 260 | -- | °C | |

Note 1: Applied TEST[2:1], RST.

Note 2: MDS=L, MD[1:0]=LL, MD[3:2]=HH, FS[1:0]=LL, SDSEL=L, DUAL=H, D[7:0]=LHLHLHLH.

Note 3: Solder Time = 20~40 Seconds.

8-2 MPU Interface Timing



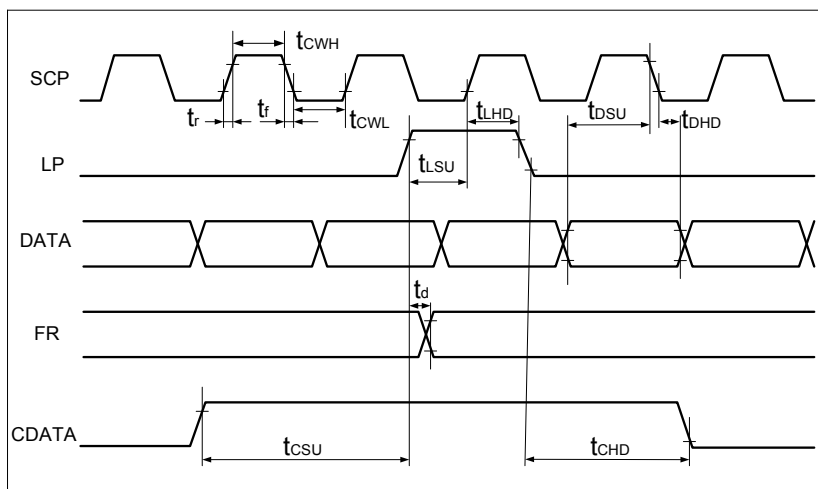
< Figure 8-1 >

< Table 8-3 >

($V_{DD}=+5V\pm5\%$, $GND=0V$, $T_a = -20$ to $+70^{\circ}C$)

| Item | Symbol | Test Conditions | Min. | Max. | Unit |
|---|--------------------------------|-----------------|------|------|------|
| C/ \overline{D} Set Up Time | t_{CDS} | -- | 100 | -- | ns |
| C/ \overline{D} Hold Time | t_{CDH} | -- | 10 | -- | ns |
| CE, \overline{RD} , \overline{WR} Pulse Width | t_{CE} , t_{RD} , t_{WR} | -- | 80 | -- | ns |
| Data Set Up Time | t_{DS} | -- | 80 | -- | ns |
| Data Hold Time | t_{DH} | -- | 40 | -- | ns |
| Access Time | t_{ACC} | -- | -- | 150 | ns |
| Output Hold Time | t_{OH} | -- | 10 | 50 | ns |

8-3 Driver Interface Timing



< Figure 8-2 >

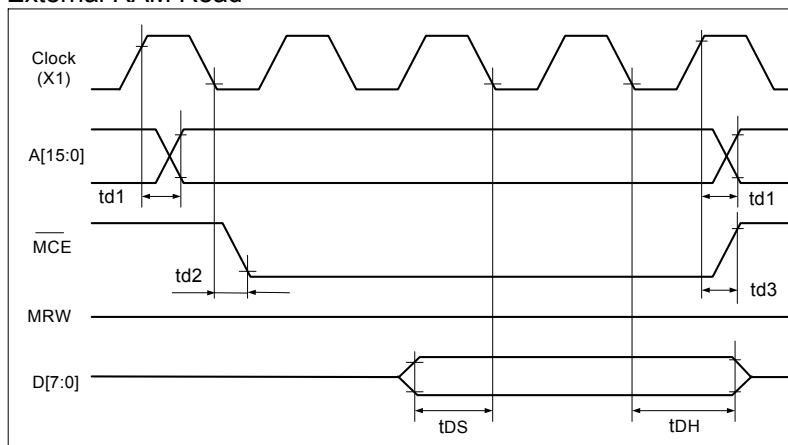
< Table 8-4 >

($V_{DD}=+5V\pm5\%$, GND=0V, $T_a = -20$ to $+70^{\circ}C$)

| Item | Symbol | Test Conditions | Min. | Max. | Unit |
|---------------------|--------------------|----------------------------|------|------|------|
| Operating Frequency | f_{SCP} | $T_a = -20\sim70^{\circ}C$ | -- | 9 | MHz |
| SCP Pulse Width | t_{CWH}, t_{CWL} | -- | 150 | -- | ns |
| SCP Rise/Fall Time | t_r, t_f | -- | -- | 30 | ns |
| LP Setup Time | t_{LSU} | -- | 150 | 290 | ns |
| LP Hold Time | t_{LHD} | -- | 5 | 40 | ns |
| Data Setup Time | t_{DSU} | -- | 170 | -- | ns |
| Data Hold Time | t_{DHD} | -- | 80 | -- | ns |
| FR Delay Time | t_d | -- | 0 | 90 | ns |
| CDATA Setup Time | t_{CSU} | -- | 450 | 850 | ns |
| CDATA Hold Time | t_{CHD} | -- | 450 | 950 | ns |

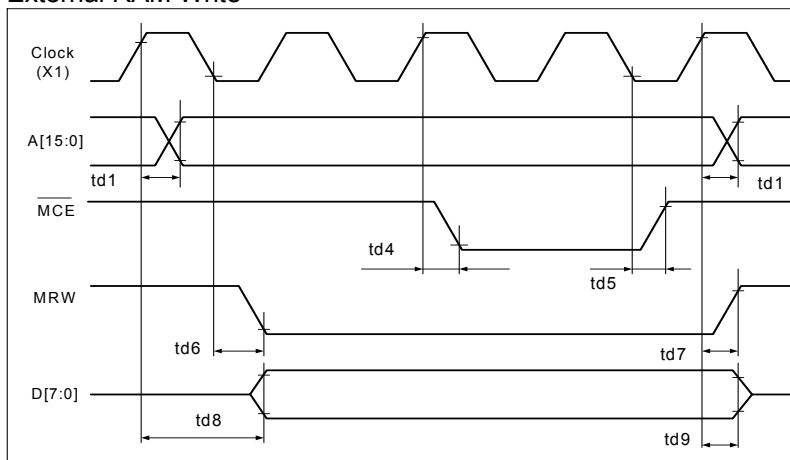
8-4 External Memory Interface

External RAM Read



< Figure 8-3 >

External RAM Write



< Figure 8-4 >

< Table 8-5 >

($V_{DD}=+5V\pm5\%$, $GND=0V$, $T_a = -20$ to $+70^{\circ}C$)

| Item | Symbol | Test Conditions | Min. | Max. | Unit |
|---|----------|-----------------|------|------|------|
| Address Delay Time | t_{d1} | -- | -- | 250 | ns |
| \overline{MCE} Fall Delay Time(Read) | t_{d2} | -- | -- | 180 | ns |
| \overline{MCE} Rise Delay Time(Read) | t_{d3} | -- | -- | 180 | ns |
| Data Setup Time | t_{DS} | -- | 0 | -- | ns |
| Data Hold Time | t_{DH} | -- | 30 | -- | ns |
| \overline{MCE} Fall Delay Time(Write) | t_{d4} | -- | -- | 200 | ns |
| \overline{MCE} Rise Delay Time(Write) | t_{d5} | -- | -- | 200 | ns |
| MRW Fall Delay Time | t_{d6} | -- | -- | 180 | ns |
| MRW Rise Delay Time | t_{d7} | -- | -- | 180 | ns |
| Data Stable Time | t_{d8} | -- | -- | 450 | ns |
| Data Hold Time | t_{d9} | -- | -- | 200 | ns |

9. Application

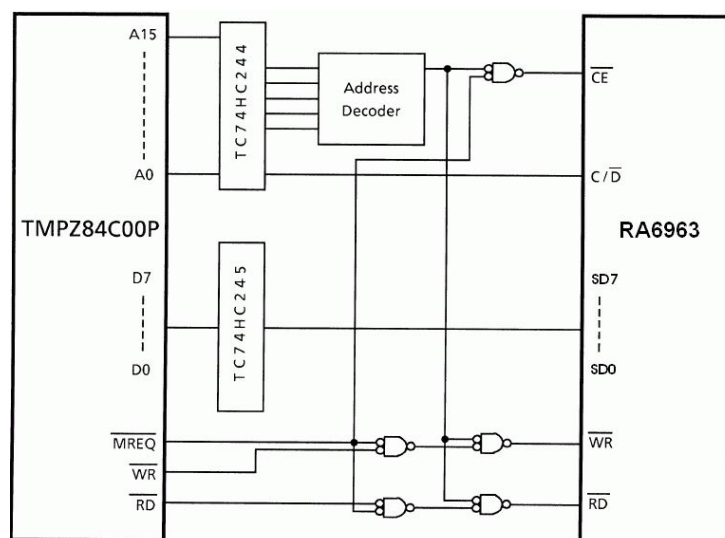
The RA6963 can be directly connected to Z80(Note 1) series MPU. The following applications are use a TMPZ84C00A to connect RA6963.

9-1 MPU Memory Address Mapping

Data is transferred to the RA6963 using a memory request signal.

< Table 9-1 >

| | Address |
|----------------|-----------|
| DATA (I/O) | XXXXh |
| Command/Status | XXXX + 1h |



< Figure 9-1 >

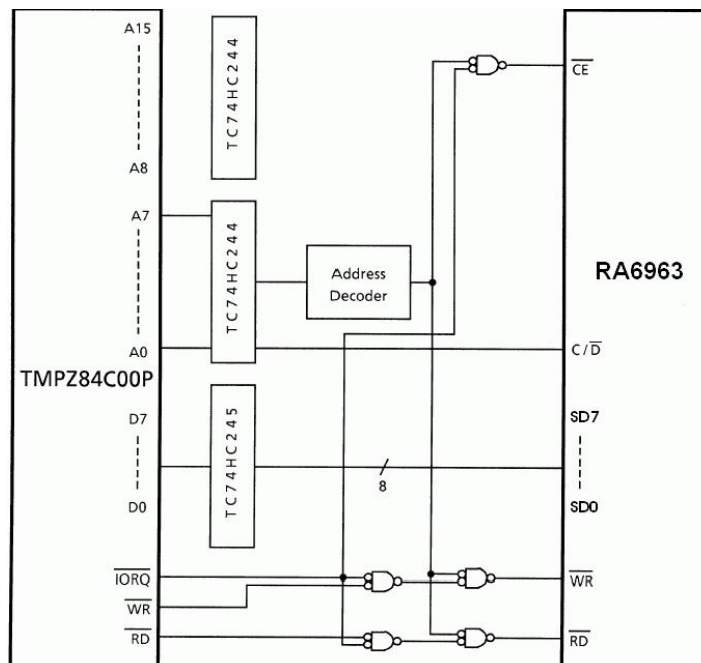
Note 1: Z80 is a trademark of Zilog Inc.

9-2 MPU I/O Addressing

Data is transferred to the RA6963 using an I/O request signal.

< Table 9-2 >

| | I/O Address |
|------------------|-------------|
| DATA | XXh |
| Command / Status | XX + 1h |



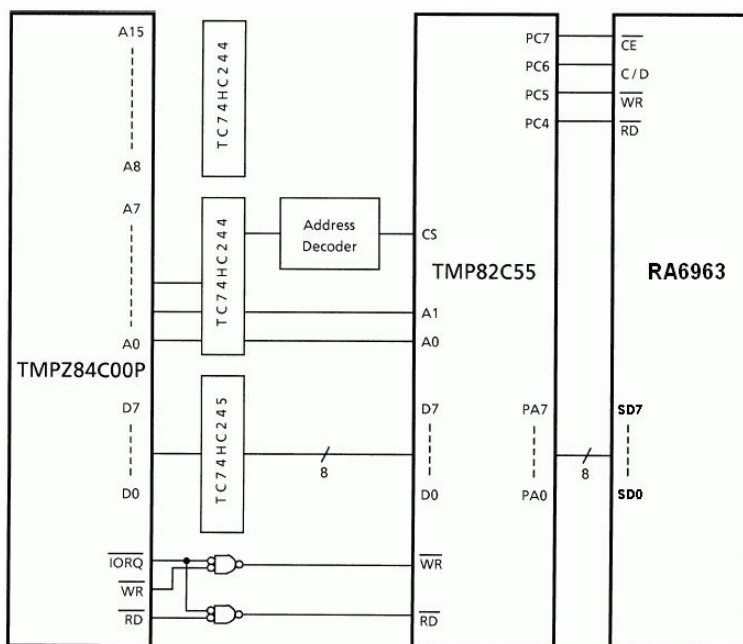
< Figure 9-2 >

9-3 Use PPI LSI

The RA6963 can be connected to a PPI LSI.

The port A connects to the data bus.

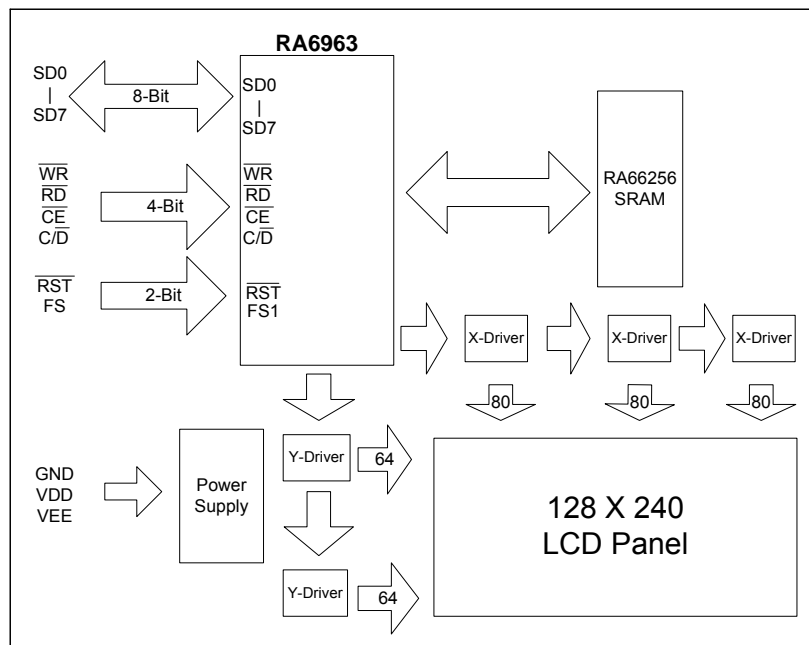
The port C connects to the control bus. ($\overline{C/D}$, \overline{CE} , \overline{WR} , \overline{RD})



< Figure 9-3 >

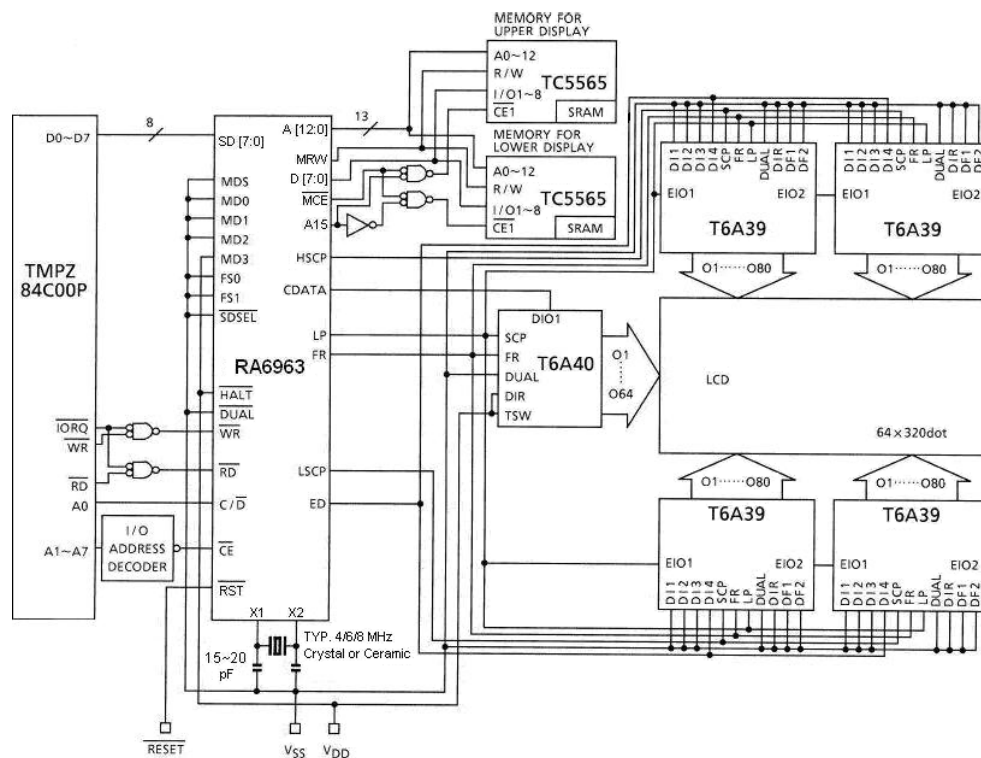
9-4 Application Block Diagram

All LCD require two power sources, VDD for logic circuits and VEE for Liquid Crystal (LC) drive. Some graphics LCD modules will run directly of a single VDD supply by generating the VEE voltage on-board; others will require an external DC-DC converter to generate the negative VEE voltage. Refer to individual specifications for details.



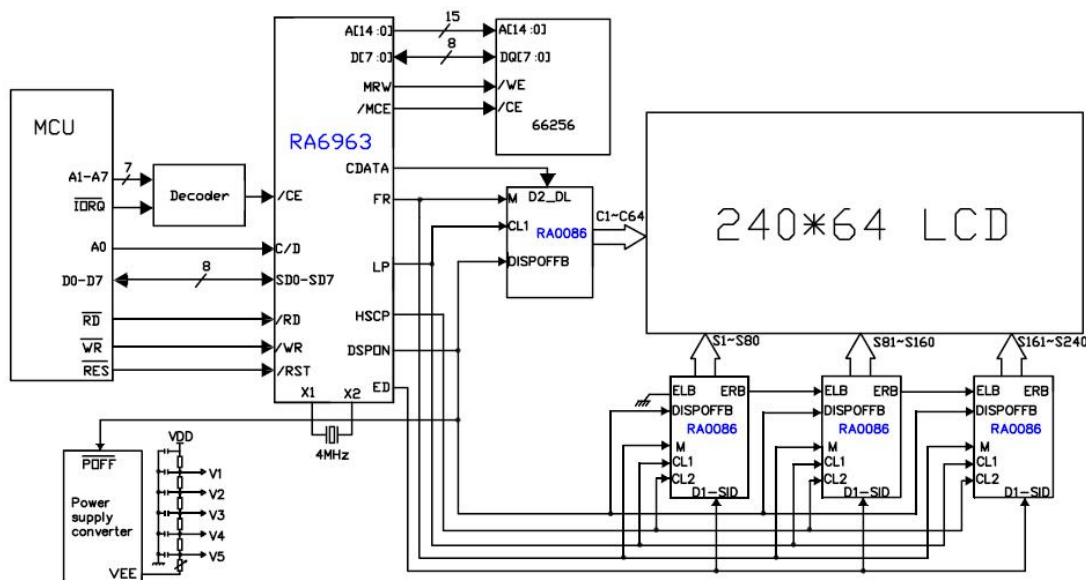
< Figure 9-4 >

9-5 Application Circuit(1)



< Figure 9-5 >

9-6 Application Circuit(2)



< Figure 9-6 >

