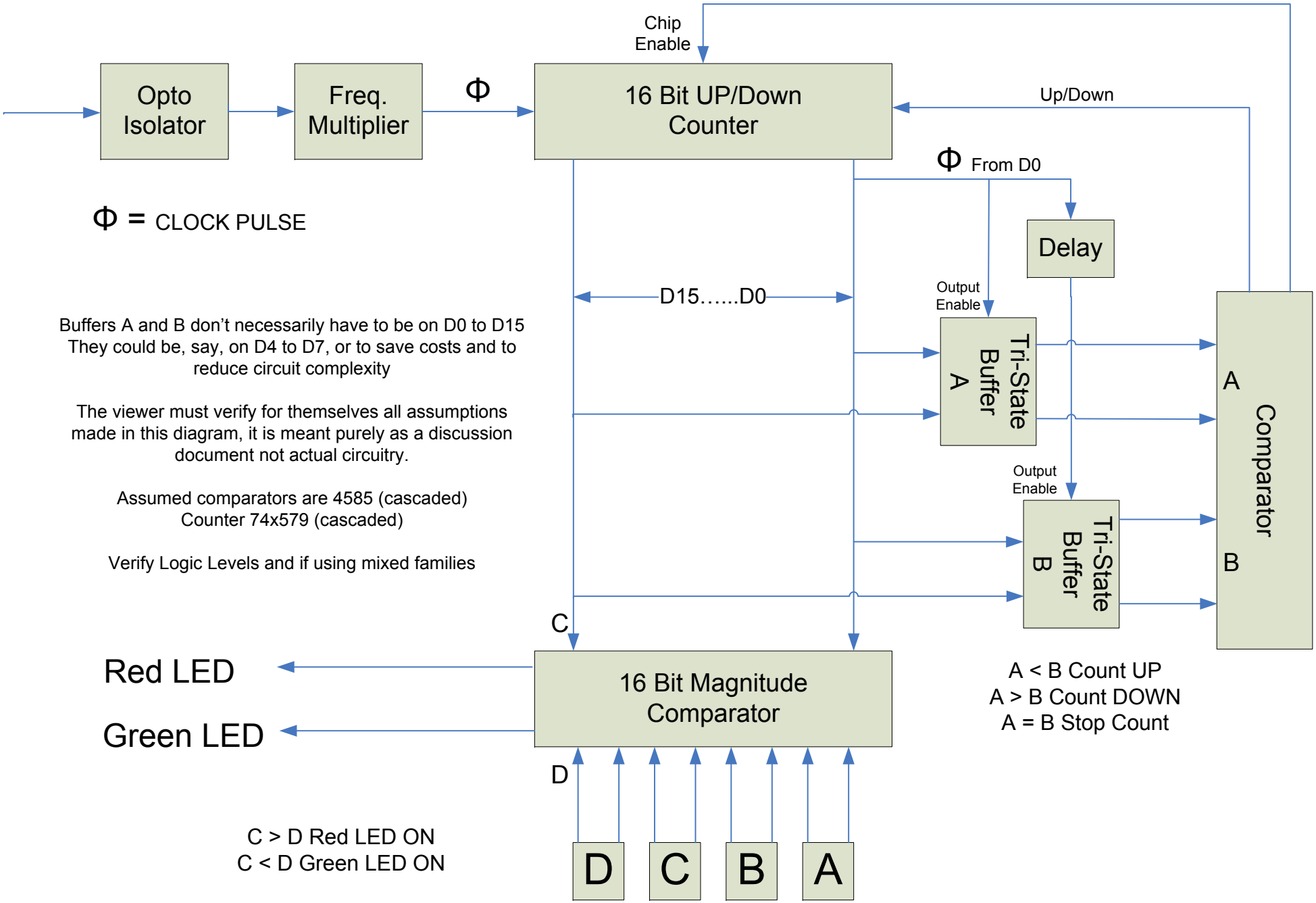
Chip Enable
Opto Isolator
Freq. Multiplier
Φ
16 Bit UP/Down Counter
Up/Down
Φ From D0
Φ = CLOCK PULSE
Delay
D15……D0
Output Enable
Tri-State Buffer A
Output Enable
Tri-State Buffer B
A
Comparator
B
Buffers A and B don't necessarily have to be on D0 to D15
They could be, say, on D4 to D7, or to save costs and to reduce circuit complexity
The viewer must verify for themselves all assumptions made in this diagram, it is meant purely as a discussion document not actual circuitry.
Assumed comparators are 4585 (cascaded)
Counter 74x579 (cascaded)
Verify Logic Levels and if using mixed families
C
Red LED
Green LED
16 Bit Magnitude Comparator
A < B Count UP
A > B Count DOWN
A = B Stop Count
D
C > D Red LED ON
C < D Green LED ON
D
C
B
A