Get precise voltage division without precision parts

Pulse-width modulation can be advantageously applied to building a voltage divider that is accurate enough to serve as a calibration standard even with parts that only have a 10% tolerance (Fig. 1).

To produce precision voltage division, the circuit uses a pulse signal that has its duty cycle proportional to the desired voltage. The signal's amplitude is stabilized, and integration of the resulting waveform provides the desired output.

An SN74L73 operates as a two-stage ripple counter driven by a clock signal generated by part of an SN74L00 gate package. Two of the 74L00 gates decode the counter output to produce waveforms of 0%, 25%, 50%, 75% and 100% duty cyce. Two FETs operated as switches driven by these controlled waveforms fix the amplitude at a reference voltage, V_R, which in this case is equal to 4.0000 V. The resulting signal output from the FET circuit is averaged by an RC low-pass filter and then buffered with an LM 208.

The 1-V output steps are accurate to well within 1-mV; output noise level is under 0.3-mV peak to peak; and stabilization time is about 10 s. For equivalent results with a conventional divider network, expensive resistors with better than ±0.05% accuracy and long-term stability would be needed. Such resistors alone cost more than this entire circuit.

Logic to provide any number of output steps can be added easily. Stabilization time can be cut by reducing the averaging filter's time constant, but that would increase output ripple unless a higher clock rate is used requiring higher-speed FETs.

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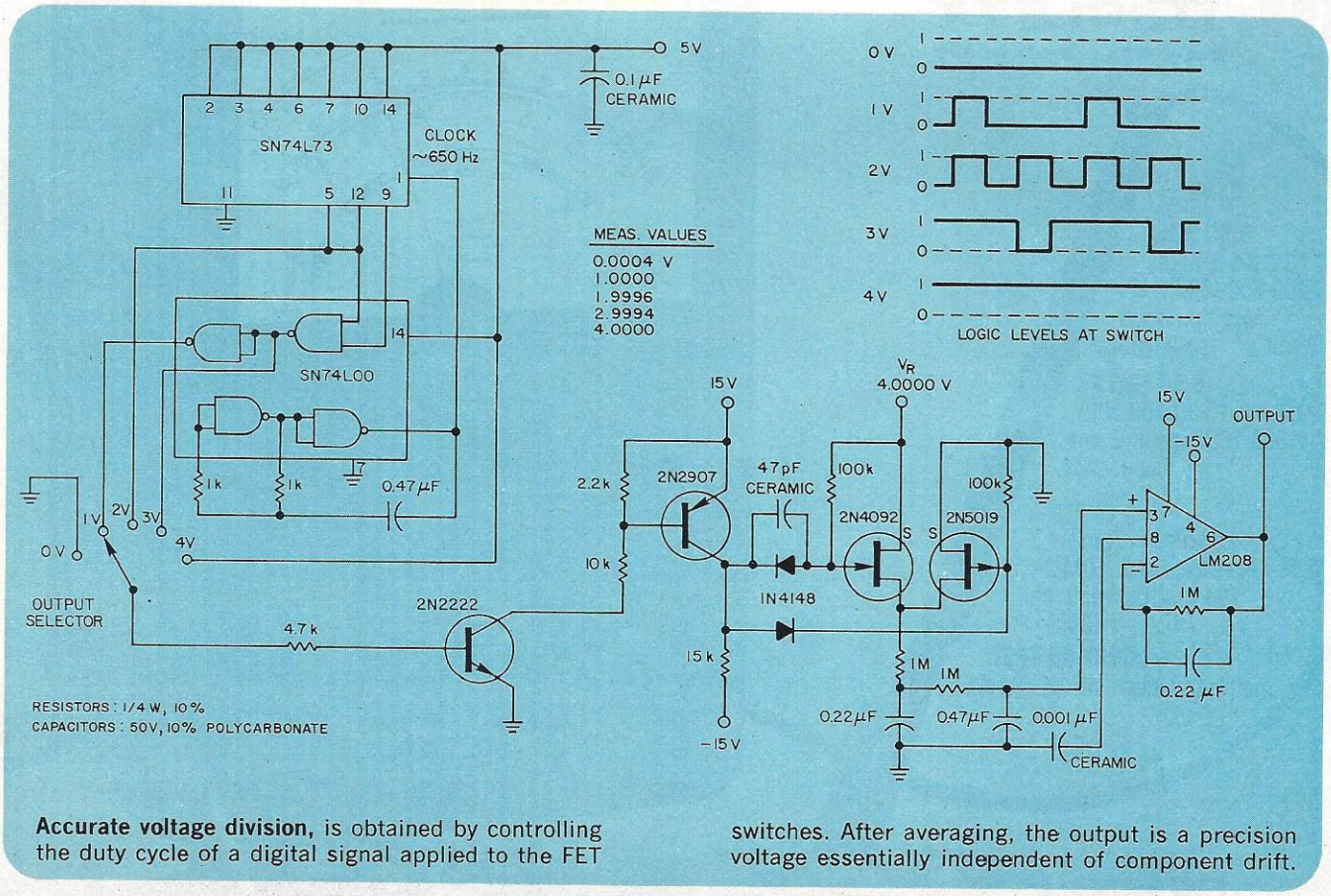

Accurate voltage division, is obtained by controlling the duty cycle of a digital signal applied to the FET switches. After averaging, the output is a precision voltage essentially independent of component drift.