Table 3: ISD1100 and ISD1200 Address Space

Dec.	Binary								ISD1100/1200 (Seconds)
	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0.125
8	0	0	0	0	1	0	0	0	1.0
10	0	0	0	0	1	0	1	0	1.25
13	0	0	0	0	1	1	0	1	1.625
50	0	0	1	1	0	0	0	0	6.25
64	0	1	0	0	0	0	0	0	8.0
79	0	1	0	0	1	1	1	1	9.875
80	0	1	0	1	0	0	0	0	
through	Unused address space. An ISD1100/1200 device addressed in this region will default to an overflow condition.								
191	1	0	1	1	1	1	1	1	
192	1	1	0	0	0	0	0	0	
through	This address space used by the ISD1100/1200 Operational Modes.								
255	1	1	1	1	1	1	1	1	

To playback a message previously recorded at the 10-second boundary, the address pins are again loaded with an address of 100, and with PD LOW and P/$\overline{R}$ HIGH, $\overline{CE}$ is pulsed LOW. The ISD1016A will play back the message, stopping when it finds the set EOM bit. At the same time, the $\overline{EOM}$ pin will pulse LOW to indicate a message end. Whenever a Record operation is in progress and passes through the time of a previously set EOM bit, the bit is cleared. Thus, the EOM is recorded over and "erased."

SIMPLIFIED ADDRESSING SCHEMES

The ISD devices have eight, nine or ten address lines, depending upon which series is considered. For full control of the addressing this means that an 8- or 10-bit latch or microcontroller port must be used to completely address the ISD analog storage chip.