

# Optimum Design of Snubber Capacitors in 9kW Three-phase Inverter for Doubly Salient Permanent Magnet Motor

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**Abstract**—Single-chop upper switch hysteretic-current control strategy is used in three-phase full-bridge MOSFET inverter for a 9kW 12/8-pole doubly salient permanent magnet (DSPM) motor. Due to high chopping frequency, mosfet's parasitics, the existence of parasitic inductance, and also instantaneous variation of winding back EMF and winding inductance, the working of the inverter is quite complicated, and significant voltage spike and current spike will appear each time when chopped upper mosfet's turn off, which induces severe voltage and current stress on MOSFETs and reduces system reliability. Thus, effective and easy-to-implement snubbers are needed to release or resolve the above mentioned problem. The paper details the working of three phase snubbers, and gives design guidelines, heat dissipation analysis and cooling ways for snubber capacitors.

## I. INTRODUCTION

Single-chop upper switch hysteretic-current control strategy is used in three-phase full-bridge MOSFET inverter for a 9kW 12/8-pole doubly salient permanent magnet (DSPM) motor. Due to high chopping frequency, mosfet's parasitics, the existence of parasitic inductance, and also instantaneous variation of winding back EMF and winding inductance, the working of the inverter is quite complicated, and significant voltage spike and current spike will appear every time when chopped upper mosfets turn off, which induces severe voltage and current stress on mosfets and reduces system reliability.

In the paper, the working principle of three-phase inverter with single-chop upper switch hysteretic-current control strategy is first presented, with the analysis focus on the operation of switching intervals for mosfets and the working of three phase snubbers, which show that due to physical position differences for three phase snubbers, the active energy they need to deal with during switching intervals for mosfets is quite different and so are their design requirements. Then formulas for capacitance choice of three-phase snubber capacitors are deduced. Detailed heat dissipation analysis is given, considering extreme working conditions, and then design guidelines for snubber capacitors of three-phase are generalized, with the aim of making heat dissipation evenly distributed in the inverter. Finally, the optimum three-phase snubbers design is given, which is a trade-off among capacitance, temperature rise, size and cost. Main experimental waveforms, overall efficiency test results, and temperature rise test results of snubber capacitors are given under different sets of snubber parameters, whose comparison testify the analysis is correct and the design of snubbers is feasible and reliable, thus ensuring reliability of the whole motor drive.

## II. BASIC PRINCIPLES OF SINGLE-CHOP OPERATION

### A. Control Strategy of Three-Phase Inverter

Fig.1 shows a preferred three-phase full-bridge inverter for the 12/8-pole flume-rotor DSPM motor, and in order to obtain maximum torque output, three-phase six-state conduction modes are adopted. At any time, compare back EMFs of three windings, and for the maximum positive voltage among three back EMFs, the high switch of corresponding phase conducts, and for the maximum negative voltage among three back EMFs, the low switch of corresponding phase conducts. In each period, the conducting region for every switch is 120 electrical angle, and switches commute every 60 electrical angle. There are totally six working regions in each period, neglecting commutation process. And during every working region two windings are conducting.

For the effective control of motor speed, single-chop control strategy is commonly adopted to adjust the equivalent voltage on the winding. Thus under single-chop high switch control strategy, the operation of the inverter is as follows. During every working region in one period, phase p1 and phase p2 are conducting, here p1 and p2 refer to any two of three phases. The high mosfet of phase p1 is working in PWM state and the low mosfet of phase p2 keeps conducting. Fig.2 gives driving signals of mosfets in three phase inverter. Tab.I shows the relationship among winding back EMFs, winding currents and switches of conducting phases.

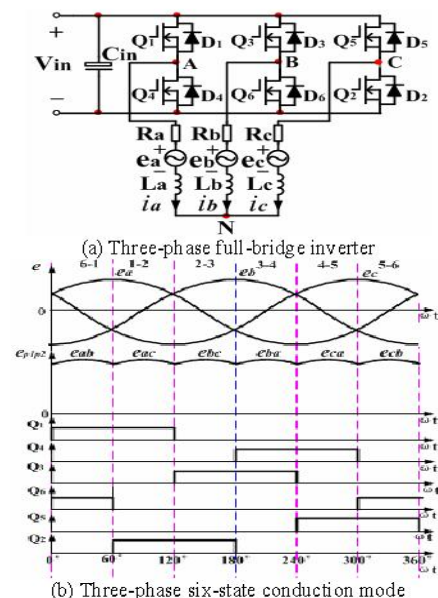


Fig.1 Three-phase full-bridge inverter and conduction mode

TABLE I. Relationship between winding back EMFs, switches and winding currents in one period

Conduction Modes	1	2	3	4	5	6
Working Regions	$[0, 60^\circ]$	$[60^\circ, 120^\circ]$	$[120^\circ, 180^\circ]$	$[180^\circ, 240^\circ]$	$[240^\circ, 300^\circ]$	$[300^\circ, 360^\circ]$
Line Back Expressions	$e_{ab}$ $\sqrt{3}E \sin(\alpha t + \pi/3)$	$e_{ac}$ $\sqrt{3}E \sin(\alpha t)$	$e_{bc}$ $\sqrt{3}E \sin(\alpha t - \pi/3)$	$e_{ba}$ $\sqrt{3}E \sin(\alpha t - 2\pi/3)$	$e_{ca}$ $\sqrt{3}E \sin(\alpha t - \pi)$	$e_{cb}$ $\sqrt{3}E \sin(\alpha t + 2\pi/3)$
EMF Variation	$3E/2 \sim \sqrt{3}E \sim 3E/2$					
Current Rising Stage	$Q_1 Q_6$	$Q_1 Q_2$	$Q_3 Q_2$	$Q_3 Q_4$	$Q_5 Q_4$	$Q_5 Q_6$
Current Falling Stage	$D_4 Q_6$	$D_4 Q_2$	$D_6 Q_2$	$D_6 Q_4$	$D_2 Q_4$	$D_2 Q_6$
$i_a$	+	+		-	-	
$i_b$			+	+		-
$i_c$		-	-		+	+

### B. Mechanism for Upper Mosfet Turn-off Voltage Spike

The equivalent circuit for three-phase full-bridge inverter and motor winding is illustrated in Fig.3, with the focus on the relative positions of snubber capacitors.  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  are snubber capacitors, which can be expressed as the series of capacitance and its ESR. There exists parasitic inductors in the power bus, and their inductance value varies with the distance between the input spot to the calculated point. Corresponding capacitors  $C_1$ ,  $C_2$  and  $C_3$ , equivalent inductors are labeled as  $L_a$ ,  $L_b$  and  $L_c$  respectively, and their inductance values test results are shown in Tab.II. Because  $C_3$  is far from the input spot, and the area for circuit loop is largest, so that the equivalent parasitic inductor for the position of  $C_3$  has the largest inductance.

Due to the existence of these parasitic inductors, the upper mosfet will appear turn-off voltage spike. For convenience, here we take phase a as example and give the analysis. At the time interval that power mosfet A+ turns off, winding current is freewheeling through the body diode of A-. At the same time, due to the existence of parasitic inductance, corresponding bus current can't disappear instantly, and oscillation between parasitic inductors and capacitors will happen, resulting in much

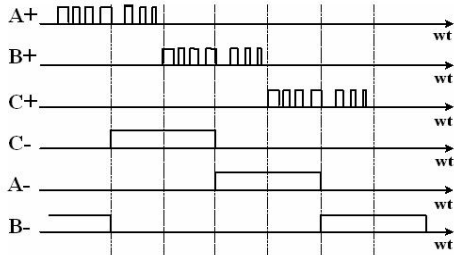


Fig.2 Driving signals of mosfets in three phase inverter

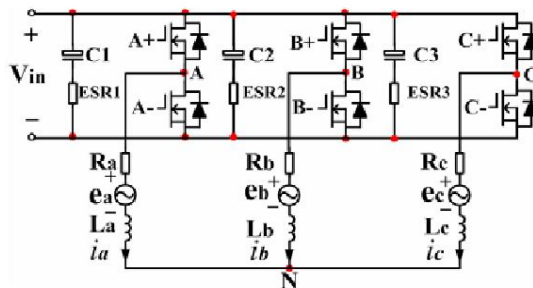


Fig.3 Equivalent circuit of three phase inverter and winding

Tab.II. Inductance value test results of three-phase power inverter

Frequency (Hz)	Inductance Value (uH)		
	$L_a$	$L_b$	$L_c$
1K	0.142	0.306	0.400
20K	0.126	0.258	0.352
50K	0.123	0.240	0.346

voltage spike between the drain and source gates in upper mosfet. The induced voltage spike will reduce the reliability of system and it's expected to find solution to reduce or eliminate the voltage spike.

### III. CHOICE OF SNUBBER CAPACITORS

#### A. Choice of capacitance value

According above analysis, it's apparent that at the time interval that upper mosfet turns off, oscillation between parasitic inductor and capacitor will happen, and its resonant circuit is illustrated in Fig.4.

Neglecting the power loss, and starting from the time interval that upper mosfet turns off, parasitic inductor and capacitor are working in resonant state, and circuit meets

$$L \frac{di_L}{dt} + V_c = V_{in} \quad (1)$$

$$C \frac{dV_c}{dt} = i_L \quad (2)$$

It can be derived from (1) and (2) that,

$$v_c(t) = V_{in} - V_{in} \cos \omega_r(t - t_0) + Z_r I_{L0} \sin \omega_r(t - t_0) \quad (3)$$

here,  $\omega_r = 1/\sqrt{LC}$ ,  $Z_r = \sqrt{L/C}$

From (3), it can be seen that voltage spike is affected by the following parameters: (1) The more the parasitic inductance, the lower the resonant frequency, and the corresponding voltage spike will be higher. (2) The more the parasitic capacitance, the lower the resonant frequency, and the corresponding voltage spike will be lower. (3) The higher initial current value, the larger the voltage spike. Thus, for different bus inductors as shown in Tab.II., the needed snubber capacitors ( $C_1$ ,  $C_2$  and  $C_3$ ) are different.

#### B. Loss Calculation

The power loss of snubber capacitor comes from the current flowing through it and capacitor's equivalent series resistor. When the same snubber capacitors are adopted in the inverter, the power losses for them approach the same. Also due to large winding current in power inverter, the commonly used high frequency capacitors can be not used any more because their low capacitance to voltage ratio and also the power dealing ability. Here, the electrolyte capacitors with low ESR and good temperature characteristic are used.

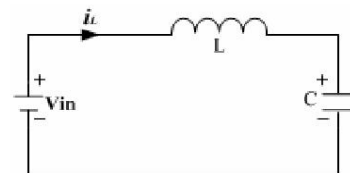


Fig.4 LC series-resonant network



### C. Consideration from The Passage of Forced-Air

Fig.5 gives the illustration of passage of forced-air in three-phase full-bridge. The direction of the air is from phase a to phase b, phase c and then enter into the environment. That means the heat produced at the position of phase a and phase b will be partially transferred to phase c, which makes the ambient temperature of mosfets and snubber capacitors at the position of phase c approach the highest. In order to alleviate the heat stress from phase c, the following choices can be considered: (1) Change the numbers of paralleled mosfets. If the increase of the numbers for paralleled mosfets corresponds to the reduction of power loss for mosfet at phase c, we can add the numbers for paralleled mosfets. (2) Choose the capacitor with larger capacitance, lower ESR, and also better temperature characteristics.

### IV. DESIGN GUIDELINES FOR SNUBBER CAPACITORS

The choice of snubber capacitors are related with many factors, including parasitic inductor, power mosfet, the passage of forced-air, cooling methods and cost. The design guidelines for three-phase full-bridge inverter in the paper can be outlined as follows. Step-1: Establish the control strategy of the inverter, and give the detailed analysis on the possible voltage spike, considering the devices and parasitic inductance in the actual power inverter. Step-2: Determine the strategy for snubber circuit. In all snubber candidates, try to find an easy-to-implement and also effective one. And calculate the value for components in snubber circuits. Step-3: Calculate power loss. According the chosen component value, calculate or estimate the power loss of mosfets and snubber circuits, and adjust their value to meet the design requirement. Step-4: Check heat design and reliability. Compare actual temperatures of snubbers at different physical positions, and ensure that the final design is optimum.

### IV EXPERIMENTAL RESULTS AND ANALYSIS

Based on the above analysis, a prototype of 9kW 12/8-pole flume-rotor DSPM constant-speed drive is fulfilled. The main specifications for the DSPM drive are listed in TABLE.III.

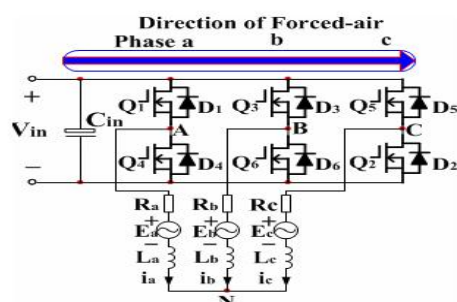


Fig.5 Illustration of direction for forced air in inverter

TABLE.III Specifications for DSPM-BLDCM drive

Input Voltage Span	95VDC-130VDC
Nominal Input Voltage	120VDC
Nominal Output Power	9kW
Nominal Output Speed	7500r/min
Nominal Toque Output	11.46N·m
Efficiency	No less than 75%

### A. Winding Current Waveforms

Fig.6 gives waveforms of phase c at nominal load and nominal speed, with different capacitance value for snubber capacitors which are 680uF and 1200uF respectively. It can be seen from Fig.6 that, the larger the capacitance value, the lower the voltage spike between drain and source gate of mosfet C+. It testifies that larger capacitance is better to restrain the turn-off voltage spike.

### B. Efficiency Test Results

At nominal speed and nominal load conditions, overall efficiency is also tested at two different sets of capacitors, including 680uF and 1200uF. Fig.7 gives overall efficiency curves when input voltage is kept between 90V and 130V. As input voltage increases, overall efficiency decreases. The overall efficiency when snubber capacitor is 1200uF is larger than the one when snubber capacitor is 680 uF, which may be because larger capacitance corresponds to better voltage spike restraining effect, and the switching loss and resonant power are relatively low, thus leading high efficiency.

### C. Temperature Rise Test

A temperature rise test at rated speed under nominal load was also carried out the DSPM drive when snubber capacitors are set to be two different values of 680uF and 1200uF, and are shown in Fig.8(a) and (b) respectively. In Fig.8, C1 to C4 are corresponding to capacitors for different physical positions. From Fig.8, it can be seen that

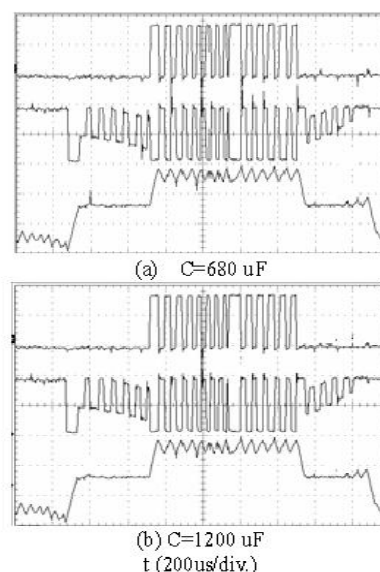


Fig.6 Waveforms of phase c under nominal speed and at nominal load. From the top of trace:1) driving signal for  $Q_5$ (5V/div), 2)voltage between drain and source gate for  $Q_5$ (50V/div), 3)current of winding c(121A/div.)

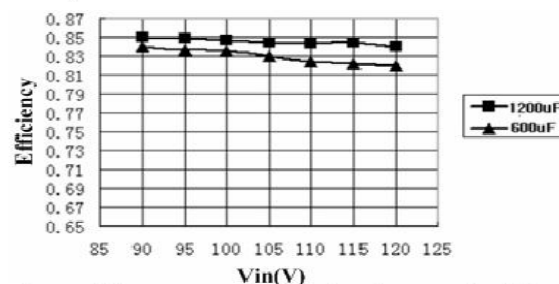


Fig.7 Efficiency curves as input voltage changes under different snubber capacitors

the snubber capacitor at the position that is far away from the input spot is hotter than the one that is near the input spot. Also, capacitor with larger capacitance has better temperature rise characteristics.

Based on the above analysis and experimental results, and consideration from capacitance consistency, circuit connection style, temperature rise, size and cost, the snubber capacitors used in the developed DSPM drive are as follows. Each phase adopts two capacitors and they are in parallel with the power bus, with each capacitor of 1200uF. Through many times of trial experimental tests, their physical positionS are set to be as shown in Fig.9, and the layout in Fig.9 has the best voltage spike restraining effect.

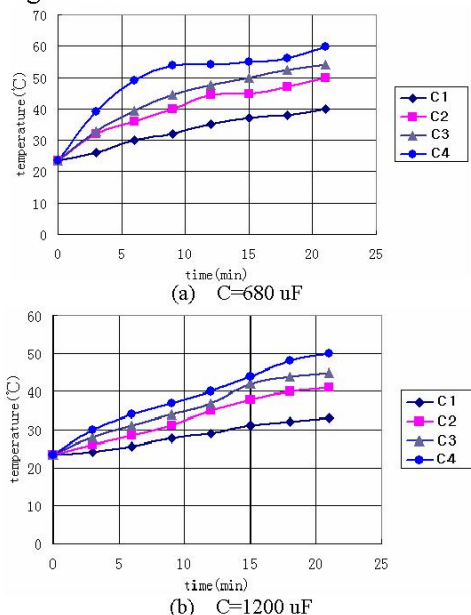
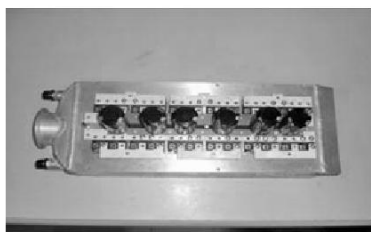


Fig.8 Temperature curves of snubber capacitors



(a) Power mosfet and power bus



(b) Power mosfet, power bus and snubber capacitors

Fig.9 Outline of Power bus and heatsink

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