AN1585
APPLICATION NOTE

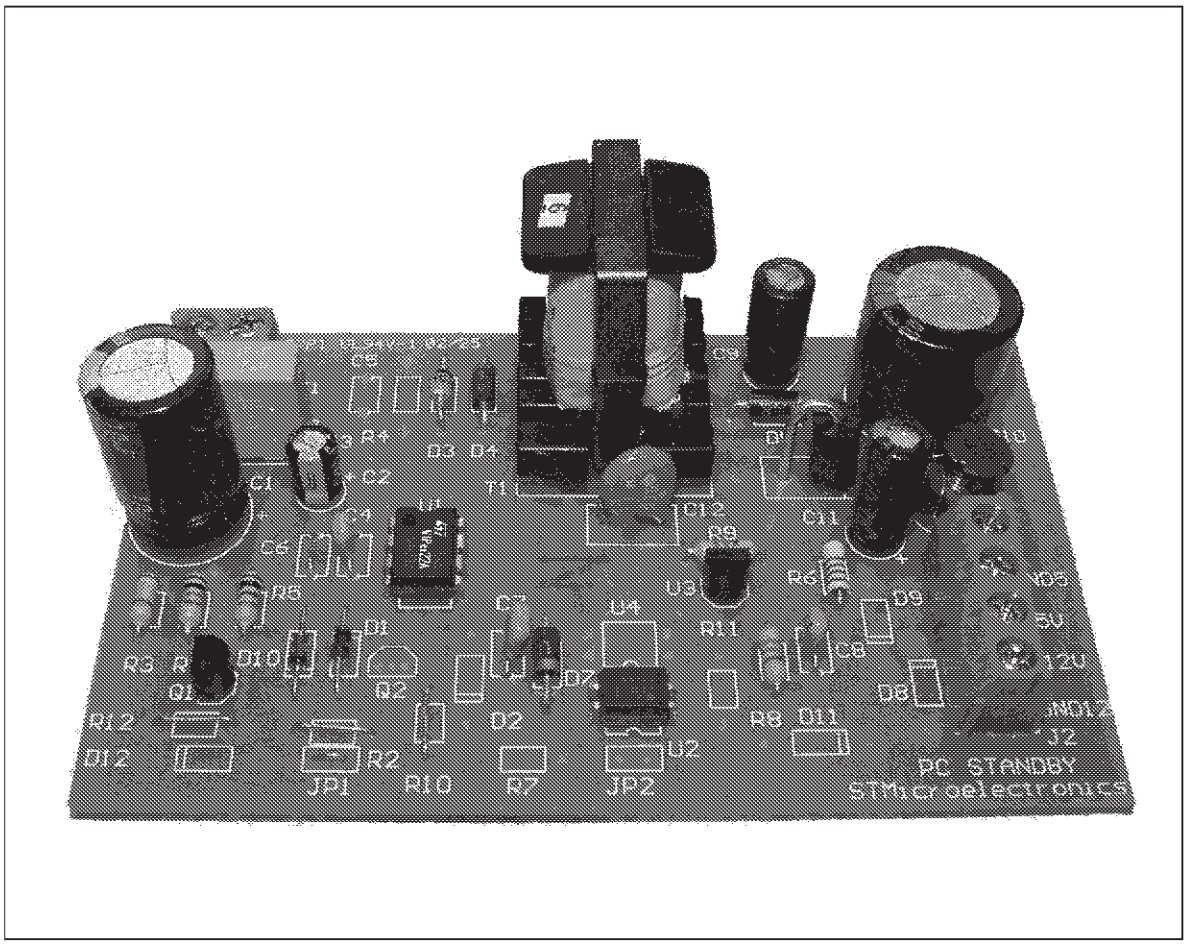
PC Stand-by Power Supply with VIPer22A

A. BAILLY - G. AUGUSTONI

A desktop PC power supply is generally made of two power supplies: the main one built around a forward structure and able to deliver a few hundreds of Watt and switched off in standby mode; the second one with a power capability of up to 15 W always operates to insure the ”instant on” feature or simply the waking up from the off state.

This application note describes the results obtained when designing a VIPer22A in the standby section of such power supplies. A particular concern is the consumption in the idle mode (0.5W of output power), where the input power must not exceed 1W. In addition, a brown-out feature monitors the input voltage in order to switch off the power supply when it is too low.

The figure here below shows the corresponding demoboard. Its description is also included in this document.



1. VIPERX2A DESCRIPTION

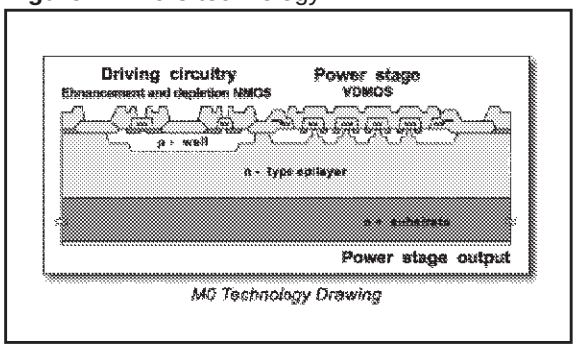
The VIPer12A and VIPer22A devices are high voltage integrated circuits, intended to be used in off line power supply switching taking advantage from minimized part count, reduced size (SO-8 package available) and consumption. They are also able to meet the new Eco Standards with cost effectiveness.

1.1. General features

The VIPerX2A family is a range of PWM controller IC together with a high voltage power MOSFET housed in the DIP-8 and the small SMD SO-8 packages. The features of these devices allow to reduce the overall parts count, leading to compactness and higher reliability which are also reinforced by the automatic thermal shutdown, thanks to the monolithic structure.

This structure uses the proprietary VIPower M0-3 HV Technology which combines a power stage with vertical current flow and a low voltage circuitry in a P-type buried layer, as illustrated by figure 1.

Figure 1: M0-3 technology



The VIPerX2A family devices get a benefit from this technology and from small size packages to address low power applications, as shown on tables 1 and 2. Note that these power capabilities can be achieved with adequate thermal configuration, such as sufficient copper plane area connected to the drain pins on the printed circuit board.

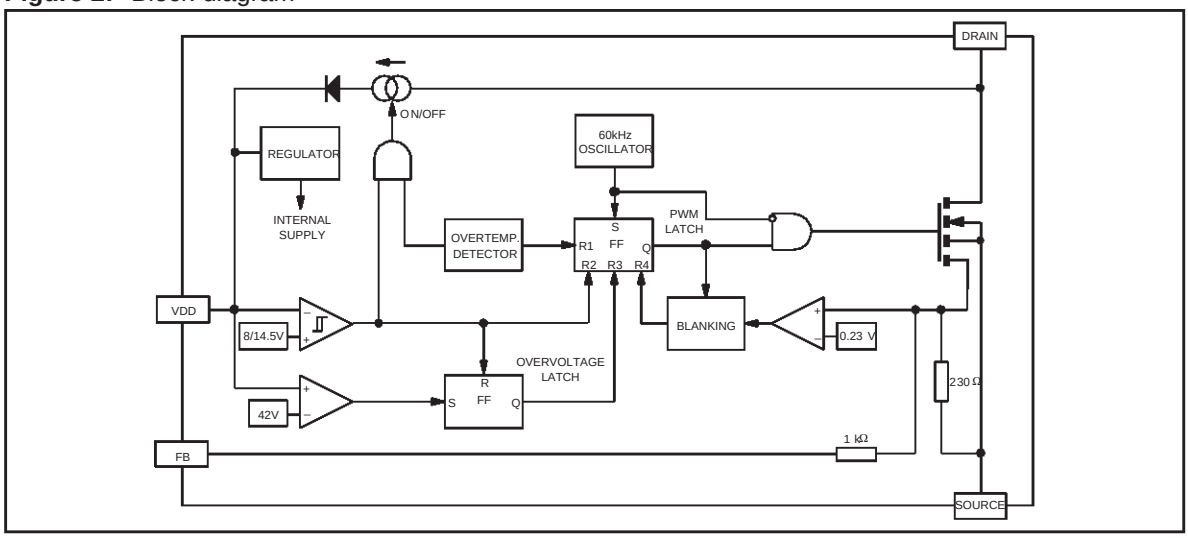
Table 1: Power capability with wide input voltage range (85 - 265 Vac)

DEVICE	PACKAGE	
	SO-8	DIP-8
VIPer12A	5 W	8 W
VIPer22A	7 W	12 W

Table 2: Power capability with European input voltage range (180 - 265 Vac)

DEVICE	PACKAGE	
	SO-8	DIP-8
VIPer12A	8 W	13 W
VIPer22A	12 W	20 W

Figure 2: Block diagram



1.2. Block diagram

Figure 2 presents the internal diagram of the VIPerX2A family.

The power section is a high voltage sense N type mosfet, with a minimum guaranteed breakdown of 730 V. It is driven by a current mode structure with fast comparator using the current delivered by the Nmosfet sense, and blanking time. The switching frequency is internally fixed at 60 kHz.

All the internal signal circuits are supplied with a regulator able to accept a voltage in excess of 45 V. Various protections are implemented, such as the overvoltage on the VDD pin at 42 V, and the thermal shutdown at 170°C typical. As the control structure is a current mode, the drain current is limited cycle by cycle and has a maximum value corresponding to a FB pin held to ground. The feedback loop is implemented by driving this FB pin with an optocoupler connected to a positive voltage.

An hysteresis comparator monitors the VDD voltage to manage the start up current source.It is switched on for charging the VDD capacitor to the start up threshold, and maintained in the off state during the normal switching operation to minimize the input power consumption.

1.3. Current mode structure and burst mode

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input (the inverted input of an operational amplifier), the FB pin is sensitive to current. The figure presents the internal current mode structure.

The Power MOSFET delivers a sense current Is proportional to the main current I_D. R2 receives both this current and the current coming from the FB pin. The voltage across R2 is then compared to a fixed reference voltage of about 0.23V. The MOSFET is switched off when the following equation is reached:

$$R_2 \cdot (I_S + I_{FB}) = 0.23V$$

By extracting Is and introducing the sense mosfet ratio G_{ID}:

$$I_D = G_{ID} \cdot \left(\frac{0.23V}{R_2} - I_{FB} \right)$$

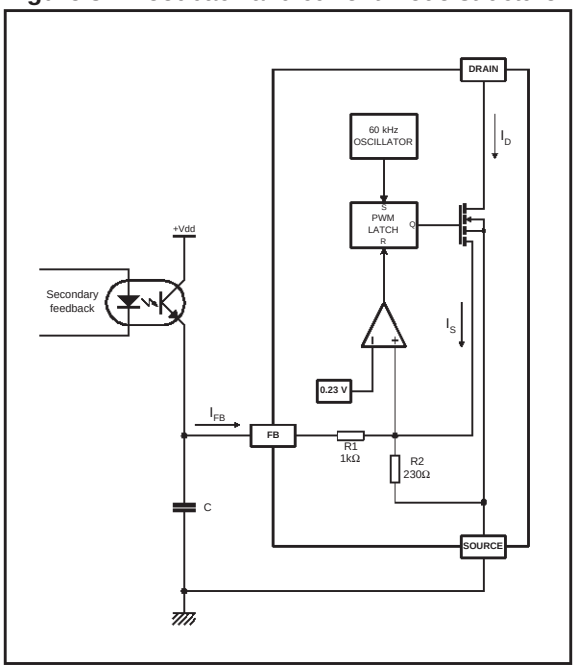
This formula demonstrates that the peak drain current depends linearly on the FB pin current, and that the feedback current must be increased for the drain current to decrease. For very low drain currents, it is effective as long as I_{FB} satisfies:

$$I_{FB} < I_{FBsd}$$

Where I_{FBsd} is an internal threshold of the VIPerX2A. If I_{FB} exceeds this threshold, the device stops switching. This threshold on the FB pin corresponds to about 12% of the current limitation of the device, i.e. about 80 mA for a VIPer22A.

When the output load is decreased and the regulation loop makes the FB pin reach the I_{FBsd} threshold, the device enters a burst mode operation by skipping switching cycles. This is especially important when the converter is lightly loaded, in order to achieve very low input power consumption. Values in the range of 100mW of input power can be reached with no load on the output.

Figure 3: Feedback and current mode structure



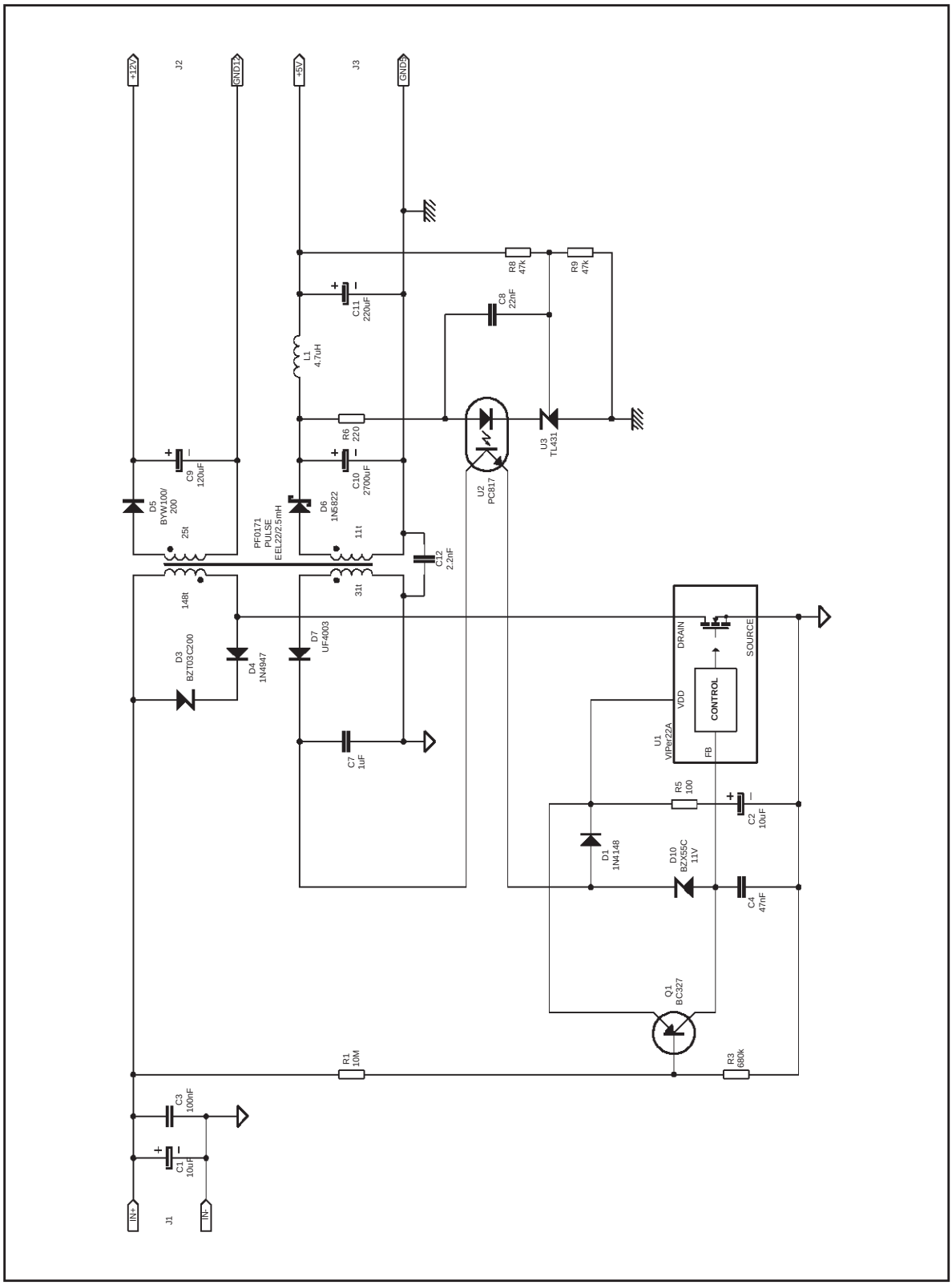
2. PC STANDBY APPLICATION

2.1. Schematics

Figure 4 gives the schematic used to deliver two supply voltages, the +5V and the +12V. Note that most of the power is delivered on the +5V, with a current capability of 2A or 3A, depending on the output diode D6. The board comes with a 1N5822 axial diode able to deliver up to 2A, and the PCB footprint is also compatible with an STPS745 to go up to 3A. All the results given, have been measured in the 3A configuration. The +12V current capability is 100mA.

The +5V output is regulated thanks to U3 and the resistive divider R8 and R9. The regulation information is passed through the optocoupler U2 to the primary side.The feedback is not applied directly to the device FB pin as it is usually done with VIPerX2A, but through D10.

Figure 4: Standard schematic



This configuration offers the following benefits:

1. The device is supplied through the optocoupler, which means that in case of short circuit, it surely goes into hiccup mode as it doesn't receive any more energy from the auxiliary winding. This is a very efficient protection, because the optocoupler is necessarily off in this condition as there is no more voltage on secondary side.
2. The brownout function can be simplified (two transistors are generally needed to insure the same behavior, when the optocoupler is connected on the FB pin), with still a very efficient operation: The consumption on the high voltage rail can be reduced to a minimum thanks to the use of a 10MΩ resistance, and only one transistor is used. The diode D1 can be replaced by a short circuit if D10 is a zener of at least 18V. But of course, the standby consumption will be higher because the device will be supplied with 19V instead of 12V. The auxiliary winding should be modified accordingly.

The brownout feature is built around Q1 and the resistive divider R1 and R3. Q1 behaves like an emitter follower and therefore limits the voltage on its emitter, while sending the corresponding current to the FB pin. When the input voltage rises, the emitter voltage increases accordingly and the VDD voltage is limited to a fraction of the input voltage. This fraction is defined by the ratio of the resistances R1 and R3, and the start up doesn't occur until about 15V is reached on the VDD pin of U1 which corresponds to the start up threshold. With the values indicated on the schematics, this happens for an input voltage of about 245VDC.

When the converter operates normally, and the input voltage decreases, Q1 will force the voltage to decrease because it sends the current drawn from the VDD network to the FB pin. So, the optocoupler sends the feedback current through Q1 instead of D10. The output voltage remains stable, but the VDD pin decreases until it reaches V_{DDoff} where it stops operating. This is occurs for an input voltage of about 130 VDC. The restart current delivered by U1 is drained by Q1 which still limits the VDD voltage to V_{DDoff}, and the V_{DDon} threshold cannot be triggered.

To summarize, the brownout feature designed in this application provides clean turn on and turn off with an hysteresis based on the VDD thresholds of the VIPer22A. As a consequence, the input voltage thresholds are proportional to the V_{DDon} and V_{DDoff}.

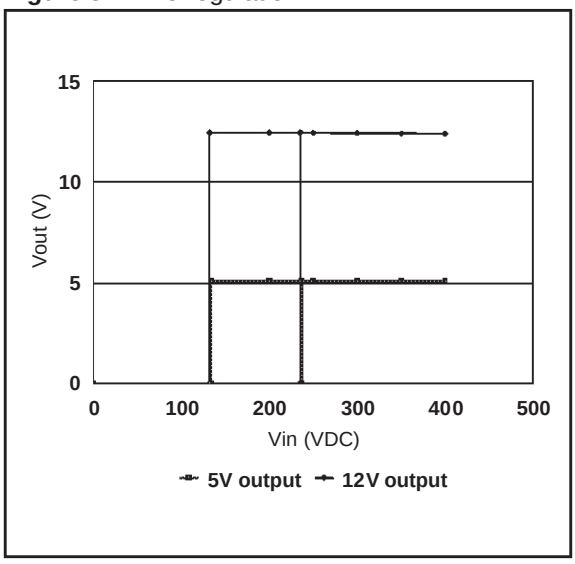
The +12V output is galvanically isolated from any other signal on the board. This allows to connect it on either side of the power supply, for instance on primary side where it can supply the main PWM circuit. In this case, the attention of the reader is drawn on the fact that the general safety requirements are not respected any more, as the transformer is designed to insure a safe isolation between the primary and auxiliary windings on one side, versus the +5V and +12V windings on the other side.

As this converter is intended to be connected after the rectifying of the main power supply, it doesn't have any front diodes bridge, but only capacitive filtering which are mainly here to prevent any interaction with the wires used to experiment the board. In a real application, at least C1 can be omitted, and the input filter is shared with the main power supply.

2.2. Results

The output voltages are measured in the whole input voltage range, i.e. 0VDC to 400VDC. This gives at the same time the line regulation, and the brownout thresholds. This is shown in figure 5, where the +5V output remains constant, and the +12V one decreases by less than 50mV in the whole operating range.

Figure 5: Line regulation



The +12V output voltage is presented in figure 6 for a fixed load of 1A on the +5V output. It has also been measured for fixed loads, and for the whole output current range on the +5V output as shown in figure 7. When lightly loaded, this output should be clamped with a zener to avoid any overvoltage. All measurements have been done for a 300VDC input voltage.

The +5V output doesn't show any significant variation thanks to the direct regulation through U2. So, no measurement is presented for this voltage.

Figure 6: Load regulation

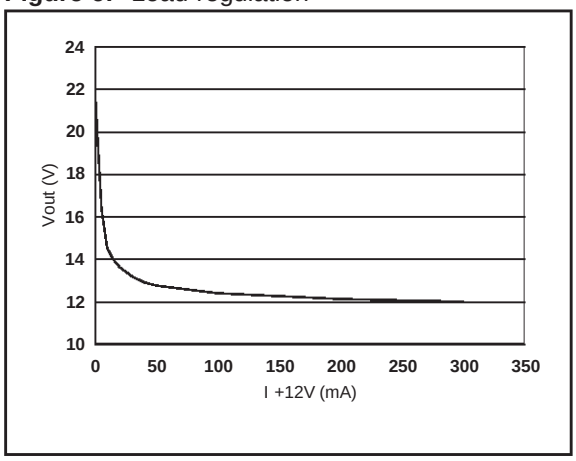
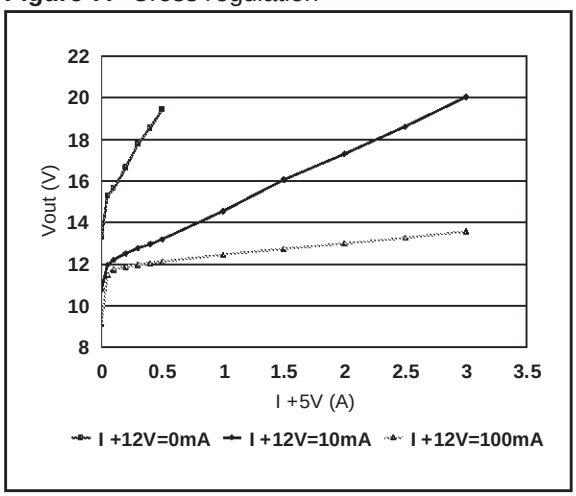


Figure 7: Cross regulation



The efficiency has been measured with the +12V output unloaded, and for an input voltage of 150V and 300V. The results are shown in figure 8. The maximum efficiency is obtained for an output current of about 1A, and the maximum available current is reduced when working with a 150VDC input voltage: 2.5A instead of more than 3A for a 300VDC input.

The input power is also a key issue in this kind of application, where a maximum total value of 1W must be respected when the output load is 0.5W. Therefore, the previous measurement is also presented in figure 9 in terms of input power. 0.82W has been measured for an output of 0.5W, which gives a margin of about 200mW. Note that this margin can be significantly reduced by the main power supply section which has a quiescent consumption in the same range of value. The input power can be decreased further as described in par. 2.3.

Figure 8: Efficiency

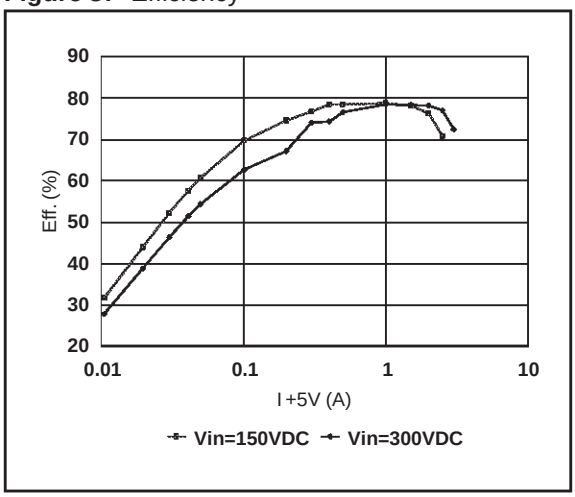
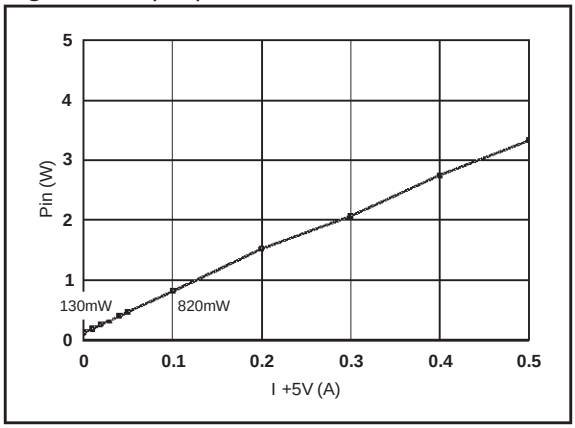


Figure 9: Input power



When operating at low load, the VIPerX2A family of device enters automatically in burst mode, also called pulse skipping mode. This is insured by the threshold I_{FBsd} (about 0.9mA) on the FB pin above which the device stops switching, as explained in par. 1.3. This can be observed in figure 10 shot for an output current of 50mA and an input voltage of 300VDC. The FB voltage oscillates around 1V, which corresponds to the I_{FBsd} threshold multiplied by the input impedance of the FB pin (about 1.2kΩ).

A magnification of one switching cycle is given in figure 11 for an output current of 100mA. The duty cycle remains very low, and as a consequence, the current flowing in the transformer is limited to low values. This avoids mechanical vibration which may cause audible noise, as the switching frequency may reach values well below 16kHz. The advantage of such a low operating frequency is the decrease of the commutation losses and of the input power.

Figure 10: Burst mode operation

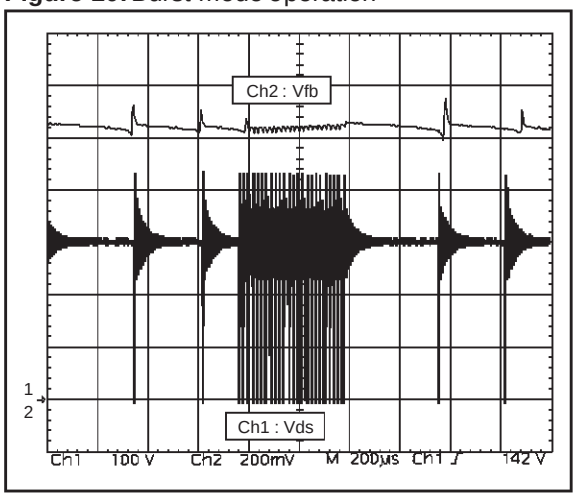


Figure 11: Switching cycle in burst mode

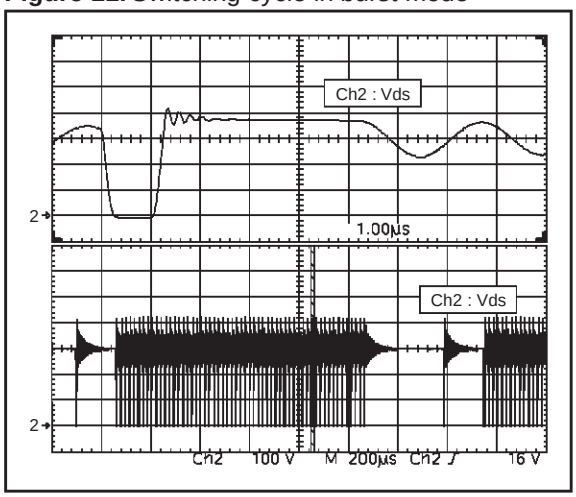
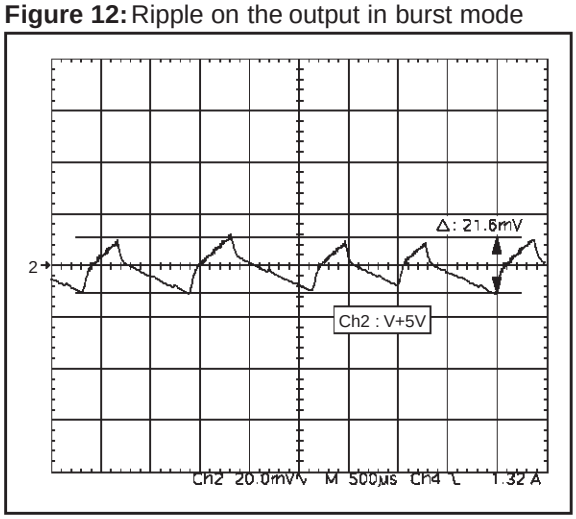


Figure 12: Ripple on the output in burst mode



A low frequency ripple also appears on the output as shown in figure 12, because the converter stops and resumes switching by “packet”, thus generating a triangular waveshape. The amplitude of this ripple remains very limited (less than 22mVpp), and doesn’t depend on the output current value on the whole burst mode operation range.

Figure 13 presents the switching ripple on the output at 3A. Its amplitude (34mVpp) is even higher than the ripple due to burst mode at light load.

Figure 13: Switching ripple on the output

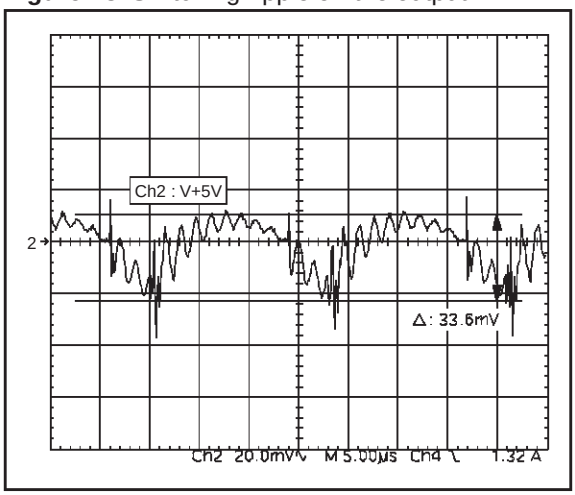
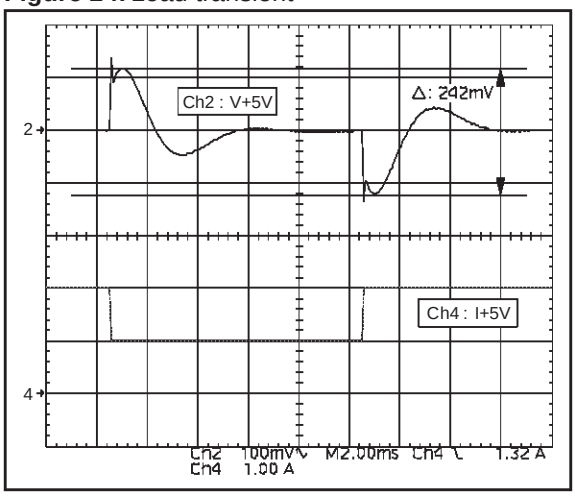


Figure 14: Load transient



A dynamic test has been done on the +5V output with an output current changing from 1A to 2A in a few µs. Figure 14 presents the results, with a variation of the output voltage of about 240mVpp. An initial spike is present at the beginning of each

transient, due to the output filtering network L1-C11. The value of these components can be eventually adjusted (decreasing of L1 and/or increasing of C11) in order to decrease the amplitude of these spikes.

The start up and shutdown of the power supply has been checked on the +5V output. Respective waveforms are shown in figures 15 and 16. The rising time is monotonic with no overshoot, and no glitch can be observed at shut down.

Figure 15: Rising waveforms at start up for 100mA, 1A and 2.5A

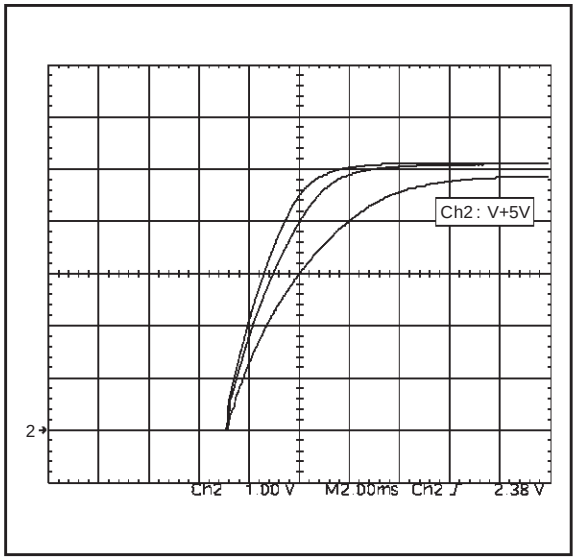
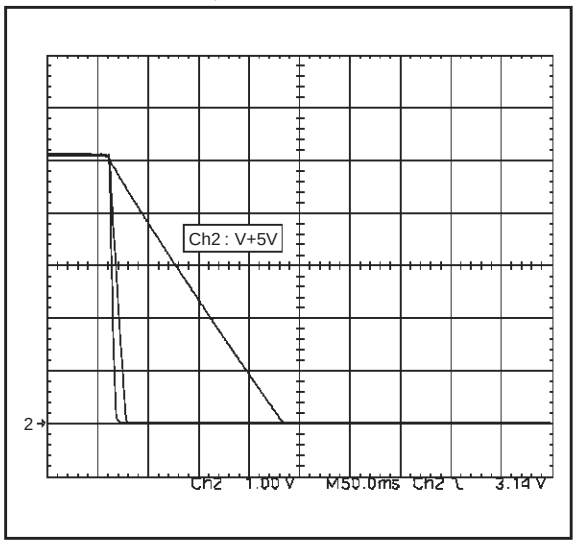


Figure 16: Falling waveforms at shut down for 100mA, 1A and 2.5A



2.3. Options

Various options can be implemented in order to improve the behavior of this power supply, or to lower its cost. Figure 18 presents the full schematics with all options highlighted. Here is the list of all the available features, with their label on the schematics:

1. Capacitive clamper instead of high voltage zener (CLAMP)
2. Three different types of overvoltage protection (OVP1, OVP2 and OVP3)
3. Decreasing of the input power at low load (PIN)
4. Limiting of the output power capability (IOUTlim)
5. +5V output current capability (IOUT)
6. Modifying the brownout thresholds (VINon)
7. Provision for future evolution of the VIPerX2A family (OVL)

2.3.1 Capacitive clamping

The first option deals with the replacement of the high voltage zener D3 by the R4-C5 network to clamp the drain voltage of the device at turn off. The advantage is a lower price, but with two drawbacks:

– The peak drain voltage is not constant anymore. The worst case is at start up with the maximum input voltage. Figure 17 has been shot with an input voltage of 400VDC and a load of 2.5A.

– An additional power is dissipated at light load in this network, as it is submitted at least to the reflected voltage. With the value indicated on the schematics, the input power increases by about 50mW at the critical output power of 0.5W.

Figure 17: Peak drain voltage at start up with an RCD clamp

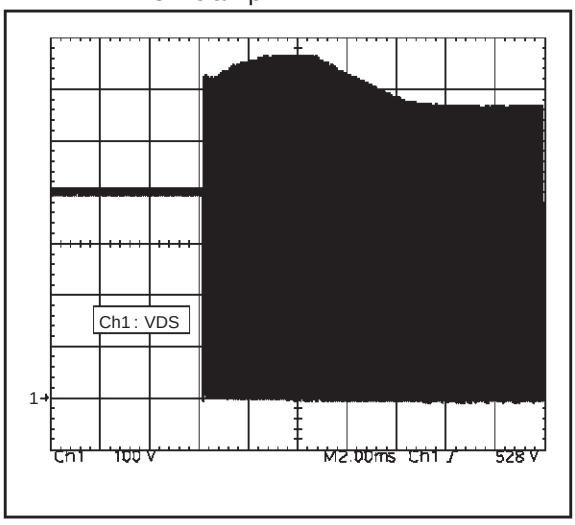
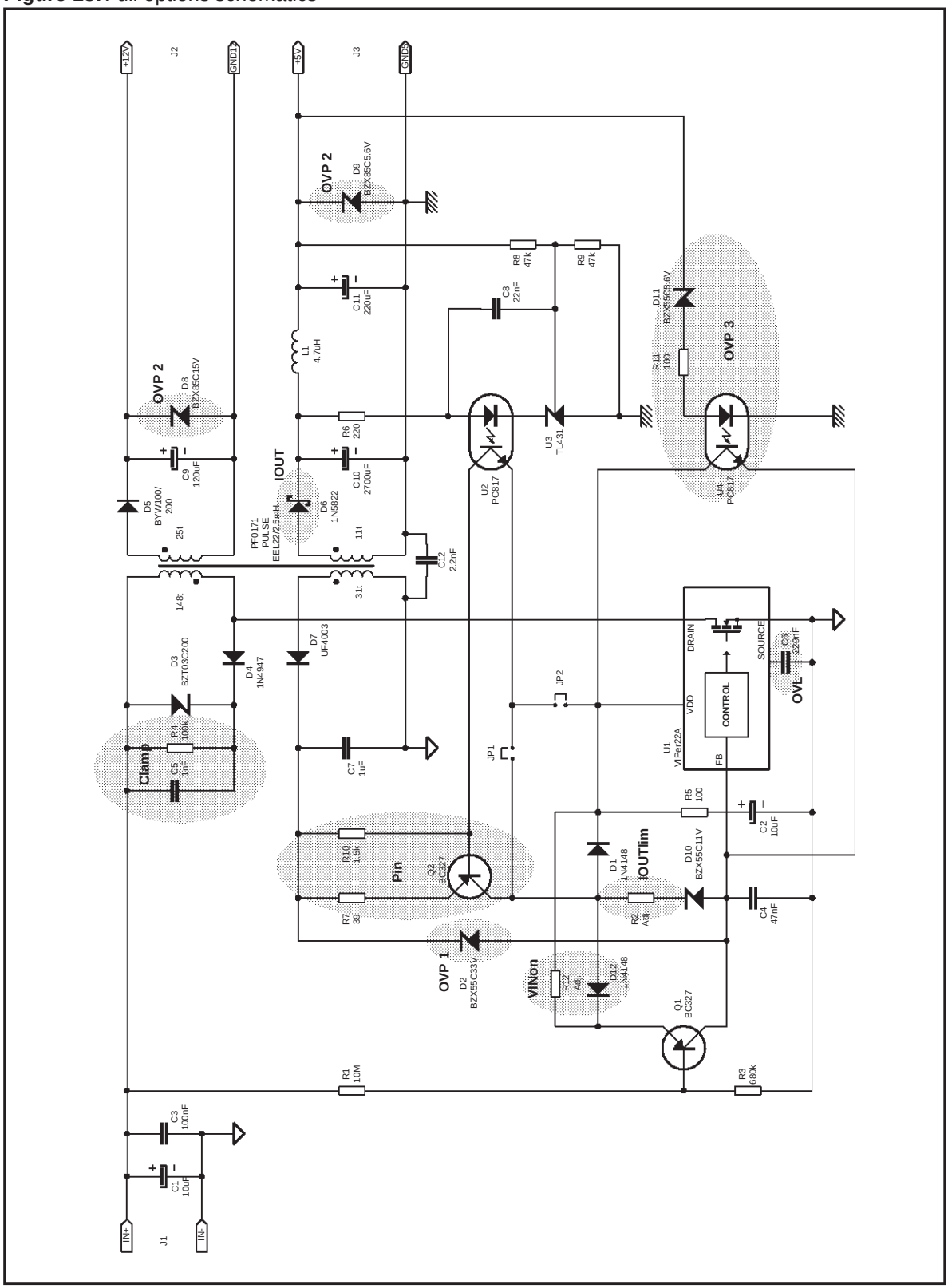


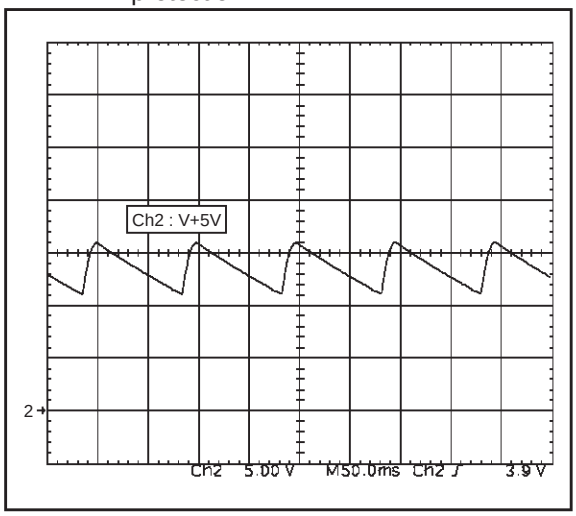
Figure 18: Full options schematics



2.3.2 Overvoltage protection

In case of loss of the secondary feedback, the output voltage could not be controlled anymore, and reaches high values as shown in figure 19. Note that the converter is working in hiccup mode in this condition, as the VIPer22A is no more supplied from the auxiliary winding. This explains the oscillatory behavior of the observed overvoltage.

Figure 19: Overvoltage on the output without any protection



Three different solutions can be implemented to overcome this issue:

– The lowest cost solution consists in implementing a single zener diode D2 between the auxiliary voltage developed across C7 and the FB pin of U1. As soon as the auxiliary voltage - which is an image of the secondary one through the coupling of the transformer - reaches the D2 zener voltage, the peak drain current is limited and the voltage is kept constant on that point. Figure 20 shows a peak voltage at 8V with a load of 100mA. This is not so bad, considering the coupling effect of the transformer which generates high voltages in low load condition.

– Two zener diodes D8 and D9 directly connected on the outputs are able to efficiently clamp the voltages. But they absorb all the power that the converter is able to deliver in overload mode, and they are blown up within a few restart cycles. As this type of zener generally dies in short circuit conditions, the output voltage is still limited, and the converter works in short circuit condition. All this sequence is presented on figure 21. This protection mode may be acceptable, as the initial loss of feedback is already a major board malfunction. The peak voltage reaches almost 7V.

Figure 20: Overvoltage protection with primary zener diode

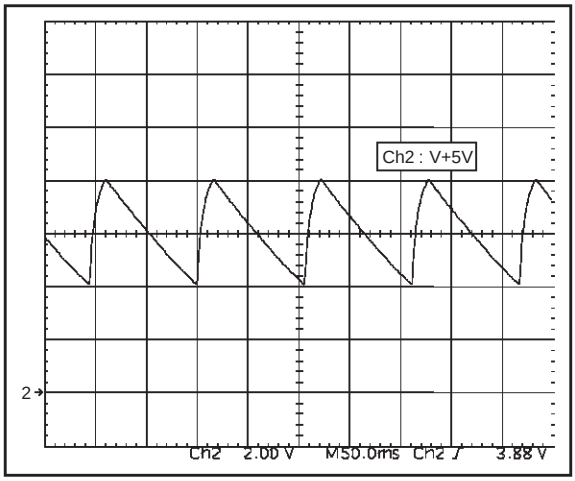
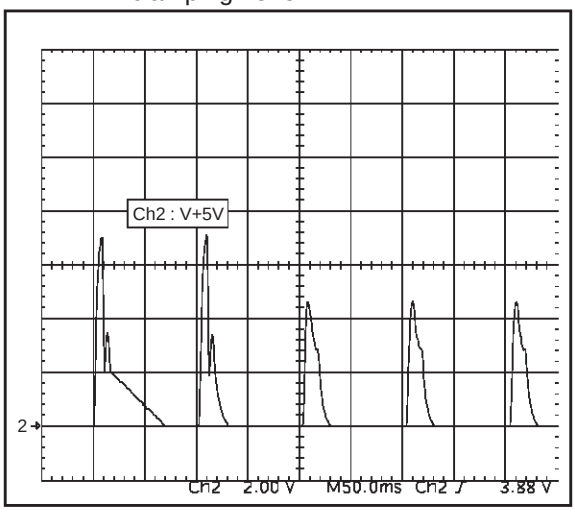
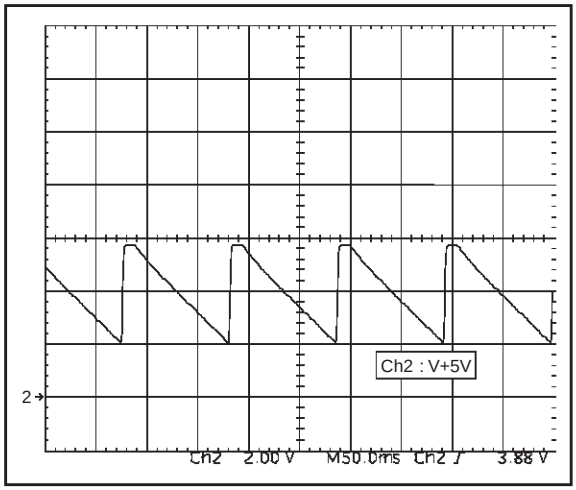


Figure 21: Overvoltage protection with secondary clamping zener



– The secondary control of overvoltage can be also done through a second feedback, using a different optocoupler to prevent any failure in the main loop circuit. A zener diode connected on the +5V output will drive the second optocoupler U4 as soon as the output voltage approaches 6V. As this optocoupler is connected between the FB pin and the VDD pin, it keeps the converter working in hiccup mode because it cannot supply the VDD current to U1. This is shown in figure 22 with a peak voltage below 6V. This protection mode is by far the most efficient, but it is also the most expensive one.

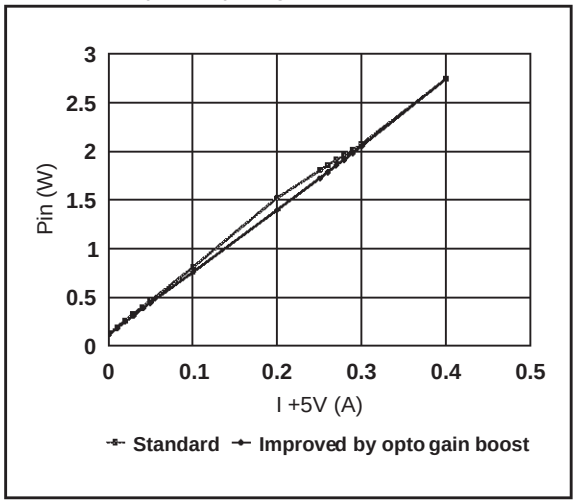
Figure 22: Overvoltage protection with redundant feedback



2.3.3 Input power lowering

The input power can be further reduced versus the results obtained with the standard schematic. The proposed improvement consists in the lowering of the current consumed on the +5V output by the optocoupler which supplies the VDD pin of U1 on primary side. The optocoupler gain is boosted by the mean of a signal PNP bipolar transistor Q2 and two resistances R7 and R10. Also, the optocoupler is directly connected to the VDD pin of the device in order to keep some voltage headroom for its operation. For this purpose, JP1 is open and JP2 is closed. The value of R6 on secondary side is changed to 1kΩ for keeping a reasonable loop gain.

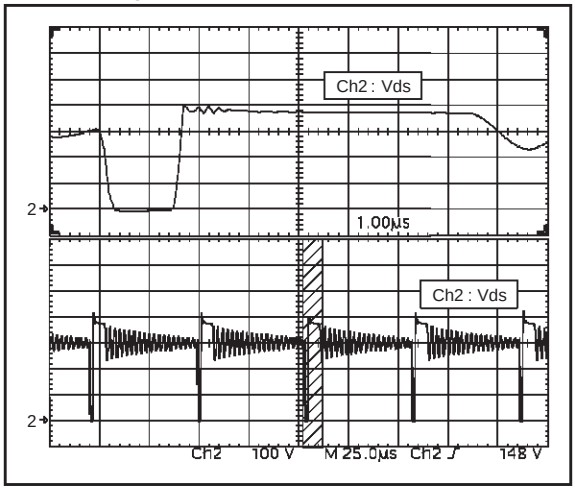
Figure 23: Input power improvement with optocoupler gain boost



The input power improvement is shown in figure 23. The most interesting point is at 0.5W, where the gain is almost 60mW versus the standard schematics. This increases the margin versus the 1W limit by 30%.

Part of this improvement is explained through the reduction of the secondary current drawn from the +5V output for supplying the diode of the optocoupler, but also by a modification of the burst mode occurring in such a configuration. Figure 24 shows the detail of the switching cycle, which is longer. The equivalent overall switching frequency is now 15kHz instead of the previous 30kHz, which lowers the switching losses. This is the other part of the input power improvement, due to a higher ripple on the FB pin. The peak current in the transformer is still sufficiently low to avoid any audible noise.

Figure 24: Switching cycle detail with optocoupler gain boost



2.3.4 Overload current adjustment

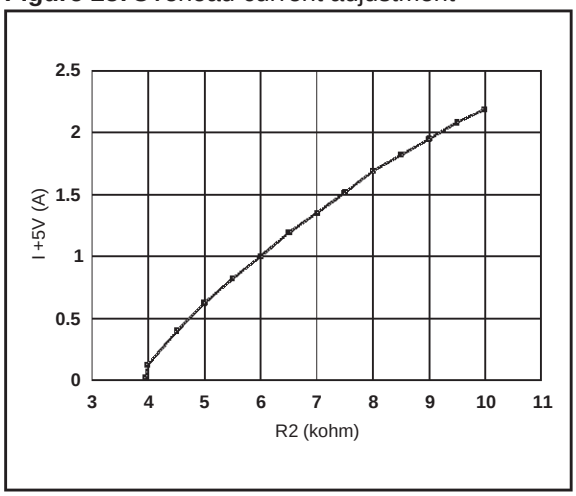
The output current can be limited to a lower value compared to the full capability of the device, thanks to the addition of a resistance R2 in series with the feedback zener diode D10. As the feedback current flows in this network and depends on the peak drain current of the device, the voltage on the anode of D1 will also depend on this parameter which is representative from the output power; The higher is the output power (or current), the lower is the feedback current, and the lower will be the voltage on the anode of D1. As a consequence, the V_{DDoff} threshold where the device stops switching will be reached for a level of output power which can be set through the value of R2. The converter then enters a hiccup mode.

Two modifications are needed to use this feature:

– D10 must be replaced by a lower value in order to let some room for R2 to develop a sufficient voltage to overcome the inaccuracy of the V_{DDoff} threshold.
– As R2 is in series with the input impedance of the FB pin, it builds a resistive divider which lowers the gain of the feedback loop. This may lead to some instabilities, and R6 must be decreased accordingly.

Figure 25 presents the result obtained by replacing D10 with a 6.8V zener diode, and R6 with a 47Ω resistor. It can be seen that the overload current value can be set in a large range of value, by varying the value of R2 between 4kΩ and 10kΩ.

Figure 25: Overload current adjustment



Values below 4kΩ are useless because the device operates in burst mode for currents lower than 200mA, and so the FB pin current doesn't vary any more according to the output power. This can be observed in the figure, where the output current falls down brutally to zero for a value of 3.95kΩ for R2. For values higher than 10kΩ, the overload current may become relatively inaccurate because the FB current can be very low, and the zener diode D10 is no more correctly biased and its voltage becomes unpredictable. There are other parameters impacting the overload threshold:

– All parameters giving the transfer function between the peak primary current and the output current, i.e. the primary inductance of the transformer, the switching frequency, the output voltage, and part of the efficiency.
– The input voltage, especially when working continuously.
– The current ratio between the FB pin and the DRAIN pin, and the V_{DDoff} threshold.

So, the user must take a particular care to design such a feature in its application, and foresee a sufficient margin to cover all the possible variations impacting the final result.

2.3.5 Output current capability

The standard schematics are able to deliver more than 3A on the +5V output, with no load on the +12V one. If this full current is needed, the user must take care to replace the diode D6 with an STPS745 able to withstand the corresponding dissipation. The standard diode 1N5822 in axial package will reach a very high temperature and may blow up.

The printed circuit board of the demoboard has a double footprint to accommodate both of them.

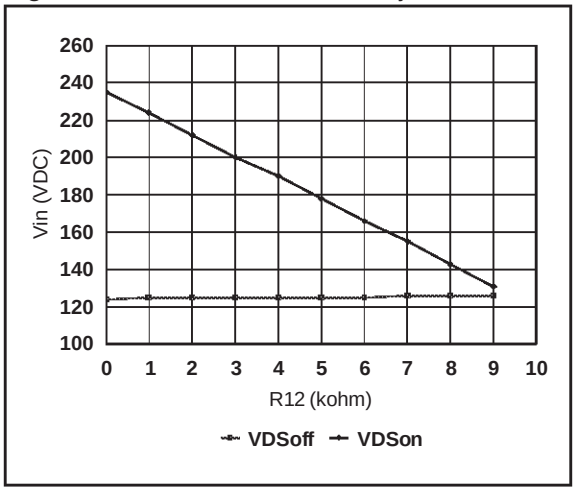
2.3.6 Brownout thresholds adjustment

The standard schematic proposes a brownout feature whose the thresholds depend on the VDD ones of the VIPer device. So, the ratio between the startup and shutdown thresholds cannot be adjusted. Only both values can be moved at the same time by adjusting the values of R1 and/or R3.

An option requiring an additional diode D12 and resistance R12 allows to modify the startup threshold without modifying the shutdown one. R12 creates a voltage drop together with the starting current of the VIPer device. This voltage is summed up with the voltage fixed by the resistive divider R1/R3 and Q1 so that the startup will occur at a lower input voltage. The shutdown threshold remains unchanged thanks to D12 and depends only on the V_{DDoff} of the VIPer device.

Figure 26 gives the two thresholds versus R12 value. It can be seen that the ratio between them can be adjusted. If the shutdown threshold is to be adjusted as well, then the resistive divider R1/R3 has to be modified.

Figure 26: Brownout thresholds adjustment



Values in excess of 6kΩ should be avoided. The inaccuracy of such a feature can become very large, as it depends on the VDD thresholds and on the startup current of the VIPer device. In any case, the user has to foresee a sufficient margin to cover all the possible variations impacting the final result.

2.3.7 VIPerX2A provision for evolution

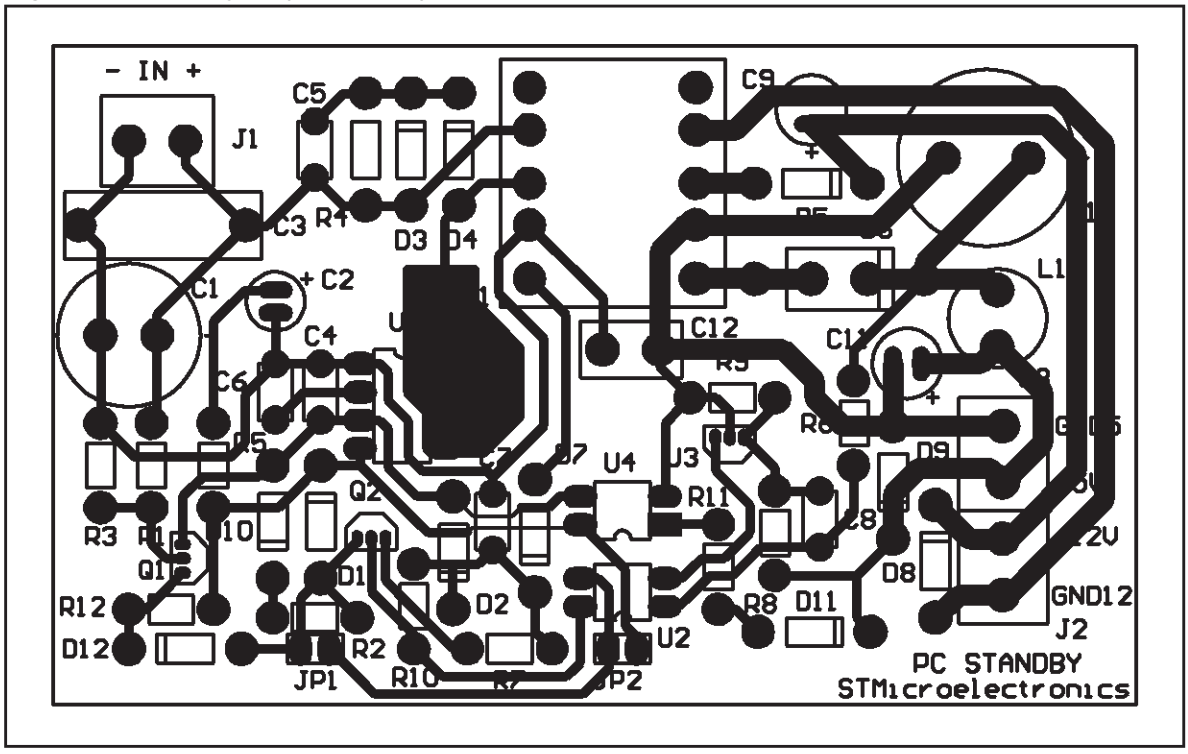
C6 is not provided on the standard schematics, and is replaced by a strap on the demoboard. It will be used by the next generation of VIPerX2A devices, for which one of the SOURCE pin will be dedicated to overload protection. An external capacitor connected on this pin will delay the protection.

3. DEMOBOARD DESCRIPTION

3.1. Board layout

It is a single layer type with copper on bottom side, and serigraphy on top side. Both of them are represented in figure 27.

Figure 27: Board layout (not in scale)



3.2. Bill of material

Table 3 gives the list of all components for the standard configuration, but also for all the options described in par. 2.3. The board comes in the standard configuration.

Table 3: Bill of material

	Standard	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6	Option 7
C1	10 µF / 450 V							
C2	10 µF / 35 V							
C3	100 nF / 250 VAC							
C4	47 nF							

	Standard	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6	Option 7
C5	Not fitted	1 nF / 250 VAC						
C6	Strap							220 nF
C7	1 µF							
C8	22 nF							
C9	120 µF / 25 V							
C10	2700 µF / 6.3 V							
C11	220 µF / 10 V							
C12	2.2 nF / 1kV Ycap							
D1	1N4148							
D2	Not fitted		BZX55C 33V (Note 2)					
D3	BZT03 C200	Not fitted						
D4	1N4947							
D5	BYW100 /200							
D6	1N5822					STPS745		
D7	UF4003							
D8	Not fitted		BZX85C 15V (Note 2)					
D9	Not fitted		BZX85C 5.6V (Note 2)					
D10	BZX55C 11V				BZX55C 6.8V			
D11	Not fitted		BZX55C 5.6V (Note 2)					
D12	Not fitted						1N4148	
J1	2 pts / 0.2" connector							
J2	2 pts / 0.2" connector							
J3	2 pts / 0.2" connector							
JP1	Strap			Not fitted				
JP2	Not fitted			Strap				
L1	4.7 µH / 3 A							
Q1	BC327							
Q2	Not fitted			BC327				
R1	10 MΩ							
R2	Strap				4 -10 kΩ			

	Standard	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6	Option 7
R3	680 kΩ							
R4	Not fitted	100 kΩ / 1/2 W						
R5	100 Ω							
R6	220 Ω			1 kΩ	47 Ω			
R7	Not fitted			39 Ω				
R8	47 kΩ							
R9	47 kΩ							
R10	Strap			1.5 kΩ				
R11	Not fitted		100 Ω (Note 2)					
R12	Strap						0 - 9 kΩ	
T1	Transf. PF0171 PULSE							
U1	VIPer22A							
U2	PC817							
U3	TL431							
U4	Not fitted		PC817 (Note 2)					

Note 1: All resistances are 1/3 W rated, unless otherwise noted

Note 2: Only one of the groups of components D2, D8-D9 or D11-R11-U4 should be fitted at the same time

3.3. Transformer specification

The transformer has been designed and manufactured by PULSE. It is wound on an EEL22 core.

The electrical, mechanical and winding specification are given in figures 28, 29 and 30.

Figure 28: Electrical specification

FINAL OUTLINE NOTES
ALL DIMENSIONS ARE IN MM

ELECTRICAL CHARACTERISTICS:
(FOR REFERENCE ONLY. USED FOR CUSTOMER INFORMATION.)

ITEM	SPECIFICATIONS	TEST CONDITIONS	VALUE		UNIT
1	INDUCTANCE	10kHz–100mV	/	2.5 ±10%	mH
2	LEAKAGE INDUCTANCE (2–3) WITH (9'–8), (7'–6), SHORTED	100kHz–100mV	MAX	40	µH
3	CAPACITANCE (2–3) TO (6–7–8–9)	100kHz–100mV	MAX	70	pF
3	WINDING CAPACITANCE (2–1)	1MHz–1V	MAX	5.5	pF
4	HIPOT (2–3) TO (8–7)+(6–5)+(3–4)	/ /	/	2500 Vac	1Sec
5	HIPOT (2–3)+(9–8)+(7–6)+(4–5) TO CORE	/ /	/	2500 Vac	1Sec
6	DCR(2–3)	/	MAX	4	Ohms
6	DCR(9–8)	/	MAX	220	mOhms
6	DCR(7–6)	/	MAX	33	mOhms
6	DCR(4–5)	/	MAX	300	mOhms
7	RATIO (2–3)/(4–5)	10kHz–100mV	/	4.78 ±2%	/
7	RATIO (2–3)/(7–6)	10kHz–100mV	/	13.47 ±2%	/
7	RATIO (2–3)/(9–8)	10kHz–100mV	/	5.92 ±2%	/

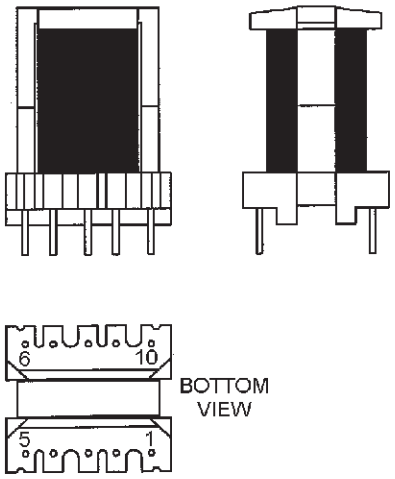


Figure 29: Mechanical specification

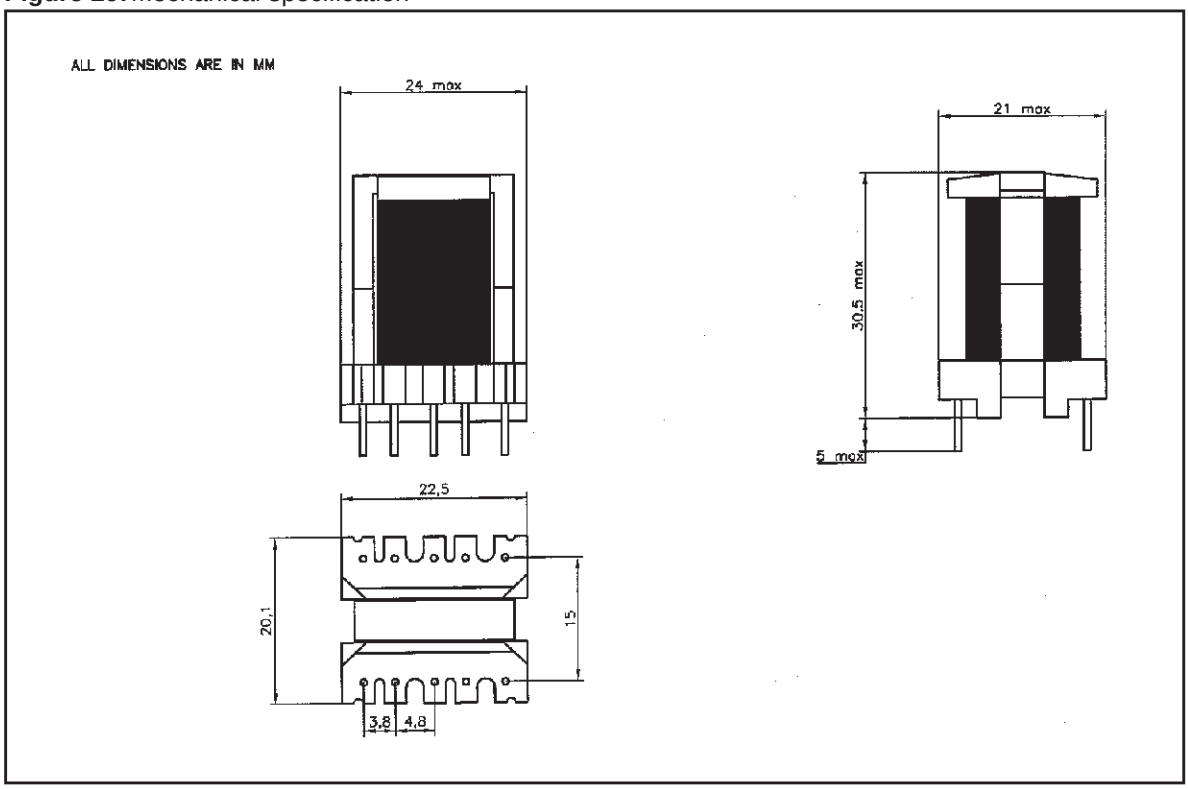


Figure 30: Winding specification