CMOS Sample-and-Hold Circuits

ECE 1352 Reading Assignment

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1. Introduction

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where V_{in} is the input signal, M_1 is an MOS transistor operating as the sampling switch, C_h is the hold capacitor, *ck* is the clock signal, and V_{out} is the resulting sample-and-hold output signal.

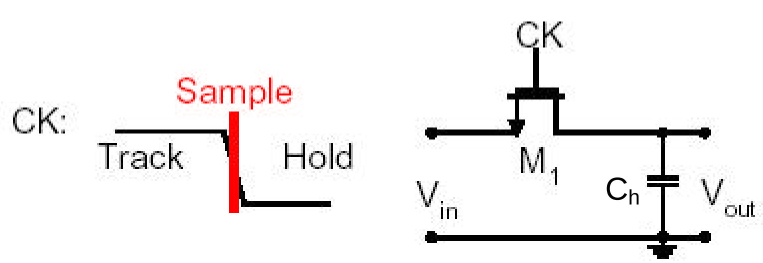

Figure 1: Simplest sample-and-hold circuit in MOS technology.

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows V_{out} to track V_{in}. On the other hand, when *ck* is low, the MOS switch is off. During this time, C_h will keep V_{out} equal to the value of V_{in} at the instance when *ck* goes low [2].

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The next section of this paper explains two major types of errors, charge injection and clock feedthrough, that are associated with this S/H implementation. The section after that presents three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feedthrough. In addition, this paper briefly discusses some of the future researches in S/H circuits.

2. What are Charge Injection and Clock Feedthrough?

2.1.Charge Injection

When a MOS switch is on, it operates in the triode region and its drain-to-source voltage, V_{DS}, is approximately zero. During the time when the transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junctions as depicted in Figure 2 [1].

Figure 2: Channel charge when MOS transistor is in triode region.

For the S/H circuit in Figure 1, if the MOS switch, M_1, is implemented using an NMOS transistor, the amount of channel charge, Q_{ch}, this transistor can hold while it is on is given by equation 1,

$$Q_{ch} = -W\,L\,C_{OX}\left(V_{DD} - V_{tn} - V_{in}\right) \tag{1}$$

where W and L are the channel width and channel length of the MOS transistor, C_{OX} is the gate oxide capacitance, and V_{tn} is the threshold voltage of the NMOS device. When the MOS switch is turned off, some portion of the channel charge is released to the hold capacitor, C_h, while the rest of the charge is transferred back to the input, V_{in}. The fraction, k, of the channel charge that is injected onto C_h is given by equation 2,

$$\Delta Q_{ch} = k\,Q_{ch} = -k\,W\,L\,C_{OX}\left(V_{DD} - V_{tn} - V_{in}\right) \tag{2}$$

As a result, the voltage change at V_{out} due to this charge injection is given by equation 3,

$$\Delta V_{out} = \frac{\Delta Q_{ch}}{C_h} = \frac{-k\,W\,L\,C_{OX}\left(V_{DD} - V_{tn} - V_{in}\right)}{C_h} \tag{3}$$

Notice that ΔV_{out} is linearly related to V_{in} and V_{tn}. However, V_{tn} is nonlinearly related to V_{in} [1, 2]. Therefore, charge injection introduces nonlinear signal-dependent error into the S/H circuit.

2.2.Clock Feedthrough

Clock feedthrough is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of Figure 1, the voltage change at V_{out} due to the clock feedthrough is given by equation 4,

$$\Delta V_{out} = \frac{-C_{para}\left(V_{DD} - V_{SS}\right)}{C_{para} + C_h} \tag{4}$$

where C_{para} is the parasitic capacitance [1]. The error introduced by clock feedthrough is usually very small compare to charge injection. Also, notice that clock feedthrough is signal-independent which means it can be treated as signal offsets that can be removed by most systems. Thus, clock feedthrough error is typically less important than charge injection.

Charge injection and clock feedthrough are due to the intrinsic limitations of MOS transistor switches. These two errors limit the maximum usable resolution of any particular S/H circuit, and in turn, limit the performance of the whole system [1, 3]. New S/H techniques must be developed to reduce these errors.

3. Alternative CMOS Sample-and-Hold Circuits

This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.

3.1.Series Sampling

The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 3 is referred to as series sampling because the hold capacitor is in series with the signal [4, 5].

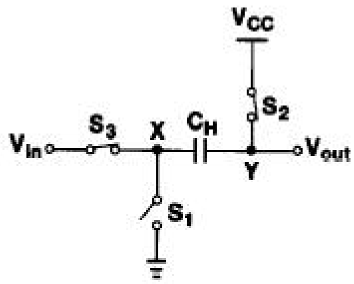

Figure 3: Series sampling.

When the circuit is in sample mode, both switches S_2 and S_3 are on, while S_1 is off. Then, S_2 is turned off first, which means V_{out} is equal to V_{CC} (or V_{DD} for most circuits) and the voltage drop across C_h will be $V_{CC} – V_{in}$. Subsequently, S_3 is turned off and S_1 is turned on simultaneously. By grounding node X, V_{out} is now equal to $V_{CC} – V_{in}$, and the drop from V_{CC} to $V_{CC} – V_{in}$ is equal to the instantaneous value of the input. As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage.

Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because S_2 is turned off before S_3. Thus, the fact that the gate-to-source voltage, V_{GS}, of S_2 is constant means that charge injection coming from S_2 is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*. This parasitic capacitance introduces distortion to the sample-and-hold value, thus mandating that C_h be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of V_{out} in series sampling is being reset to V_{CC} (or V_{DD}) for every sample, but this is not the case for parallel sampling [4, 5].

3.2 Switched Op-Amp Based Sample-and-Hold Circuit

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected.

Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 4, is proposed by [1].

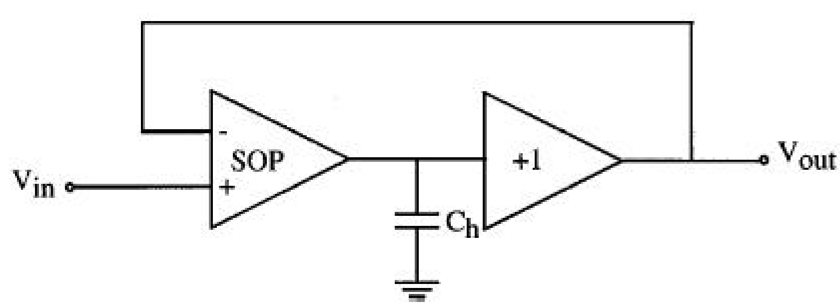

Figure 4: Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on C_h to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on C_h to the output of the S/H circuit.

An example of the SOP based S/H circuit is shown in Figure 5, in which the SOP is implemented using a switched version of the folded cascode op-amp [1].

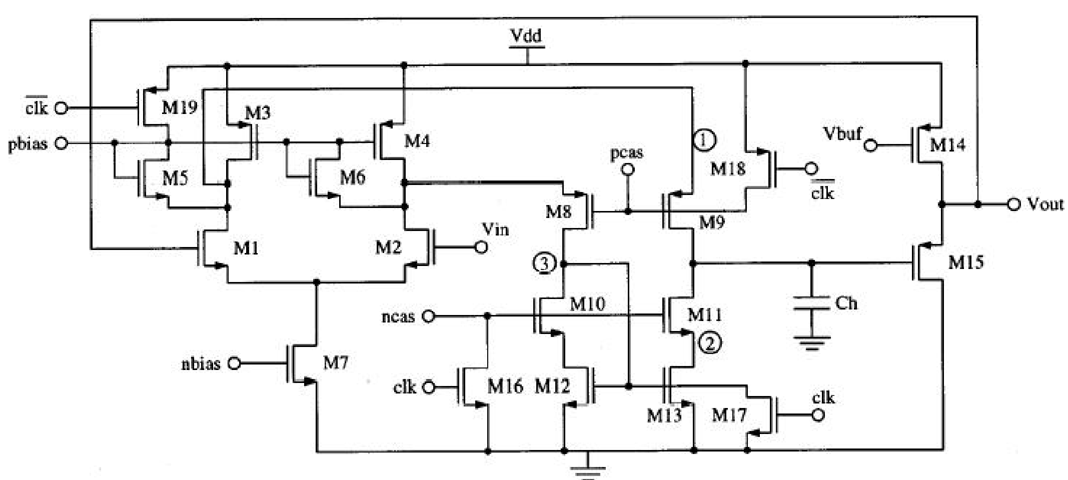

Figure 5: Sample-and-hold circuit with switched folded cascode op-amp.

Transistors M_1 through M_{13} form the regular enhanced slewrate folded cascode op-amp, while M_{14} and M_{15} make up the unity gain output buffer. Transistors M_{16} to M_{19} are added to turn the SOP off at the end of sample mode.

Since charge injection no longer exists in the SOP based S/H circuit, the only source of error is clock feedthrough. Clock feedthrough in this SOP based implementation is caused by the overlap capacitance of M_9 and M_{11}. In order to minimize this error, the channel widths of M_8, M_9, M_{10} and M_{11} should be kept as small as possible. As mentioned in Section 2.2, clock feedthrough is a signal-independent error and can be treated as an offset. By creating a pseudo-differential version of the SOP base S/H circuit, such as that depicted in Figure 6, in which the two circuit halves are matched, this offset can be canceled out. Therefore, the SOP based S/H circuit can be free of both charge injection and clock feedthrough errors [1].

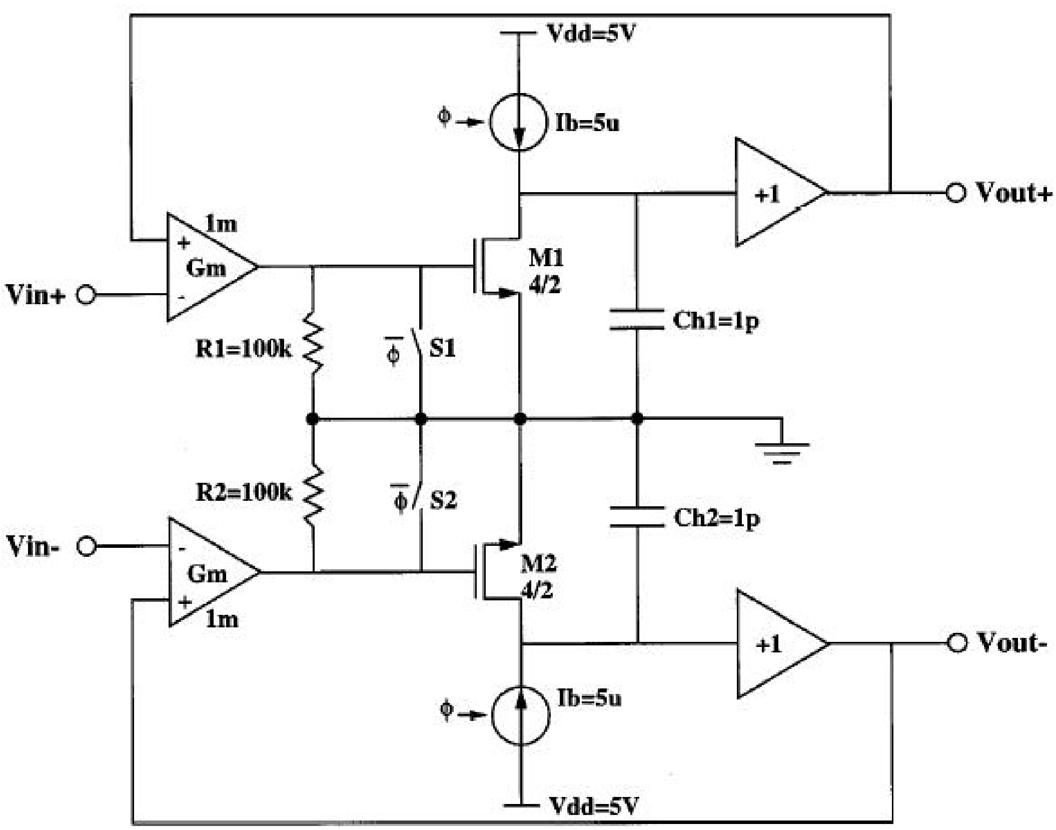

Figure 6: Pseudo-differential switched op-amp based sample-and-hold circuit.

Fabricated in a 2μm CMOS process, measurement results showed that the sinusoidal continuous-time signal and the sample-and-hold output of the pseudo-differential SOP based S/H circuit aligned perfectly with no noticeable nonlinear errors or offset. In addition, the frequency spectrum of this circuit showed that the harmonics is 78dB below the signal and in the noise floor, indicating the superior performance of this S/H circuit [1].

3.3 Bottom plate Sample-and-Hold Circuit with Bootstrapped Switch

Bottom plate sampling configuration is shown in Figure 7 [3].

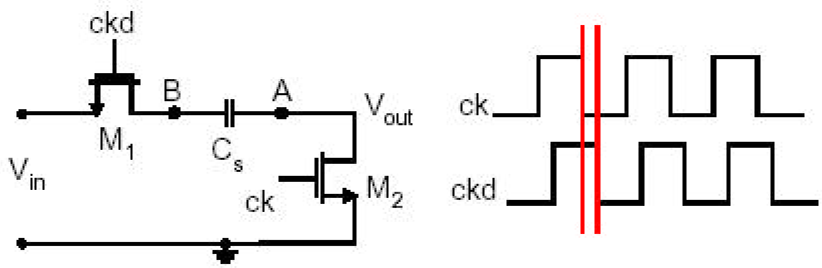

Figure 7: Bottom plate sampling configuration

In this configuration, when both *ck* and *ckd* are high, the output, V_{out}, tracks the input, V_{in}. Then, *ck* goes from high to low first, therefore turning M_2 off. At this time, the voltage at node *A* is zero and node *B* is at V_{in}. Since both the drain and the source of M_2 have a fixed potential, the charge injection caused by M_2 when it turns off is signal-independent and can be regarded as an offset error voltage. Next, *ckd* goes from high to low, turning M_1 off. The voltage drop, V_{AB}, across the sampling capacitor, C_s, is now $-V_{in}$ plus the channel charge injected by M_2. Disconnecting C_s from the input has the effect of isolating the input for the output. On top of that, although the charge injection due to the turning off of M_1 is signal-dependent, the injection does not alter the charge stored on C_s. This is because node *A* is already left floating and, thus, the voltage drop across C_s remains unaffected. Therefore, based on the above analysis, this S/H circuit suffers from a fixed charge injection error and a fixed clock feedthrough error. Both of these errors can be eliminated through a differential configuration.

To further eliminate the nonlinearity of the MOS switches and signal-dependent charge injection, bootstrapped switches can be used instead. Figure 8 shows the circuit configuration of a bootstrapped switch [3].

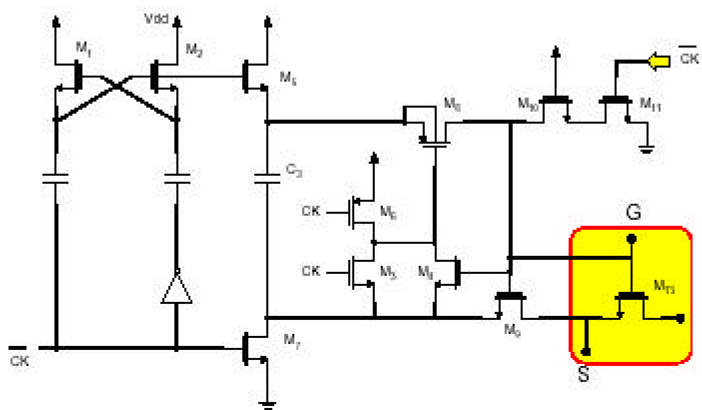

Figure 8: Bootstrapped switch circuit.

A bootstrapped switch can be thought of as a single NMOS transistor. When the bootstrapped switch is in the off state, the switch is cutoff. At the same time, C_3 is charged to V_{DD}. When it is in the on state, C_3 is switched across the gate and source terminals of the "effective transistor," M_{13}. As a result, the gate-to-source voltage, V_{GS}, of M_{13} becomes relatively independent of the input signal. Therefore, the charge injection of the bootstrapped switch is much less signal-dependent than a simple MOS transistor.

Combining the bottom plate S/H technique and the bootstrapped switch, a fully differential S/H circuit, shown in Figure 9, is proposed by [3].

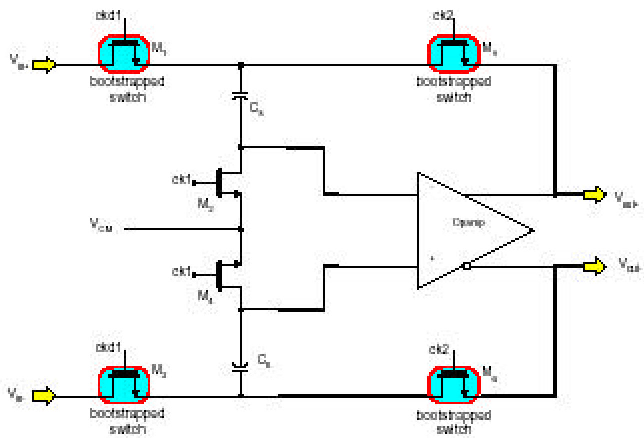

Figure 9: Fully differential sample-and-hold circuit.

In this circuit, *ck1* and *ck2* are two non-overlapping clocks, and *ckd1* is a slightly delayed version of *ck1*. When *ck1* is high, V_{in} is sampled differentially onto the two C_s capacitors. When *ck2* is high, the op-amp operates in a unity-gain configuration and the op-amp output, V_{out}, will be equal to V_{in}. Since this S/H circuit has a differential configuration, both clock feedthrough and charge injection, which is fixed for the bottom plate S/H technique, can be eliminated.

Unfortunately, this proposed fully differential S/H circuit has yet to be fabricated. Thus, no real measurement results can be obtained. However, as indicated by [3], the circuit was simulated in Cadence Analog Artist with TSMC 0.18μm CMOS process with a switched-capacitor inter-stage amplifier having a gain of 2. Since this type of op-amp is popularly used in pipelined ADCs, in some sense, the simulation environment does model reality. Simulation results showed that for a 10-bit resolution, the gain error is about 0.08%, which is less than the requirement of ±0.1%. Thus, the proposed fully differential bottom plate S/H circuit with bootstrapped switches might be able to perform wonderfully in reality.

4. Future Developments of Sample-and-Hold Circuits

With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important [3]. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits [6]. As a result, better and faster S/H circuits must be developed.

At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog circuits are now shifted from voltage-mode to current-mode. The advantages of current-mode circuits include low-voltage, low-power, and high-speed [7]. Therefore, future researches of S/H circuit should also shift toward current-mode S/H techniques.

5. Conclusion

Sample-and-hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feedthrough restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Although, this paper has described three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order to meet the increasing demand for high-speed, low-power, and low-voltage S/H circuits for data acquisition systems.

6. Reference

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