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Design of a Digital Camera with CoolRunner-II CPLDs

Summary

This document describes a digital camera reference design using a CoolRunner-II™ CPLD. The low power capabilities of CoolRunner-II CPLD devices make them the ideal target for portable, handheld applications such as digital cameras. The complete reference design is available for download in "VHDL Code," page 18.

Introduction

Digital cameras have become increasingly popular over the last few years. Digital imaging technology has grown to new markets including cellular phones and PDA devices. With the diverse marketplace, a variety of imaging technology must be available. Imaging technology has expanded to include both charge-coupled device (CCD) and CMOS image sensors.

One of the leaders today in digital imaging technology is Micron Technology, Inc. The products available from Micron include CMOS image sensors that range from CIF-size to 1.3 megapixel sensors that achieve CCD quality images. For more information on Micron Technology refer to "References," page 19.

Video Formats

Until recently, most video equipment was designed for analog video. Today, digital video has become increasingly available in consumer applications. The most common digital video formats include RGB and YCrCb. RGB is the digital version of the analog RGB signal, while YCrCb is the digital version of analog YUV and YPbPr video signals.

The structure of a video stream is actually a series of still images or frames. Video is measured by frames per second or fps. Typical video is about 60-70 fps. Each frame is composed of lines of data. The size of an image is determined by the number of lines per frame and the number of data pixels in each line. For instance, a VGA size image is 480 lines of data that contain 640 pixels of data in each line. So the corresponding VGA image size is 640 x 480 = 307,200 pixels. For more information on digital video formats refer to "References," page 19.

Digital Imaging

CMOS vs. CCD

A CMOS or CCD image sensor provides the technology to digitally capture an image and/or streaming video. CCD image sensors are used in many high end applications, such as high-resolution digital cameras. CCD image sensors provide a better picture in low-light environments over CMOS image sensors, but can be costly to manufacturer and integrate into a system.

CMOS image sensors draw much less power than CCDs. The digital camera system is able to run longer on batteries, a major advantage in handheld products. Since CMOS sensors use the same manufacturing platform as most microprocessors and memory chips, they are easier to produce and more cost effective than CCDs. CMOS image sensors require a single power supply for operation and only 20-50 milliwatts per pixel output.

Micron MI-SOC-0343

The image sensor utilized in this digital camera reference design was manufactured by Micron Technology, Inc. The MI-SOC-0343 is a complete CMOS image sensor camera-on-chip solution. The MI-SOC-0343 incorporates an "active pixel" sensor architecture core, plus a digital image processor or IFP. The MI-SOC-0343 can output digitally processed RGB or YCrCb data. This CMOS image sensor is a 640 x 480 VGA size sensor and has over 100 programmable registers for customizing. Figure 1 illustrates a block diagram of the MI-SOC-0343 image sensor.

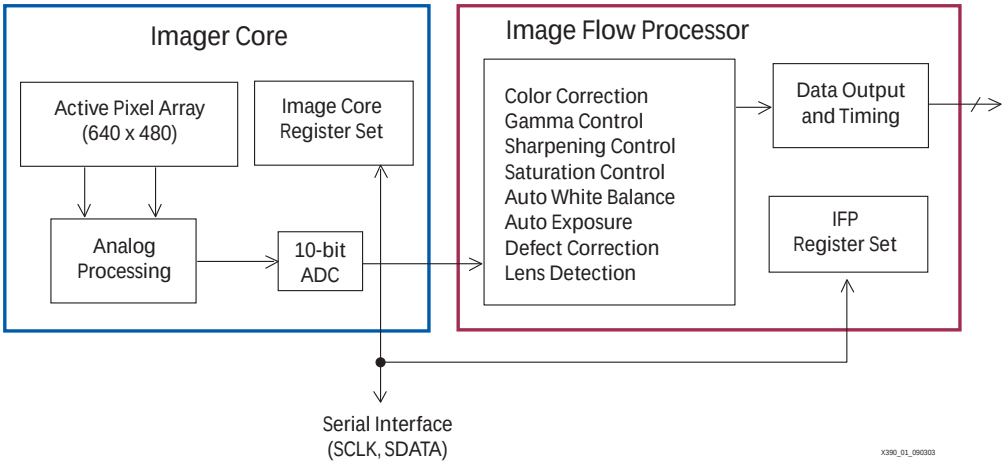
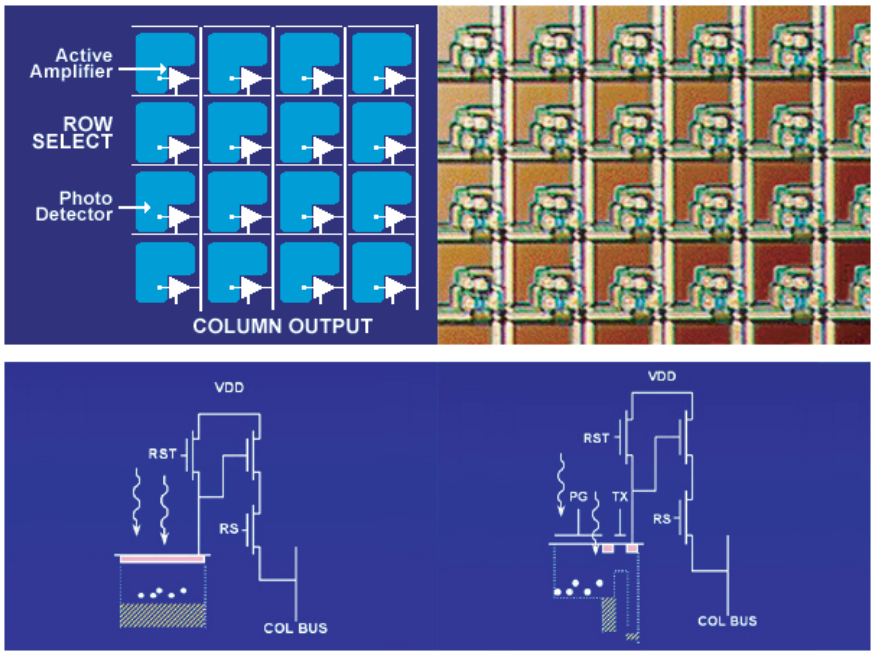


Figure 1: **MI-SOC-0343 Block Diagram**

Active Pixel Architecture

The "active pixel" architecture is shown in Figure 2. The "active pixel" architecture consists of an amplifier dedicated to each photodiode in the image array. The sensor photodiode is the area of the silicon that detects light. In a CMOS image sensor, the photosite area is about 75% (or commonly referred to as the sensor fill factor). The active amplifier circuitry consumes

approximately 25% of the die area. The "active pixel" architecture developed by Micron eliminates background noise and prevents image effects such as "line streaking".



Photodiode Active-Pixel Architecture

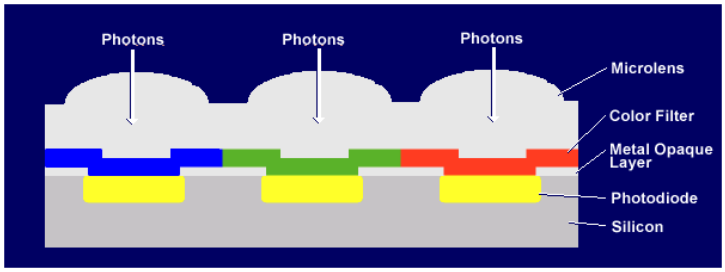
Photogate Active-Pixel Architecture

Images courtesy of Micron

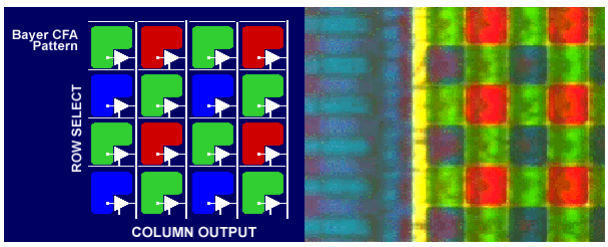
Figure 2: **Active Pixel Architecture**

Bayer CFA

Each photosite in the "active pixel" sensor array can detect light. It is necessary, however, to distinguish between colors. The Bayer Color Filter Array (or CFA) was invented to independently measure red, green, and blue photons. The Bayer CFA is an repeating 2x2 matrix in the image array to measure each color. Diagrams in Figure 3 illustrate aspects of the Bayer CFA.



G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G
G	R	G	R	G	R	G	R
B	G	B	G	B	G	B	G



Images courtesy of Micron

Figure 3: **Bayer CFA**

Image Flow Processor

The imager core outputs a raw RGB data stream to the image flow processor (or IFP) of the MI-SOC-0343. The IFP is responsible for interpolating one color per pixel into three colors per pixel by filling in missing data based on adjacent pixels.

The IFP is responsible for the following functions:

- Color Correction: Corrects or enhances the color of an image by accounting for differences between the image sensor and human eye observations.
- Gamma Control: Corrects the image for observation on an LCD.
- Sharpening Control
- Saturation Control: Controls the amount of gray in a color.
- Auto White Balance
- Auto Exposure
- Defect Correction: Substitutes pixel defects (single dark or bright pixels) with neighboring pixel data.
- Lens Detection
- Zoom Features: Allows the image size to be larger or smaller.

Digital Video Capture

The IFP can output either 4:2:2 YCrCb (CCIR656) or 4:4:4 565RGB data. Data is sampled out of the IFP according to the vertical and horizontal control signals as shown in Figure 4. The signal, PIX_CLK, is the sample clock from the MI-SOC-0343. The signal, FRAME_VALID, is the vertical synchronization control and the signal, LINE_VALID, is the horizontal synchronization control from the MI-SOC-0343. Both data output formats, YCrCb and RGB are shown for an 8-bit data bus from the image sensor.

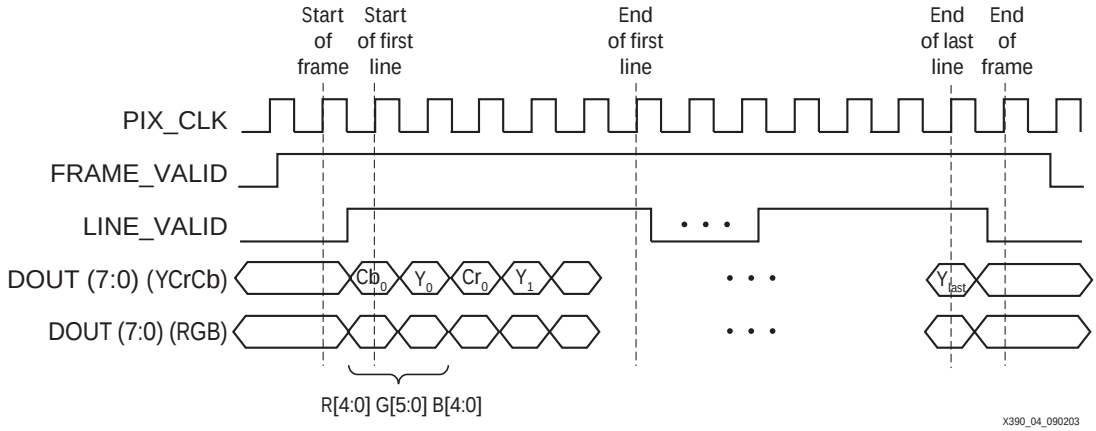


Figure 4: **Video Capture Timing**

LCD Technology

In a digital camera design, the captured image from the sensor may be stored in a memory component. It is necessary to send this image data to either a peripheral device or a display. In a digital camera application, an LCD or liquid crystal display is the desired solution. The best display for video applications is a color active matrix TFT (or thin film transistor). Most TFT modules offer display resolution with sub-pixels. This allows each pixel to individually display three colors per pixel or each red, green, and blue color.

The two main types of LCD polarization include: transmissive or transflective. Transmissive LCDs require a backlight that allows light to shine through the back of the LCD and activate

pixels in the display. Transflective LCDs have a specific type of backing that allows light to shine through the back of the LCD as well as reflect light from the front of the LCD.

Most TFT LCDs have integrated IC drivers that connect in a grid pattern to access all pixels in the display. With this type of integration, the LCD can be driven through a digital parallel data interface.

The LCD selected in this CoolRunner-II digital camera reference design is manufactured by Optrex of America, Inc. For more information on Optrex refer to "References," page 19. The display in this reference design is part # T-51382D064J-FW-P-AA. This display is an 6.4" transmissive color active matrix TFT. The display has an integrated driver and is accessible through a parallel 6-bit RGB data interface. The display resolution is VGA size or 640 x (RGB) x 480. This Optrex display is a dual CCT or cold cathode tube display. A block diagram of the Optrex 51382 device is shown in Figure 5.

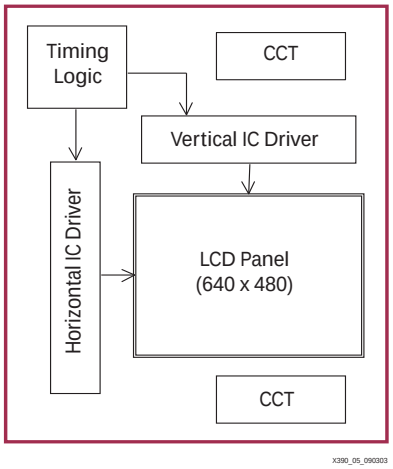


Figure 5: **Optrex Block Diagram**

CoolRunner-II Design

The complete CoolRunner-II digital camera reference design is shown in Figure 6. The CoolRunner-II CPLD is the central controller for the camera design. The CPLD is responsible for capturing data from the Micron image sensor, storing the image data in SRAM, and sending the image data to the Optrex display. The CPLD is also responsible for initializing the Micron image sensor through a configurable register set. The CPLD is also responsible for generating the PWM pulse that controls the brightness of the Optrex LCD. An inverter controls the voltage applied to the CCT of the Optrex display.

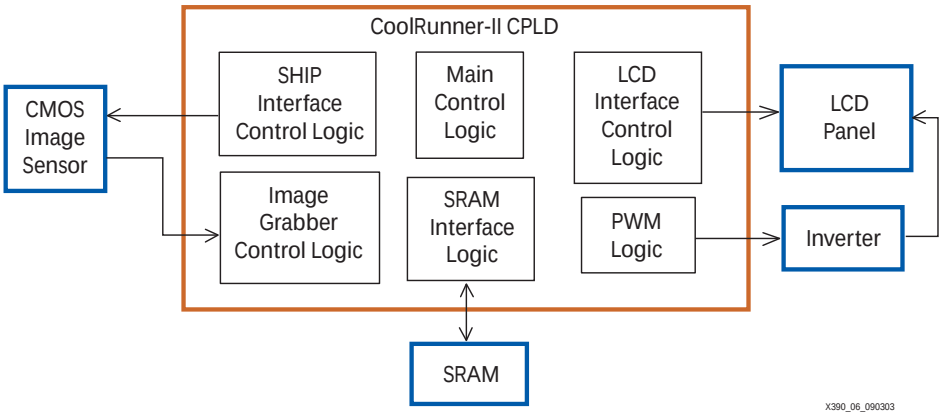


Figure 6: **Digital Camera Block Diagram**

Main Control Logic

The Main Control Logic block shown in Figure 6 is responsible for the high level operation of the digital camera. This module starts the initialization of the image sensor by releasing control of the SHIP Interface Logic. After initialization is complete, the Main Control Logic starts capturing image data by asserting a get_frame_data flag. Once the Image Grabber Logic has captured an image and stored the image data in SRAM, a get_data_done flag is asserted. The Main Control Logic then gives control to the LCD Interface module that reads data from SRAM and send the image data to the LCD module. These steps are shown in Figure 7, an illustration of the Main Control Logic state machine. The current implementation of the Main Control Logic state machine is setup for streaming video. Future implementation includes adding user inputs to capture still images.

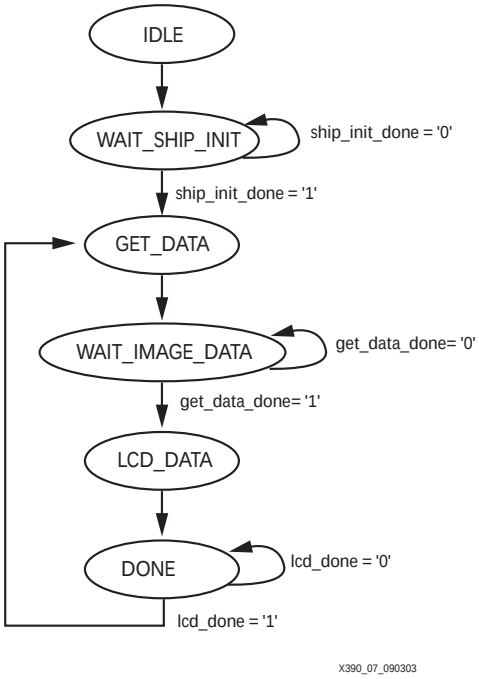


Figure 7: **Main Control Logic State Machine**

SHIP Interface Control Logic

The SHIP Interface Control Logic is responsible for writing all the necessary registers of the Micron image sensor upon power up of the camera module. This includes both imager core registers and IFP registers. Communication to registers on the MI-SOC-0343 is done via a serial link with two signals, SCLK and SDATA. This Serial Host Interface Protocol, or SHIP is similar to the I2C standard. In this implementation, the MI-SOC-0343 is the slave device while the CoolRunner-II CPLD is the master device.

The SCLK and SDATA serial lines are externally terminated to 3.3V with a 1.5 K ohm resistor. Either the master or slave device can pull the line down for communication. The clock frequency of SCLK is approximately 100 KHz.

The SHIP protocol for writing a specific register of the MI-SOC-0343 is as follows (shown in Figure 8):

1. Start condition.
2. Send slave device 8-bit address (Value = B8 (hex) for a MI-SOC-0343 write condition).
3. An acknowledge bit is sent by slave device.
4. Master sends the 8-bit register address.
5. An acknowledge bit is sent by the slave device.

6. Master sends upper 8-bits of data.
7. An acknowledge bit is sent by the slave device.
8. Master sends lower 8-bits of data.
9. An acknowledge bit is sent by the slave device.
10. Master stops operation with a stop condition.

A start condition is defined as a HIGH to LOW transition on SDATA, while SCLK is HIGH. A stop condition is defined as a LOW to HIGH transition on SDATA, while SCLK is HIGH. Figure 8 illustrates the timing for a write sequence to IFP register 01 (hex) with a value of 0004 (hex).

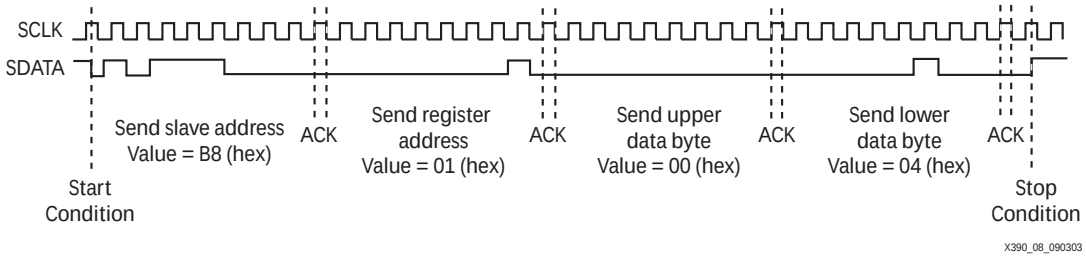


Figure 8: **SHIP Write Sequence**

Refer to the MI-SOC-0343 data sheet for a detailed description of all available registers on the image sensor. Table 1 lists a few of the registers that were utilized in this CoolRunner-II digital camera implementation.

Table 1: **Sample CPLD Register Set**

Register (hex)	Value (hex)	Purpose
IFP 01	0004	Controls register address space for SHIP communication.
IFP 08	DD00	Specifies output timing and format (selects RGB output).
IFP 48	0040	Enables color bar test-pattern generation.
IC 06	000A	Select vertical blanking time (10 rows).
IC 3B	02B0	Sets the on-chip voltage reference.
IC 5F	8984	Used for black level calibration.

Figure 9 illustrates the main components that generate the SHIP interface logic. Upon a system reset, the SHIP interface logic starts to configure the desired registers in the MI-SOC-0343 device. The registers to write in the MI-SOC-0343 are determined at configuration time of the CPLD. All register addresses and data are stored in the CPLD by building a ROM type structure in the PLA (or programmable logic array) of the CoolRunner-II architecture. The SHIP_TOP state machine shown in Figure 9 will sequence through each register write. The

SHIP_INTERFACE block shown in Figure 9 controls the generation of SCLK and SDATA on the SHIP serial communication.

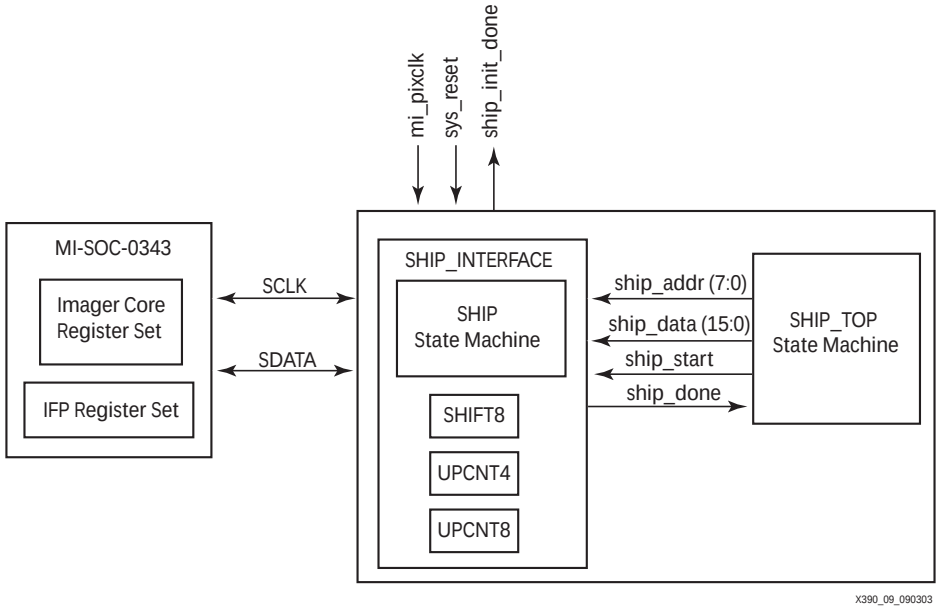


Figure 9: **SHIP Interface Block Diagram**

SHIP Top Level Logic

Figure 10 illustrates the state machine logic for the top level SHIP logic. The top level SHIP logic is responsible for sequencing through the list of desired register writes. This state machine controls which registers of the MI-SOC-0343 are written to upon start up. The top level SHIP logic creates and assigns the register address and data, ship_addr (7:0) and ship_data (15:0) to the SHIP_INTERFACE logic. A register write sequence is initiated with the assertion

of ship_start control signal. When the SHIP_INTERFACE logic has completed the single register write, the ship_done flag is asserted.

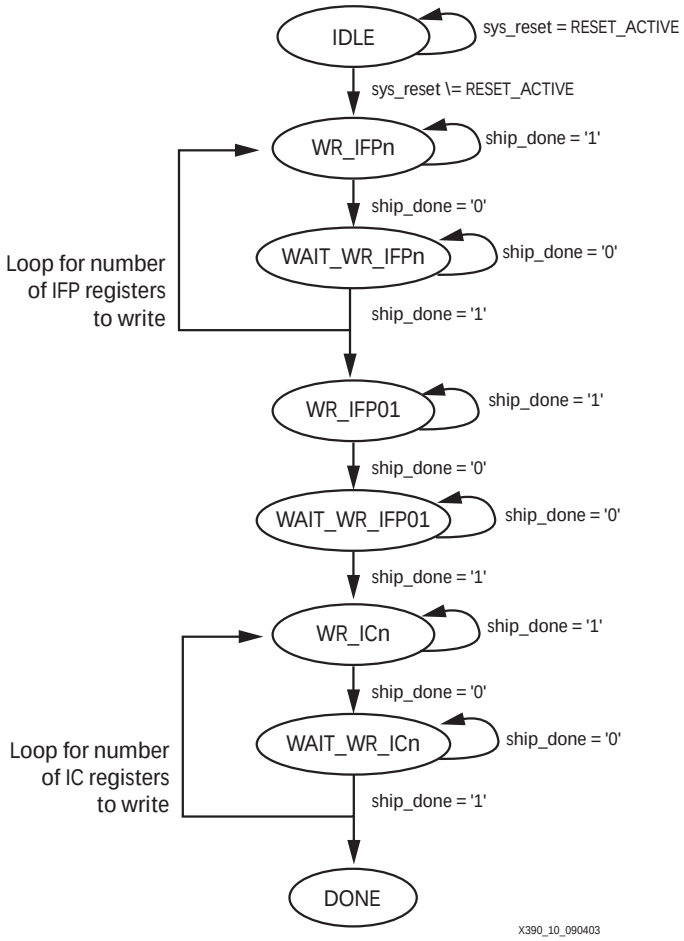


Figure 10: **SHIP Top Level State Machine**

SHIP Interface Logic

Figure 11 illustrates the state machine logic for the SHIP_INTERFACE component. The SHIP_INTERFACE state machine is responsible for loading an 8-bit shift register, SHIFT8 component, with the data to shift out on SDATA. The state machine loads an 8-bit shift register with the MI-SOC-0343 slave address, followed by the register address, followed by the upper data byte, and then concluding with the lower data byte. This sequence is illustrated in Figure 8.

The SHIP_INTERFACE state machine will be repeated for the number of registers being written to initialize the MI-SOC-0343 device. This state machine receives the register address and register data to write on the SHIP serial communication link. The register address is stored in the signal, ship_addr (7:0), provided by the top level SHIP control logic. The register data is stored in the signal, ship_data (15:0), provided by the top level SHIP control logic. The

SHIP_INTERFACE block starts each register write with the assertion of ship_start. When complete, the ship_done flag is asserted back to the SHIP top level logic.

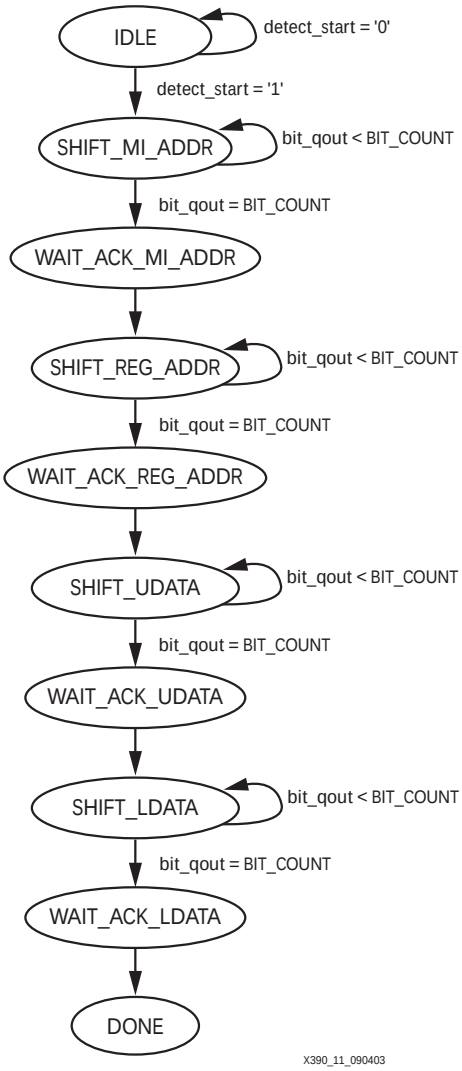


Figure 11: **SHIP Interface State Machine**

When the SHIP Control Logic has completed writing all necessary registers, the ship_init_done flag is asserted back to the Main Control Logic state machine.

SCLK & SDATA Generation

To complete the SHIP Interface Logic, one more state machine is needed. This state machine, SCLK_GEN is responsible for generating the SCLK and SDATA control signals. This state machine provides the required setup and hold times on SDATA with respect to SCLK. This state machine will also generate the start and stop conditions as specified in the SHIP

interface. This state machine will generate the necessary 100 KHz SCLK based on the 13 MHz frequency of the image sensor pixel clock. Figure 12 illustrates the SCLK_GEN state machine.

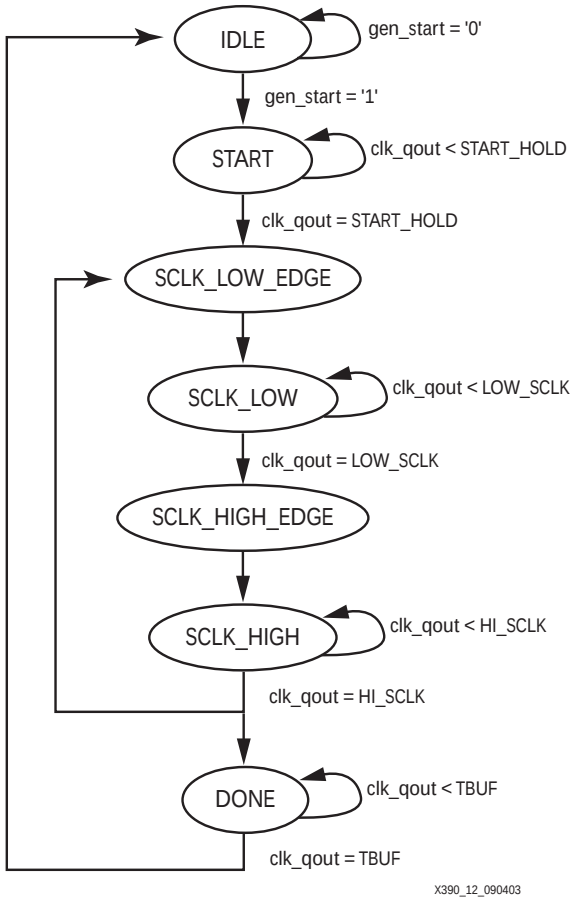


Figure 12: **SCLK_GEN State Machine**

Image Grabber Control Logic

Once the MI-SOC-0343 image sensor is initialized, valid frames can be captured. A single frame can be captured at a time and stored into memory. The defined interface between the CoolRunner-II CPLD and the MI-SOC-0343 device is shown in Figure 13.

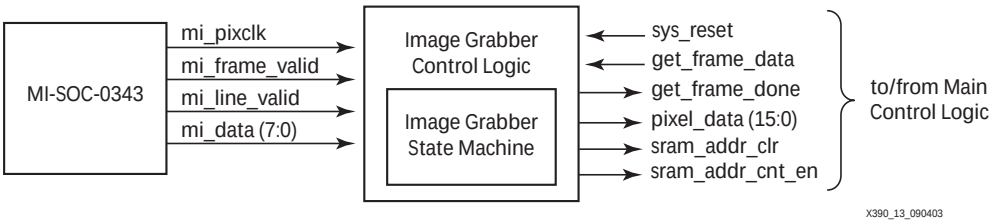


Figure 13: **MI-SOC-0343 Interface**

The Main Control Logic asserts the get_frame_data control signal to the Image Grabber Control Logic to capture a single image from the sensor and store the data in SRAM. The timing

for capturing an image is shown in Figure 4, page 4. The state machine logic for capturing an image is shown in Figure 14.

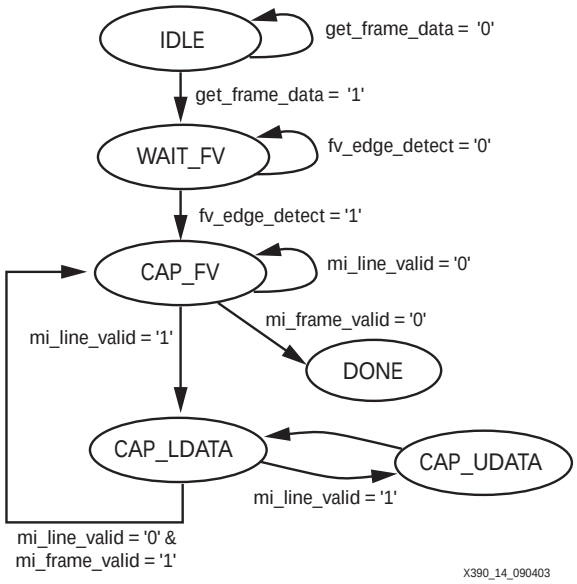


Figure 14: **Image Grabber State Machine**

Table 2 below describes the functionality of each state in the Image Grabber state machine.

Table 2: **Image Grabber State Description**

State Name	Purpose
IDLE	Wait for assertion of get_frame_data control signal.
WAIT_FV	Wait for assertion on rising edge flag of mi_frame_valid signal.
CAP_FV	Wait for rising edge of mi_line_valid. If mi_frame_valid signal is negated, go to DONE state.
CAP_LDATA	Capture lower byte of image data on rising edge of mi_pixclk. If mi_line_valid is still asserted, go to CAP_UDATA state. If mi_line_valid is negated, go to CAP_FV to start data capture for next line of frame. In this state, the pixel data word is written to SRAM by asserting the WEn signal (sram_wen).
CAP_UDATA	Capture upper byte of image data on rising edge of mi_pixclk.
DONE	Assert get_data_done flag.

LCD Interface Control Logic

The CoolRunner-II digital camera reference design uses an LCD to display images captured by the image sensor and stored into memory. The LCD interface in this reference design is a pure digital interface. The data bus is 18-bits wide with 6-bits dedicated to each red, green, and blue color. Special attention must be given to the timing of control signals to the LCD. Incorrect

timing on control signals could create image flicker, image scrolling, or partial image display. The control signals for the Optrex LCD are shown in Table 3.

Table 3: **Optrex LCD Control Signals**

Optrex Signal Name	CPLD VHDL Name	Purpose
CLK	lcd_clk	Clock signal for capturing image data.
VSYNC	lcd_vsync	Vertical synchronous signal.
HSYNC	lcd_hsync	Horizontal synchronous signal.
DENB	lcd_denb	Data enable.
R (5:0)	lcd_red (5:0)	Red image data signal.
G (5:0)	lcd_green (5:0)	Green image data signal.
B (5:0)	lcd_blue (5:0)	Blue image data signal.
R/L	lcd_r_l	Horizontal image shift-direction select signal.
U/D	lcd_u_d	Vertical image shift-direction select signal.

The Optrex LCD TFT is compatible with four types of VGA timing. The various modes are VGA-480, VGA-400, VGA-350, and freedom mode. The polarization of HSYNC and VSYNC determine the VGA timing. In this reference design, the VGA-480 mode is utilized. Table 4 indicates the LCD mode based on polarization of VSYNC and HSYNC.

Table 4: **LCD Mode Select**

Polarization	VGA-480	VGA-400	VGA-350	Freedom Mode
HSYNC	Low	Low	High	High
VSYNC	Low	High	Low	High

The sample clock, CLK, frequency for the Optrex LCD is typically 25 Mhz. In this CoolRunner-II reference design, the LCD clock frequency is 6.6 MHz or 150 ns clock period. The timing parameters shown below in Table 5 and Table 6 will vary based on LCD clock frequency. The values shown correspond to a clock frequency of 6.6 MHz.

The horizontal (or HSYNC) and vertical (or VSYNC) timing for the LCD must be given special consideration. If the timing parameters shown below are not met, the image will not display correctly on the LCD. Effects such as image scrolling or partial image display will occur.

Horizontal Timing

Table 5 and Figure 15 illustrate the horizontal timing specifications for HSYNC. The back porch and front porch times are with respect to the assertion of DENB. When DENB is asserted, data is shifted into the LCD at each rising edge of the LCD CLK.

Table 5: **Horizontal Timing**

Indicator	Description	Parameter	Clock Cycles	Actual Value
A	Horizontal Width	t_{HPW}	96	14 µs
B	Horizontal Back Porch	t_{HBP}	48	7 µs
C	Horizontal Display	t_{HD}	640	96 µs

Table 5: **Horizontal Timing**

Indicator	Description	Parameter	Clock Cycles	Actual Value
D	Horizontal Front Porch	t_{HFP}	16	2.4 µs
E	Horizontal Total	t_{HP}	800	120 µs

For clarification, each timing parameter in Table 5 is assigned a letter shown in Figure 15.

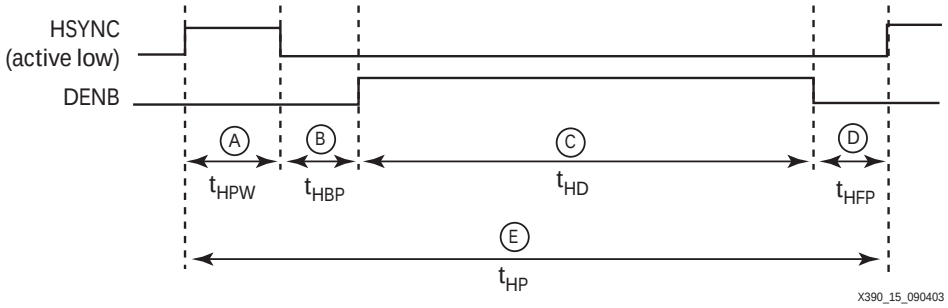


Figure 15: **Horizontal Timing Diagram**

Vertical Timing

Table 6 and Figure 16 below describe the vertical timing parameters for VSYNC. The VSYNC back porch time is with respect to the rising edge of DENB for the first line of image data. The VSYNC front porch parameter is with respect to the falling edge of DENB on the last line of image data. Note the assertion time of DENB in Figure 16 is for shifting data on all lines to the LCD.

Table 6: **Vertical Timing**

Indicator	Description	Parameter	Lines	Actual Value
A	Vertical Width	t_{VPW}	2	240 µs
B	Vertical Back Porch	t_{VBP}	33	3.96 ms
C	Vertical Display	t_{VD}	480	57.6 ms
D	Vertical Front Porch	t_{VFP}	10	1.2 ms
E	Vertical Total	t_{VP}	525	63 ms

The letters in Table 6 correspond to each timing parameter shown in Figure 16.

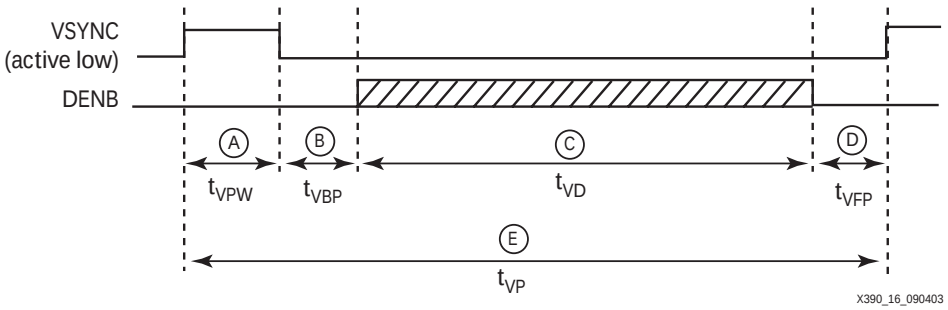


Figure 16: **Vertical Timing Diagram**

Another critical timing parameter on the LCD is the phase difference between active edges of VSYNC and HSYNC. This timing parameter is indicated as t_{VH} and shown in Figure 17. The

minimum value of t_{VH} is one clock cycle. The maximum value of t_{VH} is (t_{HP} - 1) clock cycles, where t_{HP} is the number of clock cycles to shift in an entire line of data.

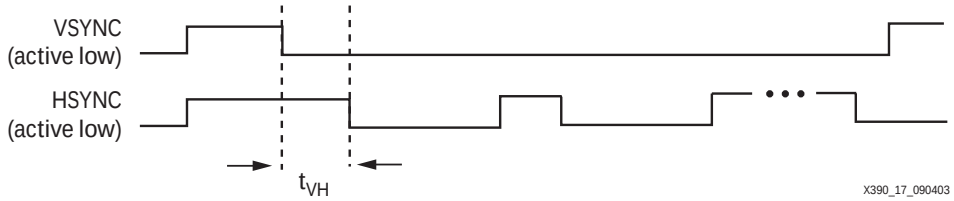


Figure 17: **VSYNC & HSYNC Phase Difference Timing**

LCD Control Logic

Figure 18 below illustrates the logic components necessary to use the CoolRunner-II CPLD to interface to the Optrex LCD. The lcd_start flag is generated by the Main Control Logic of the CPLD that released control of the memory to the LCD Control Logic. Once the LCD Control Logic has read an image from memory and sent the image data to the LCD, the lcd_done flag is asserted for the Main Control Logic.

The counters shown in Figure 18 are used for creating the timing specifications of the LCD display. VBP_CNT is a 17-bit counter for calculating the vertical back porch specification. HBP_CNT is a 6-bit counter that calculates the horizontal back porch specification. The vertical and horizontal back porch counters are separate counters, because they must both increment simultaneously. LINE_CNT is a 10-bit counter that keeps track of the number of lines for the LCD display. CLK_CNT is a general purpose 17-bit counter that is used for calculating HSYNC & VSYNC phase difference, HSYNC pulse width, VSYNC pulse width, HSYNC front porch, VSYNC front porch, and the number of pixels per line.

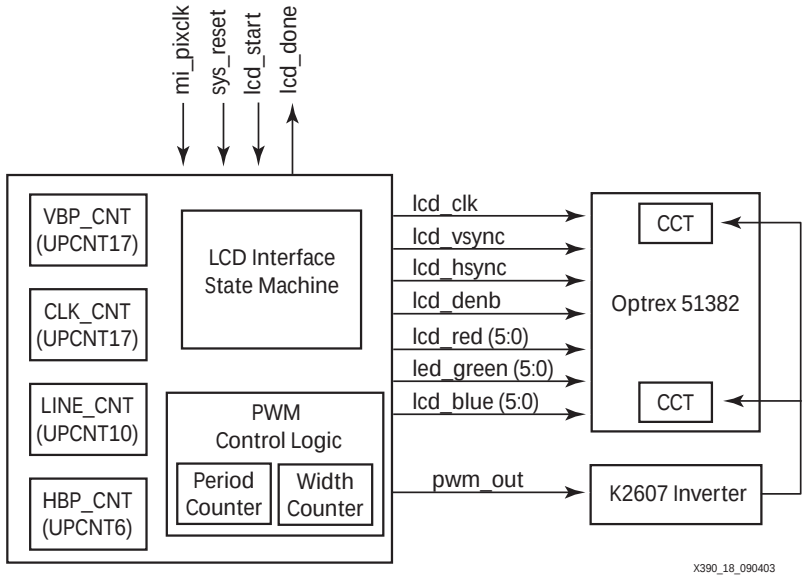


Figure 18: **LCD Interface Block Diagram**

The LCD state machine logic is shown below in Figure 19. The LCD state machine generates all the control signals to the Optrex LCD.

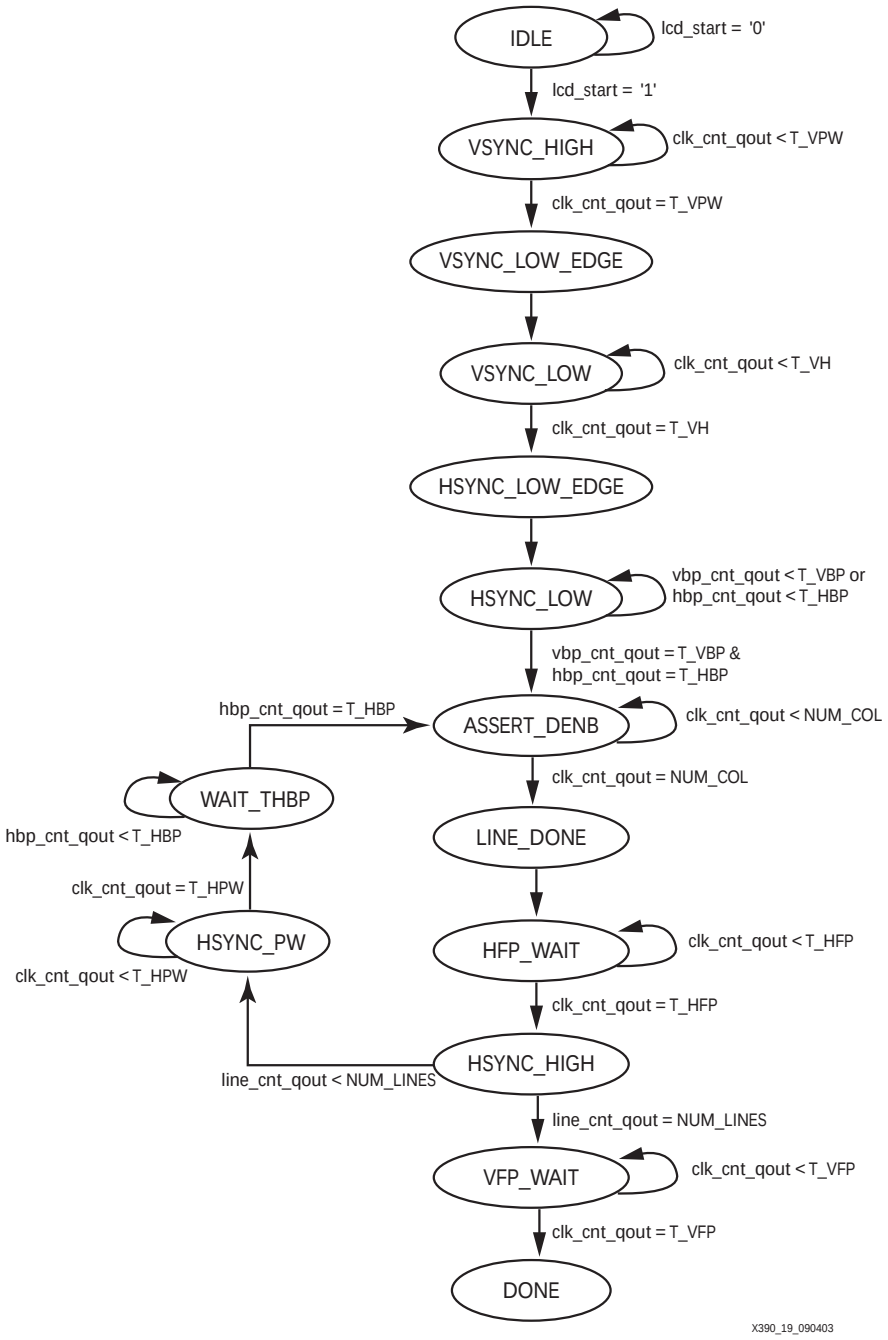


Figure 19: **LCD Interface State Machine**

A description of each state in the LCD state machine is provided in Table 7.

Table 7: **LCD State Machine Description**

State Name	State Purpose
IDLE	Wait for the assertion of lcd_start.
VSYNC_HIGH	De-assert lcd_vsync. Wait for t_{VPW} (VSYNC pulse width). Use CLK_CNT and wait for T_VPW. Also reset ADDR_CNT (SRAM address counter).

Table 7: **LCD State Machine Description**

State Name	State Purpose
VSYNC_LOW_EDGE	Assert lcd_vsync. Enable VBP_CNT (VSYNC back porch counter).
VSYNC_LOW	Wait for t_{VH} (VSYNC to HSYNC phase difference). See Figure 17. Use CLK_CNT and wait for T_VH.
HSYNC_LOW_EDGE	Assert lcd_hsync. Enable HBP_CNT (HSYNC back porch counter).
HSYNC_LOW	Wait for both VBP_CNT and HBP_CNT (VSYNC and HSYNC back porch counters) to reach T_VBP and T_HBP, respectively. Meet both t_{VBP} and t_{HBP} requirements.
ASSERT_DENB	Assert lcd_denb. Send data to LCD. Assign lcd_red, lcd_green, and lcd_blue signals. Enable CLK_CNT and wait for number of data pixels per row. Wait for CLK_CNT to reach NUM_COL.
LINE_DONE	This state is reached when all the pixel data has been shifted to LCD for the current line. Increment LINE_CNT (line counter).
HFP_WAIT	Wait for HSYNC front porch (t_{HFP}). Use CLK_CNT and wait until T_HFP is reached.
HSYNC_HIGH	De-assert lcd_hsync. Compare LINE_CNT to NUM_LINES. If max number of lines for LCD is reached proceed to VFP_WAIT state, else repeat sending line data to LCD.
HSYNC_PW	Wait for t_{HPW} (HSYNC pulse width). Use CLK_CNT and wait for T_HPW.
WAIT_THBP	Assert lcd_hsync. Wait for t_{HBP} (HSYNC back porch). Use HBP_CNT and wait for T_HBP.
VFP_WAIT	Wait t_{VFP} (VSYNC front porch). Use CLK_CNT and wait for T_VFP.
DONE	De-assert lcd_vsync. Assert lcd_done flag.

PWM Logic

The PWM Logic of the CPLD is responsible for generating a pulse width modulated (or PWM) signal. The PWM signal controls the brightness of the LCD as an input to a DC to AC inverter. The PWM signal is an input to the ERG K2607 low profile DC to AC inverter that is designed specifically for the Optrex T51382 LCD. The overall period of the PWM signal should be approximately 5 ms, while the width (or active high time) can vary from 5% to 100% of the signal period. The K2607 inverter powers the dual cold cathode tubes (or CCT) of the Optrex LCD.

The PWM Logic in the CPLD mainly consists of two counters, a PERIOD counter and a WIDTH counter. The PERIOD counter counts the full cycle length of the PWM signal, while the WIDTH

counter controls the active high time of the PWM signal. Figure 20 illustrates the PWM signal generation.

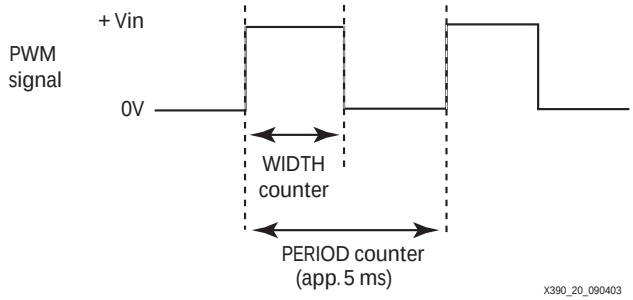


Figure 20: **PWM Signal Generation**

CoolRunner-II Implementation

Device Utilization

The current digital camera reference design is targeted to a CoolRunner-II XC2C256 TQ144 device. Table 8 below describes the utilization numbers for the digital camera reference design.

Table 8: **CoolRunner-II Design Utilization**

Parameter	Used	Available	% Utilization
I/O Pins	76	118	64 %
Macrocells	235	256	92 %
Product Terms	633	896	71 %
Registers	217	256	85 %
Function Block Inputs	501	640	78 %

Verification

The digital camera design functionality has been verified in functional simulation, post route timing simulation, and in hardware implementation. Test benches are provided in the VHDL code download pack.

VHDL Code

THIRD PARTIES MAY HAVE PATENTS ON THE CODE PROVIDED. BY PROVIDING THIS CODE AS ONE POSSIBLE IMPLEMENTATION OF THIS DESIGN, XILINX IS MAKING NO REPRESENTATION THAT THE PROVIDED IMPLEMENTATION OF THIS DESIGN IS FREE FROM ANY CLAIMS OF INFRINGEMENT BY ANY THIRD PARTY. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY OR CONDITIONS, EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, AND XILINX SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR A PARTICULAR PURPOSE, THE ADEQUACY OF THE IMPLEMENTATION, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OR REPRESENTATION THAT THE IMPLEMENTATION IS FREE FROM CLAIMS OF ANY THIRD PARTY. FURTHERMORE, XILINX IS PROVIDING THIS REFERENCE DESIGN "AS IS" AS A COURTESY TO YOU.

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Conclusion

CoolRunner-II CPLDs are low power devices targeted to portable, handheld electronics such as digital cameras. This reference design illustrates the complexity of logic that can be fit into a CPLD. This digital camera solution using CoolRunner-II CPLD to provide seamless integration between an image sensor, memory, and a LCD.

References

- Micron Technology, Inc. http://www.micron.com
- Video Demystified 3rd Edition. Keith Jack. 2001. Elsevier Science.
- Optrex of America, Inc. http://www.optrex.com

Glossary

AE - Auto Exposure

AWB - Auto White Balance

Back Porch - The portion of a video signal that occurs during blanking from the end of horizontal sync to the beginning of active video. The blanking signal portion which lies between the trailing edge of a horizontal sync pulse and the trailing edge of the corresponding blanking pulse. Color burst is located on the back porch

CCD - (Charge Coupled Device) An image sensor that reads the charges from the sensor's photosites one row at a time.

CCT- Cold Cathode Tube

CFA - (Color Filter Array) The filter dyes placed directly over each pixel on the chip surface.

CIF - (Common Interchange Format) 352x288 pixels; often used for H.261 and H.263 video codecs.

Color Correction - The process of correcting or enhancing the color of an image.

CMOS - (Complementary Metal Oxide Semiconductor) An imaging system used by digital cameras.

Digital Zoom - A digital magnification of the center 50% of an image. Digital zooms increase the apparent image size by interpolation. They do not increase the amount of image information.

Frame - One of the still pictures that make up a video.

Frame Grabber - A device that lets you capture individual frames out of a video camera or off a video tape.

Frame Rate - The number of frames that are shown or sent each second. Live action relates to a frame rate of 30 frames per second.

Front Porch - The blanking signal portion which lies between the end of the active picture information and the leading edge of horizontal sync.

Gamma - The light output of a CRT is not linear with respect to the voltage input. This non-linearity follows an exponential function that is known as gamma. The camera has the inverse gamma of the CRT so that the resulting stage light input to CRT light output transfer will be somewhat linear, given the restrictions of the video system.

IC - Integrated circuit.

IFP - Image flow processor.

Image Sensor - A solid-state device containing a photosite for each pixel in the image. Each photosite records the brightness of the light that strikes it during an exposure.

LCD - (Liquid Crystal Display) Two types: (1) a high-resolution color display device used in handheld televisions and digital photography viewfinders. (2) A monochrome information display using black alphanumeric characters on a gray/green background.

Photosite - A small area on the surface of an image sensor that captures the brightness for a single pixel in the image. There is one photosite for every pixel in the image.

Pixel - An individual element of either a CCD sensor or a digital image.

Resolution - Expressed as the number of pixels counted horizontally by the number of pixels counted vertically. It can be expressed as one of the following formats: QVGA (320 x 240), VGA (640 x 480), SVGA (800 x 600), XGA (1024 x 768) UXGA (1600 x 1200).

RGB - (Red, Green and Blue) The color system used in most digital cameras in which the image is separated by capturing the red, green, and blue light separately and then are re-combined to create a full color image.

Saturation - The degree to which a color is undiluted by white light. If a color is 100 percent saturated, it contains no white light. If a color has no saturation, it is a shade of gray.

TFT - (Thin Film Transistor) The type of hi-resolution color LCD screen used in many digital photography cameras.

VGA - An image resolution of 640 x 480 pixels.

Y,U,V - PAL luminance & color difference components. U and V are the names of the B-Y and R-Y color differences signals (respectively) when they are modulated onto subcarrier.

YPbPr - YPbPr represents component video connections, where luminance (Y) is represented by a green jack, separate from the color components blue (Pb) and red (Pr). Most high-definition sets today support this format. These colors should not be confused as RGB output.

Additional Information

CoolRunner-II Datasheets and Application Notes

Device Packages

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/27/04	1.0	Initial Xilinx release.
09/27/05	1.1	Fixed links in Additional Information